



# Complete 12-Bit 10 MSPS Monolithic A/D Converter

## SMD/883B

## AD872A

### Scope

This specification covers the detail requirements for a complete monolithic 12-bit, 10 MSPS A/D converter with an on-chip, high performance track-and-hold amplifier (THA) and voltage reference. The electrical specifications match the Standard Microcircuit Drawing (SMD) 5962-93060 in effect at the release of this data sheet. For a copy of the latest official SMD, contact DESC-ELDS.

### Part Number/Case Outline

For case outline dimensions, see Package Information Appendix of General Specification ADI-M-1000. The complete part numbers of these SMD and 883 devices are as follows:

Device Type	SMD Part Number	ADI 883B Part Number	Package Description	Package Designation ADI MIL-STD-1835
01	5962-9306001MXA	AD872ASD/883B	28-Pin Side Brazed DIP	D-28 CDIP2-T28
02	5962-9306002MYA	AD872ASE/883B	44-Terminal LCC	E-44A CQCCI-N44

### Absolute Maximum Ratings (T<sub>A</sub> = +25°C unless otherwise noted)<sup>1</sup>

AV <sub>DD</sub> to AGND	.....	-0.5 V to +6.5 V
AV <sub>SS</sub> to AGND	.....	-6.5 V to +0.5 V
DV <sub>DD</sub> , DRV <sub>DD</sub> <sup>2</sup> to DGND, DRGND <sup>2</sup>	.....	-0.5 V to +6.5 V
DRV <sub>DD</sub> to DV <sub>DD</sub> <sup>2</sup>	.....	-6.5 V to +6.5 V
DRGND to DGND <sup>2</sup>	.....	-0.3 V to +0.3 V
AGND to DGND	.....	-1 V to +1 V
AV <sub>DD</sub> to DV <sub>DD</sub>	.....	-6.5 V to +6.5 V
Clock Input, OEN <sup>2</sup> to DGND	.....	-0.5 V to DV <sub>DD</sub> + 0.5 V
Digital Outputs to DGND	.....	-0.5 V to DV <sub>DD</sub> + 0.3 V
REF IN to AGND	.....	AV <sub>SS</sub> to AV <sub>DD</sub>
V <sub>INA</sub> , to V <sub>INB</sub> , REF IN to AGND	.....	-6.5 V to +6.5 V
Storage Temperature Range	.....	-65°C to +150°C
Lead Temperature (Soldering 10 sec)	.....	+300°C

### Recommended Operating Conditions<sup>2</sup>

Operating Ambient Temperature Range	.....	-55°C to +125°C
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### Thermal Characteristics

Thermal Resistance, Junction-to-Case (θ <sub>JC</sub> ) for D-28	.....	28°C/W
Thermal Resistance, Junction-to-Ambient (θ <sub>JA</sub> ) for D-28	.....	60°C/W
Thermal Resistance, Junction-to-Case (θ <sub>JC</sub> ) for E-44A	.....	20°C/W
Thermal Resistance, Junction-to-Ambient (θ <sub>JA</sub> ) for E-44A	.....	70°C/W

### NOTES

<sup>1</sup>Permanent damage may occur if any absolute maximum rating is exceeded. Functional operation is not implied and device reliability may be impaired by exposure to higher-than-recommended voltages for extended periods of time.

<sup>2</sup>Device Type 02 only.

REV. B

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# AD872A—SPECIFICATIONS

**Table 1. Electrical Performance Characteristics**

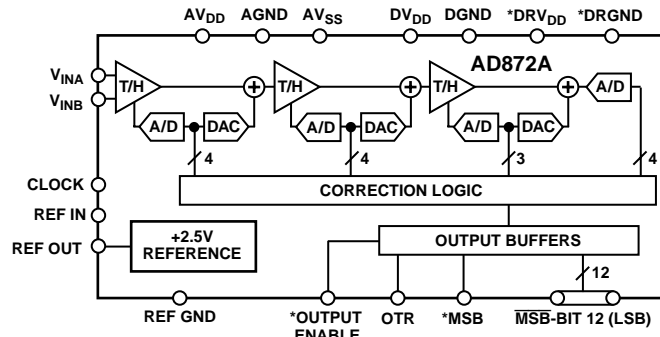
Test	Symbol	Conditions AV <sub>DD</sub> = +5 V, AV <sub>SS</sub> = -5 V, DV <sub>DD</sub> = +5 V, DRV <sub>DD</sub> = +5 V unless otherwise specified	Group A Subgroups	Device Type	Limits		Units
					Min	Max	
Resolution	RES		1, 2, 3	01, 02	12		Bits
Differential Nonlinearity <sup>1</sup>	DNL	All Codes Histogram	1, 2, 3	01, 02	12		Bits
Zero Error	B <sub>POE</sub>		1	01, 02		0.75	±% FSR
Gain Error	A <sub>E</sub>		1	01, 02		1.25	±% FSR
Zero Error Drift	TCB <sub>POE</sub>	External 2.5 V Reference	2, 3	01, 02		0.30	±% FSR
Gain Error Drift	TCA <sub>INT</sub>	Internal 2.5 V Reference	2, 3	01, 02		1.75	±% FSR
Gain Error Drift	TCA <sub>EXT</sub>	External 2.5 V Reference	2, 3	01, 02		0.5	±% FSR
Power Supply Rejection	PSR	See Note 2	1, 2, 3	01, 02		0.125	±% FSR
Analog Input Range	V <sub>IN</sub>		1, 2, 3	01, 02		1	±V
Input Resistance	R <sub>IN</sub>	T <sub>A</sub> = +25°C		01, 02	50 typ		kΩ
Input Capacitance	C <sub>IN</sub>	T <sub>A</sub> = +25°C		01, 02	10 typ		pF
Internal Reference Output Voltage	V <sub>REF</sub>		1, 2, 3	01, 02	2.46	2.54	V
Power Dissipation	PD		1, 2, 3	01, 02		1.3	W
Power Supply Current	I <sub>AV<sub>DD</sub></sub>		1, 2, 3	01, 02		92	mA
	I <sub>AV<sub>SS</sub></sub>					150	
	I <sub>DV<sub>DD</sub></sub>					21	
	I <sub>DRV<sub>DD</sub></sub>			02	2		
Signal-to-Noise and Distortion Ratio	S/(N + D)	f <sub>IN</sub> = 1 MHz; f <sub>S</sub> = 10 MHz	1, 2, 3	01	61		dB
				02	60		
Total Harmonic Distortion	THD	f <sub>IN</sub> = 1 MHz; f <sub>S</sub> = 10 MHz	1, 2, 3	01		-62	dB
				02		-60	
Logic Input High Voltage	V <sub>IH</sub>		1, 2, 3	01, 02	2.0		V
Logic Input Low Voltage	V <sub>IL</sub>		1, 2, 3	01, 02		0.8	V
Logic Input High Current (CLK)	I <sub>IH</sub>		1, 2, 3	01		115	±μA
Logic Input Low Current (CLK)	I <sub>IL</sub>		1, 2, 3	01		115	±μA
Logic Input High Current (OEN, CLK)	I <sub>IH</sub>		1, 2, 3	02		115	±μA
Logic Input Low Current (OEN, CLK)	I <sub>IL</sub>		1, 2, 3	02		115	±μA
Logic Output High Voltage (MSB—Bit 12, OTR)	V <sub>OH</sub>	I <sub>SOURCE</sub> = 500 μA	1, 2, 3	01, 02	2.4		V
Logic Output Low Voltage (MSB—Bit 12, OTR)	V <sub>OL</sub>	I <sub>SINK</sub> = 1.6 mA	1, 2, 3	01, 02		0.4	V
Leakage	I <sub>Z</sub>	Three State	1, 2, 3	02		10	±μA
Clock Period	t <sub>C</sub>	See Figure 1.	9, 10, 11	01, 02	100		ns
Output Delay	t <sub>OD</sub>	See Figure 1.	9, 10, 11	01, 02	10		ns

NOTES

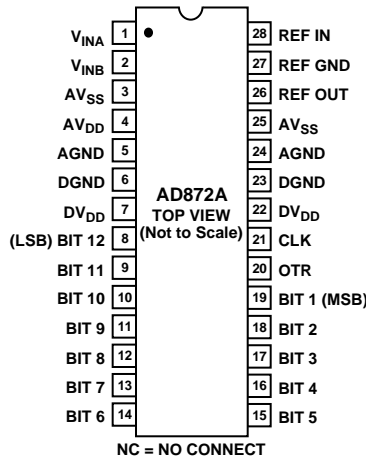
<sup>1</sup>Minimum resolution for which “No Missing Codes” is guaranteed.

<sup>2</sup>Test conditions for PSR: 4.75 V ≤ AV<sub>DD</sub> ≤ 5.25 V, -5.25 V ≤ AV<sub>SS</sub> ≤ -4.75 V, 4.75 V ≤ DV<sub>DD</sub> ≤ 5.25 V.

Functional Block Diagram and Terminal Assignment



D-28 Package



E-44A Package

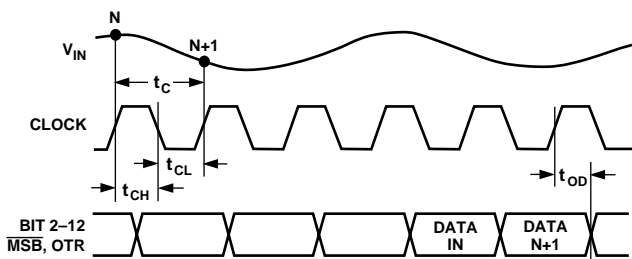
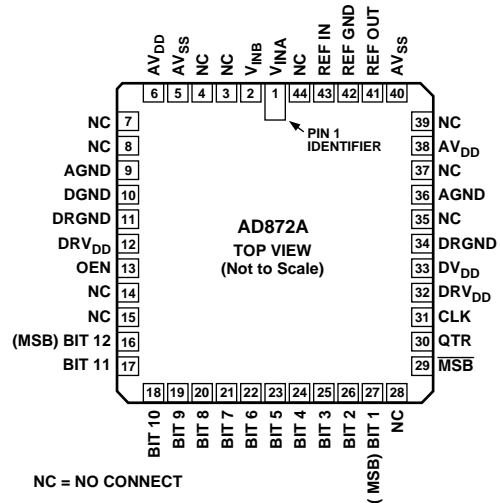


Figure 1. Timing Diagram

SWITCHING SPECIFICATIONS

( $T_{MIN}$  to  $T_{MAX}$  with  $AV_{DD} = +5 V$ ,  $DV_{DD} = +5 V$ ,  $DRV_{DD} = +5 V$ ,  $AV_{SS} = -5 V$ ;  $V_{IL} = 0.8 V$ ,  $V_{IH} = 2.0 V$ . These characteristics are included for design guidance only and are not tested or guaranteed.)

Parameter	Symbol	Limits	Units
CLOCK Pulse Width High	$t_{CH}$	45	ns min
CLOCK Pulse Width Low	$t_{CL}$	45	ns min
Clock Duty Cycle		40	% min (50% typ)
		60	% max
Pipeline Delay (Latency)		3	Clock Cycles

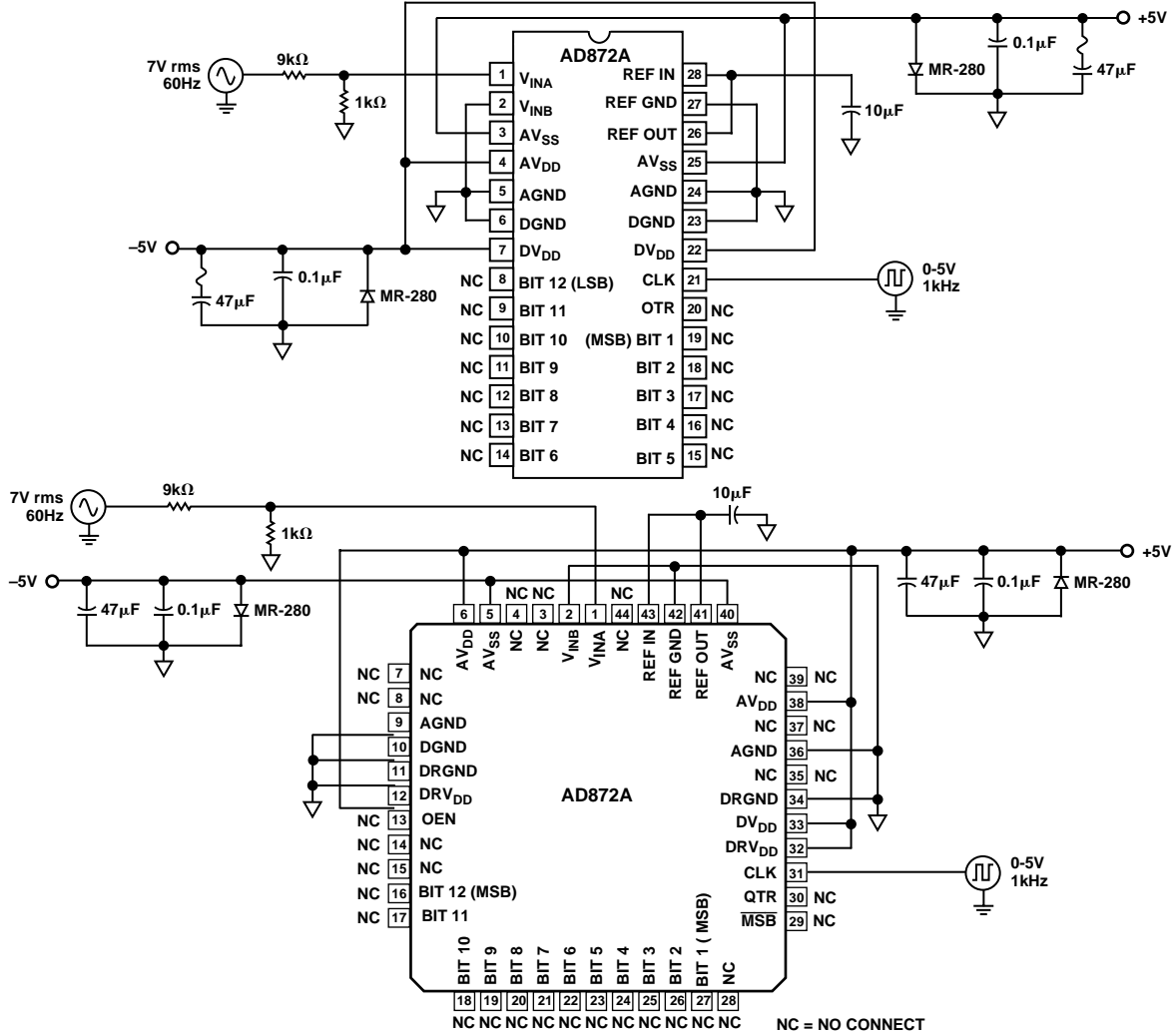
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Microcircuit Technology Group

This microcircuit is covered by technology group (93).

## Life Test /Burn-In Circuit

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

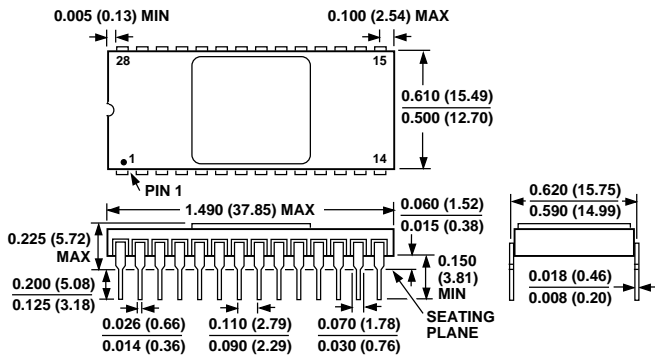


## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### D-28

28-Lead Side Brazed DIP



### E-44A

44-Terminal Ceramic Leadless Chip Carrier

