

TFF1115HN

Low phase noise LO generator for VSAT applications

Rev. 1 — 24 March 2011

Product data sheet

1. General description

The TFF1115HN is a K_u band frequency generator intended for low phase noise Local Oscillator (LO) circuits for K_u band VSAT transmitters and transceivers. The specified phase noise complies with IESS-308 from Intelsat.

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

2. Features and benefits

- Phase noise compliant with IESS-308 (Intelsat) in combination with appropriate source
- LO generator with VCO range from 11.30 GHz to 11.80 GHz
- Input signal 44 MHz to 738 MHz
- Divider settings 16, 32, 64, 128 or 256
- Output level -4 dBm; stability ± 2 dB
- Third or fourth order PLL
- Internally stabilized voltage references for loop filter

3. Applications

- VSAT up converters
- Local oscillator signal generation

4. Quick reference data

Table 1. Quick reference data
Operating conditions of [Table 10](#) apply.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		3.0	3.3	3.6	V
I_{CC}	supply current		-	100	130	mA
$f_{o(RF)}$	RF output frequency		11.30	-	11.80	GHz
$\varphi_{n(synth)}$	synthesizer phase noise	divider value = 64; at 100 kHz offset; reference phase noise is -149 dBc/Hz at 100 kHz offset	-	-97	-92	dBc/Hz
RL_{out}	output return loss	measured at demo board and de-embedded to footprint	-	-10	-	dB
$\alpha_{sup(sp)ref}$	reference spurious suppression	measured at divider value = 256	-	-	-70	dBc



8. Functional diagram

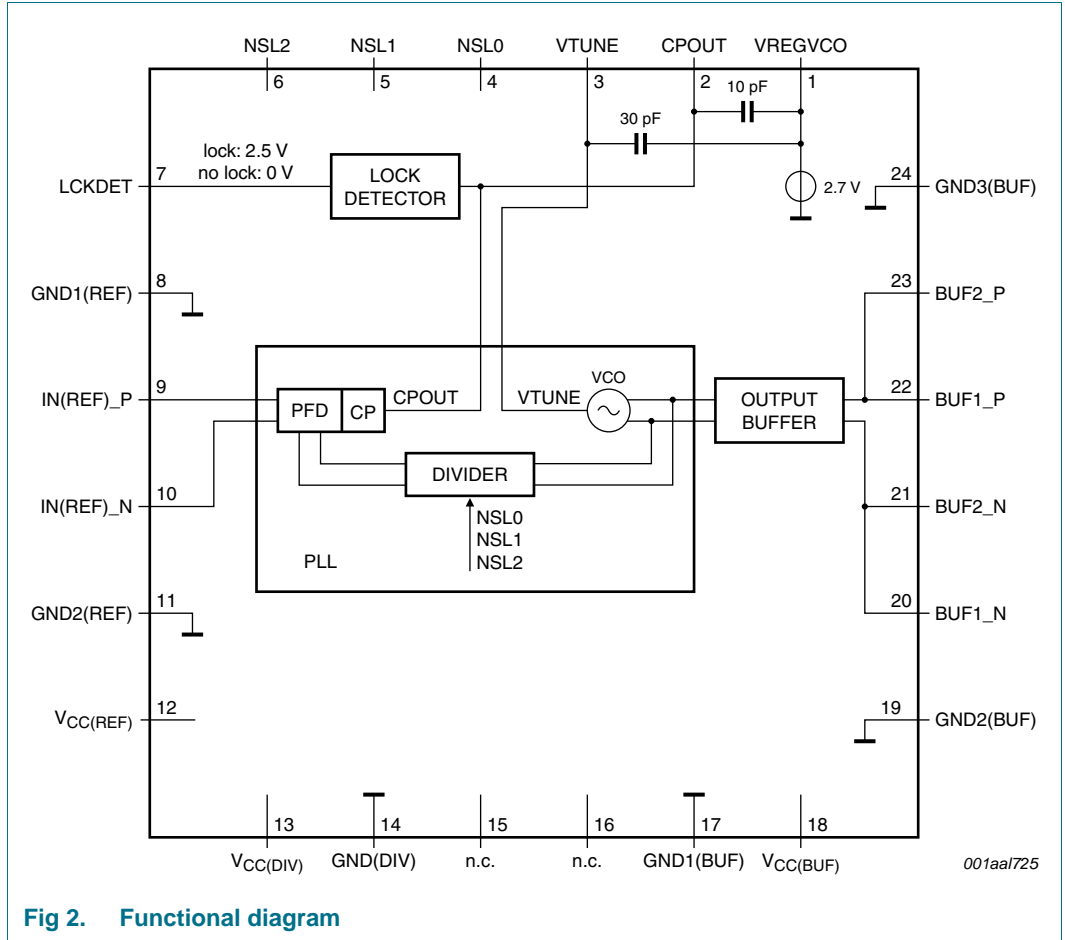


Fig 2. Functional diagram

9. Pinning information

9.1 Pinning

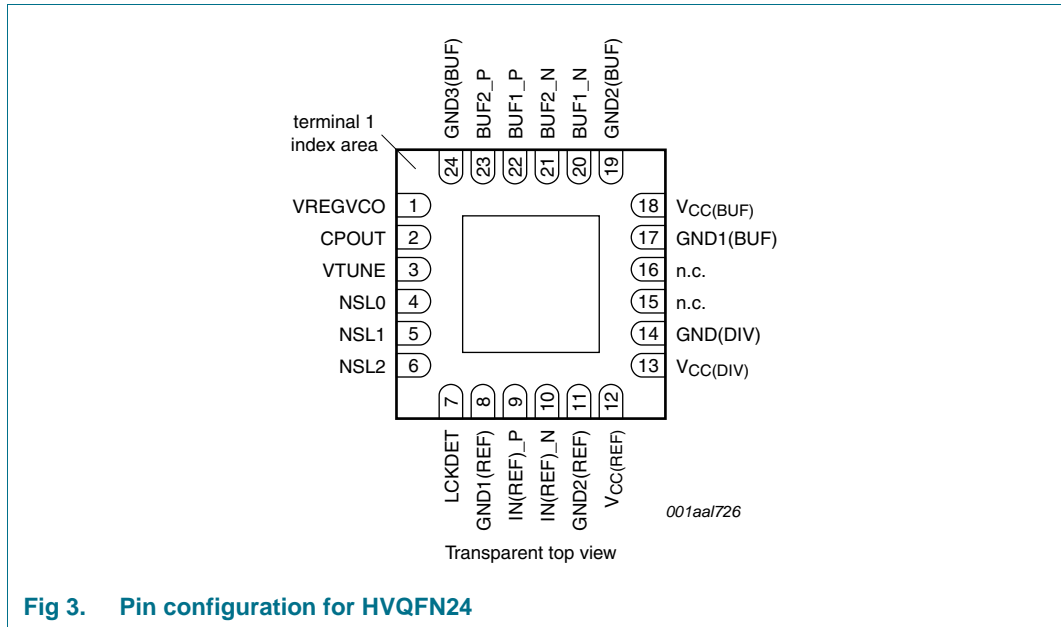


Fig 3. Pin configuration for HVQFN24

9.2 Pin description

Table 4. Pin description

Symbol	Pin	Description
VREGVCO	1	Regulated output voltage for VCO loop filter. Connect loop filter to this pin.
CPOUT	2	Charge pump output.
VTUNE	3	Tuning voltage for VCO.
NSL0	4	Divider setting, LSB. Leave open for "1", connect to GND for "0". See Table 8 .
NSL1	5	Divider setting. Leave open for "1", connect to GND for "0". See Table 8 .
NSL2	6	Divider setting, MSB. Leave open for "1", connect to GND for "0". See Table 8 .
LCKDET	7	Lock detect. Lock = 2.5 V; out of lock = 0 V. See Table 6 .
GND1(REF)	8	Ground for REF input. Connect this pin to the exposed diepad landing.
IN(REF)_P	9	Reference signal, non-inverting input. Couple this AC to the source.
IN(REF)_N	10	Reference signal, inverting input. Couple this AC to the source.
GND2(REF)	11	Ground for REF input. Connect this pin to the exposed diepad landing.
V _{CC} (REF)	12	Supply of the internal regulated voltages. Decouple this pin against GND2(REF) (pin 11).
V _{CC} (DIV)	13	Supply of the divider and PFD/CP. Decouple this pin against GND(DIV) (pin 14).
GND(DIV)	14	Ground of the divider. Connect this pin to the exposed diepad landing.
n.c.	15	not connected
n.c.	16	not connected
GND1(BUF)	17	Ground for RF output. Connect this pin to the exposed diepad landing.

Table 4. Pin description ...continued

Symbol	Pin	Description
V _{CC(BUF)}	18	Supply voltage for the RF output buffer. Decouple this pin against GND2(BUF) (pin 19).
GND2(BUF)	19	Ground for RF output. Connect this pin to the exposed diepad landing.
BUF1_N	20	RF output.
BUF2_N	21	RF output.
BUF1_P	22	RF output.
BUF2_P	23	RF output.
GND3(BUF)	24	Ground for RF output. Connect this pin to the exposed diepad landing.

10. Functional description

The TFF1115HN consists of the following blocks:

- PLL
- Output buffer
- Lock detector
- Reference input
- Divider settings

The functionality of the blocks will be discussed below.

10.1 PLL

The PLL is formed by the VCO, DIVIDER (possible settings: 16, 32, 64, 128 and 256 (see [Table 8](#))) and a PFD/CP. The tune voltage is referred to the band gap regulated voltage: VREGVCO (pin 1).

The loop filter can be set to type 2 or type 3. If a type 2 filter is used, the pins CPOUT (pin 2) and VTUNE (pin 3) must be interconnected. A 10 pF capacitor is placed internally between pins CPOUT (pin 2) and VREGVCO (pin 1), and a 30 pF capacitor is placed between pins VTUNE (pin 3) and VREGVCO (pin 1). See [Figure 4](#) and [Figure 5](#). Values for the loop filter components are given in [Table 5](#).

The VCO input voltage range is between 0.1 and 0.9 V_{O(reg)VCO}.

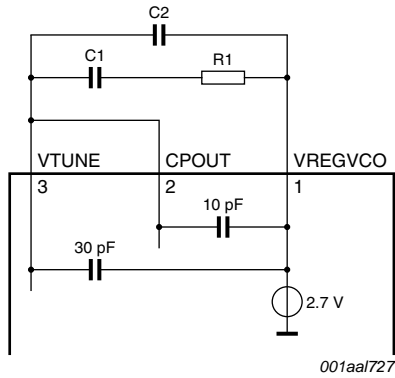


Fig 4. Type 2 loop filter

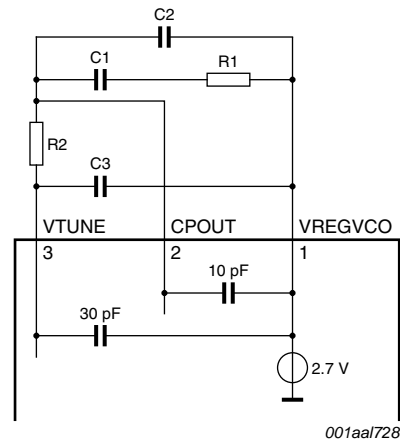


Fig 5. Type 3 loop filter

Table 5. Component values used for characterization

$f_{i(ref)}$ (MHz)	Divider value	C1 (nF)	C2 (pF)	C3 (pF)	R1 (Ω)	R2 (Ω)
44.141 to 46.094	256	27	82	33	470	560
88.281 to 92.188	128	18	82	33	330	560
176.563 to 184.375	64	18	120	33	270	560
353.125 to 368.750	32	33	270	33	120	560
706.250 to 737.500	16	68	560	33	68	560

10.2 Output buffer

The output consists of a differential pair with 50 Ω collector resistors R_{BUF_P} and R_{BUF_N} . If only one output is used, terminate the non used output with the same impedance as the load (see [Figure 8](#))

10.3 Lock detector

The lock detector is the output of a window detector. The window detector compares the output voltage over the charge pump. This voltage is identical to VTUNE when a type 2 loop filter is used (see [Figure 4](#)). In case of a type 3 loop filter this voltage is filtered by R2/C3 (see [Figure 5](#)). Due to this filtering the attack and decay time will decrease.

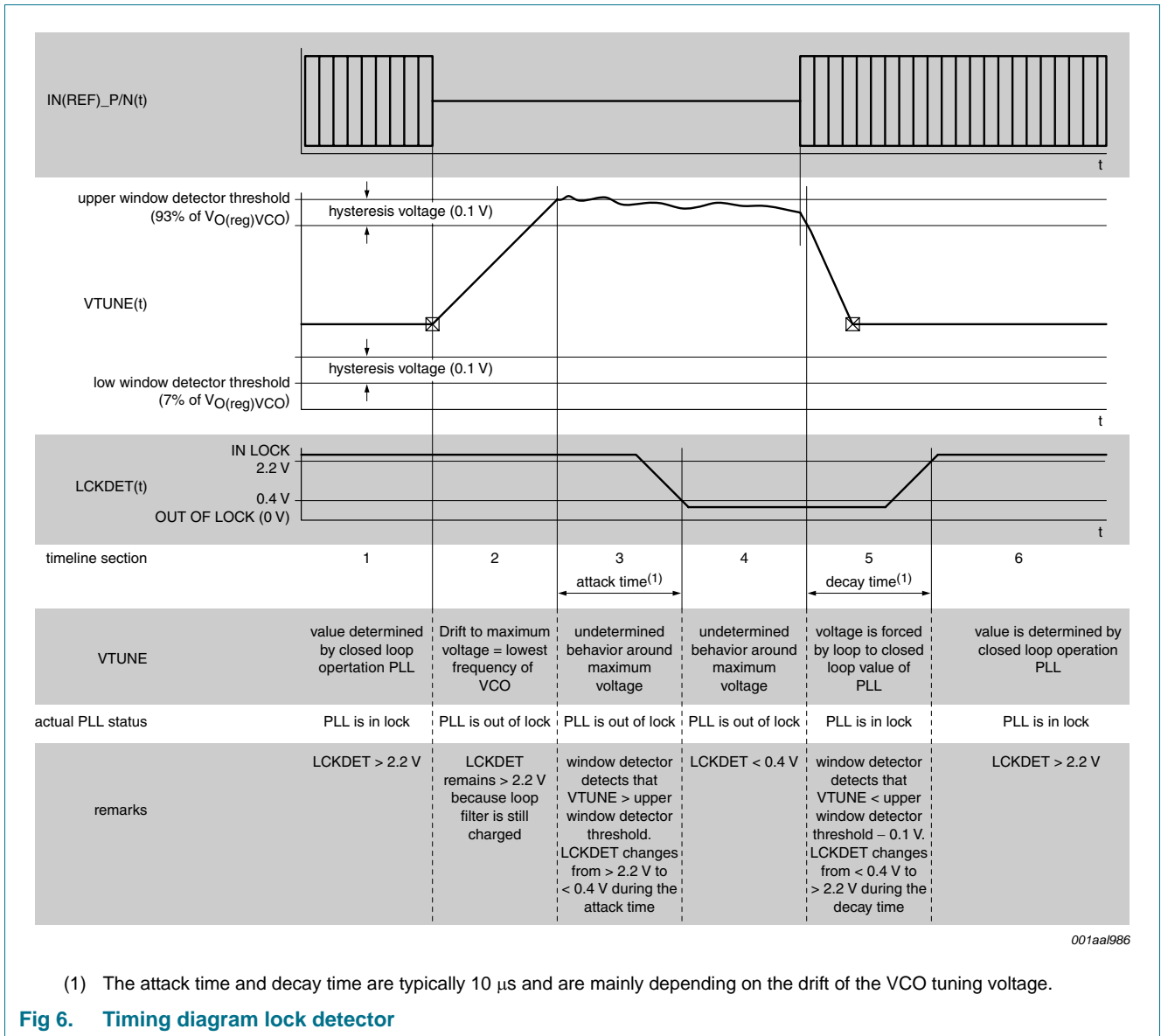
The lower window detector threshold voltage is 7 % of the output voltage on VREGVCO (pin 1), the upper window detector threshold voltage is 93 % of the output voltage on VREGVCO (pin 1). The hysteresis is 0.1 V. The output is 2.5 V CMOS compliant. The values are shown in [Table 6](#). The timing diagram is shown in [Figure 6](#).

At start-up the LCKDET (pin 7) will be LOW until the circuit has acquired lock.

Table 6. Logical value and physical value for lock detect (LCKDET)

Logical value	Physical value	Lock detect state
0	0 V	out of lock
1	2.5 V	lock

LCKDET (pin 7) has a pull-down resistor of 100 kΩ to GND1(REF) (pin 8).



10.4 Reference input (IN(REF)_P, IN(REF)_N)

The reference input is a differential pair and is internally biased. The input is high ohmic. The input signal must be AC coupled. If used in a single ended mode, the not used input must be terminated with the same impedance as the driving source.

An example of the differential source and two single ended loads are shown in [Figure 7](#). An example of a single ended application is shown in [Figure 8](#).

Note that the phase noise of the output signal is also determined by the phase noise of the reference signal. The reference frequency range is equal to the output frequency / division value. Note that the output frequency is guaranteed from 11.30 GHz to 11.80 GHz.

10.5 Divider settings (NSL2, NSL1, NSL0)

The divider can be set to 16, 32, 64, 128 and 256 (See [Table 8](#)). The logic levels for NSL0 (pin 4), NSL1 (pin 5) and NSL2 (pin 6) are given in [Table 7](#).

The pins have a pull-up resistor of 100 k Ω to $V_{CC(DIV)}$ (pin 13).

The device is only guaranteed when NSL2, NSL1 and NSL0 are predefined at start-up (no change of divider value is allowed during operation).

Table 7. Logical and physical value for divider setting (NSL2, NSL1, NSL0)

Logical value	Physical value
0	GND
1	open or V_{CC}

The truth table is shown in [Table 8](#).

Table 8. Divider setting as function of NSL2, NSL1 and NSL0

Setting number	NSL2	NSL1	NSL0	Divider value
0	0	0	0	16
1	0	0	1	32
2	0	1	0	64
3	0	1	1	128
4	1	0	0	256
5	1	0	1	[1]
6	1	1	0	[1]
7	1	1	1	[1]

[1] Test mode, divider output will be disabled.

11. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(REF)}$	reference supply voltage		-0.5	+3.6	V
$V_{CC(DIV)}$	divider supply voltage		-0.5	+3.6	V
$V_{CC(BUF)}$	buffer supply voltage		-0.5	+3.6	V
T_j	junction temperature		-40	+125	$^{\circ}\text{C}$
T_{stg}	storage temperature		-40	+125	$^{\circ}\text{C}$

12. Recommended operating conditions

Table 10. Operating conditions

NSL0 (pin 4), NSL1 (pin 5) and NSL2 (Pin 6) not changed during operation.
Loop filter component values as depicted in [Table 5](#) are used.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb}	ambient temperature		-40	+25	+85	°C
Z_0	characteristic impedance		-	50	-	Ω
$\varphi_{n(ref)}$	reference phase noise	divider value = 16	[1]	-	-	-134 dBc/Hz
		divider value = 32	[1]	-	-	-143 dBc/Hz
		divider value = 64	[1]	-	-	-149 dBc/Hz
		divider value = 128	[1]	-	-	-150 dBc/Hz
		divider value = 256	[1]	-	-	-151 dBc/Hz
$f_{i(ref)}$	reference input frequency	$f_{i(ref)} = f_{o(RF)} / \text{divider value}$	44	-	738	MHz
$P_{i(ref)}$	reference input power		-10	-	0	dBm

[1] Required reference phase noise is set 10 dB below equivalent input phase noise.

13. Thermal characteristics

Table 11. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		25	K/W

14. Characteristics

Table 12. Characteristics

Operating conditions of [Table 10](#) apply.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V_{CC}	supply voltage		3.0	3.3	3.6	V	
I_{CC}	supply current		-	100	130	mA	
PLL							
$f_{o(RF)}$	RF output frequency		11.30	-	11.80	GHz	
$V_{O(reg)VCO}$	VCO regulator output voltage		2.5	2.7	2.9	V	
I_{cp}	charge pump current		-	1	-	mA	
K_O	VCO steepness		[1]	0.6	-	GHz/V	
$\varphi_{n(VCO)}$	VCO phase noise	at 10 MHz offset	-	-130	-	dBc/Hz	
$\varphi_{n(synth)}$	synthesizer phase noise	divider value = 64; at 100 kHz offset; reference phase noise is -149 dBc/Hz at 100 kHz offset	-	-97	-92	dBc/Hz	
Output buffer							
P_o	output power	measured single ended	[2]	-6	-4	-2	dBm
RL_{out}	output return loss	measured at demo board and de-embedded to footprint	-	-10	-	dB	
$\alpha_{sup(sp)ref}$	reference spurious suppression	measured at divider value = 256	-	-	-70	dBc	

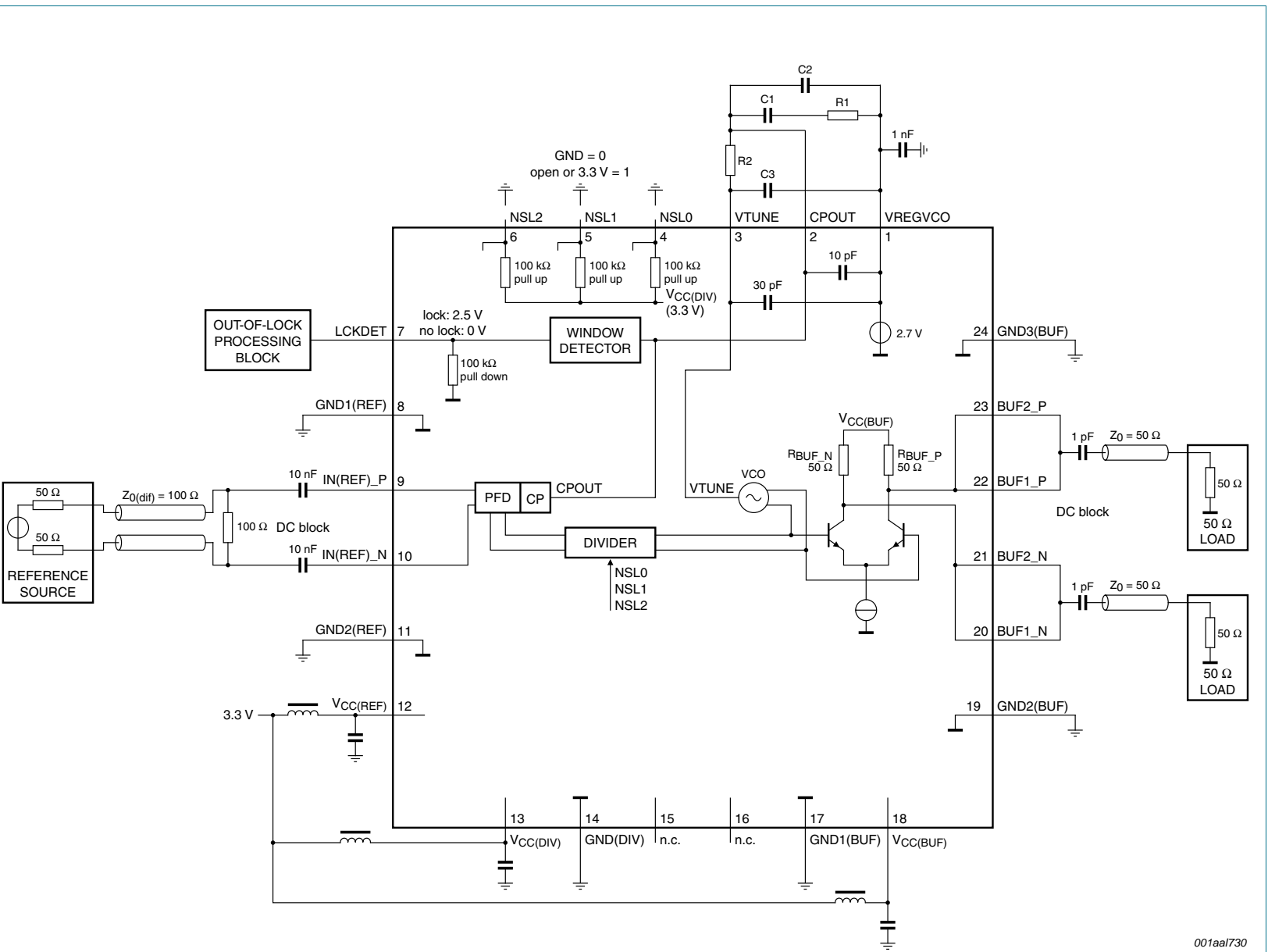
Table 12. Characteristics ...continued
 Operating conditions of [Table 10](#) apply.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\alpha_{H(LO)}$	LO harmonic rejection		-	-10	-	dBc
Lock detector						
V_{OL}	LOW-level output voltage	$I_O = 1 \text{ mA}$	-	-	0.4	V
V_{OH}	HIGH-level output voltage	$I_O = -1 \text{ mA}$	2.2	-	-	V
R_{pd}	pull-down resistance		70	100	130	$k\Omega$
Divider setting (NSL0, NSL1, NSL2)						
R_{pu}	pull-up resistance		70	100	130	$k\Omega$
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V

[1] The typical ratio of the maximum K_O in relation to the minimum K_O is 1.25.

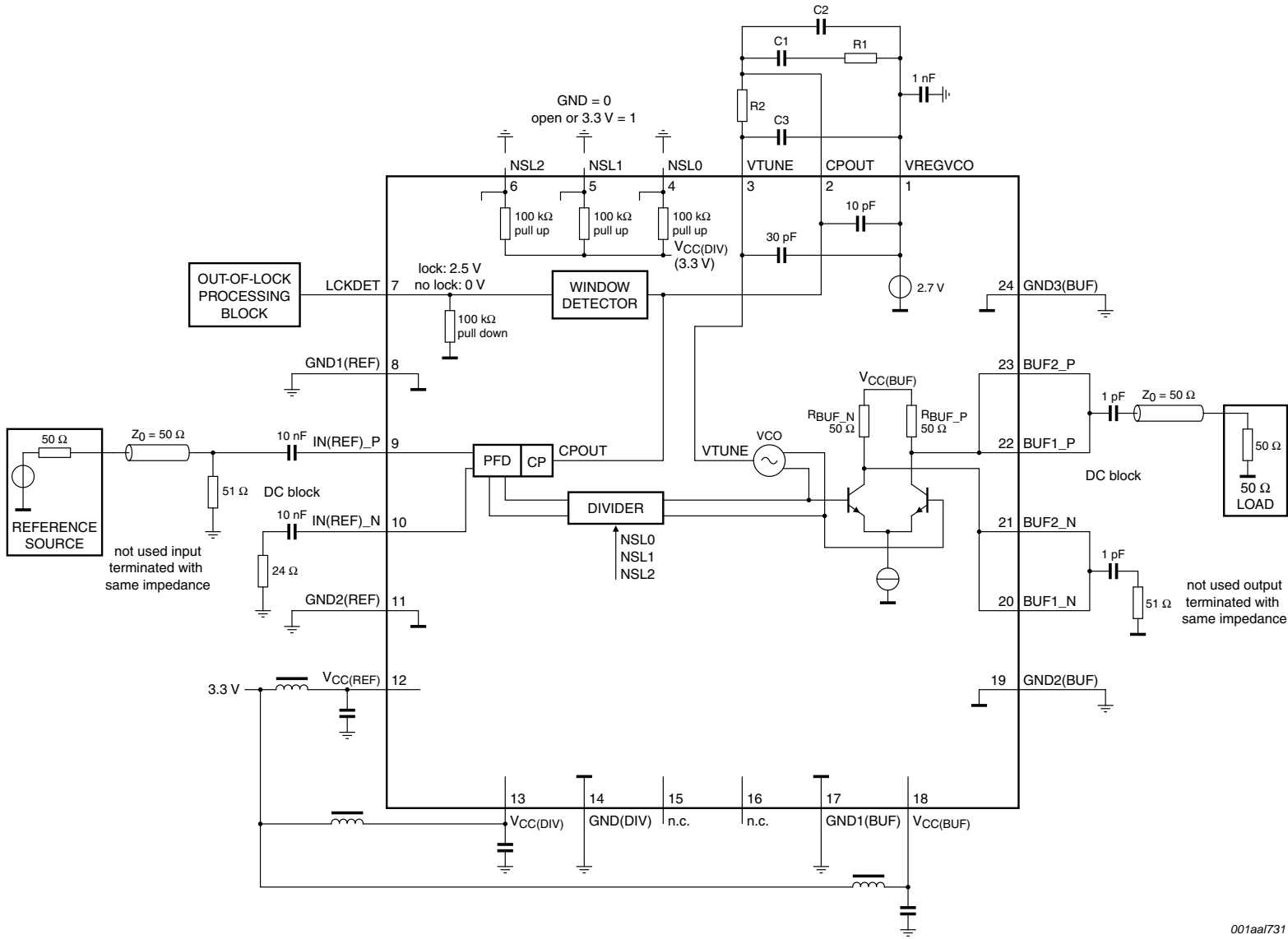
[2] Output stage is a differential pair with 50Ω collector impedances.
 Output power is measured per output pin for the fundamental tone only.
 Output is DC coupled and is AC coupled in on-board.

15. Application information



001aa1730

Fig 7. Application diagram with differential source for IN(REF) and both outputs driving a load, loop filter is type 3



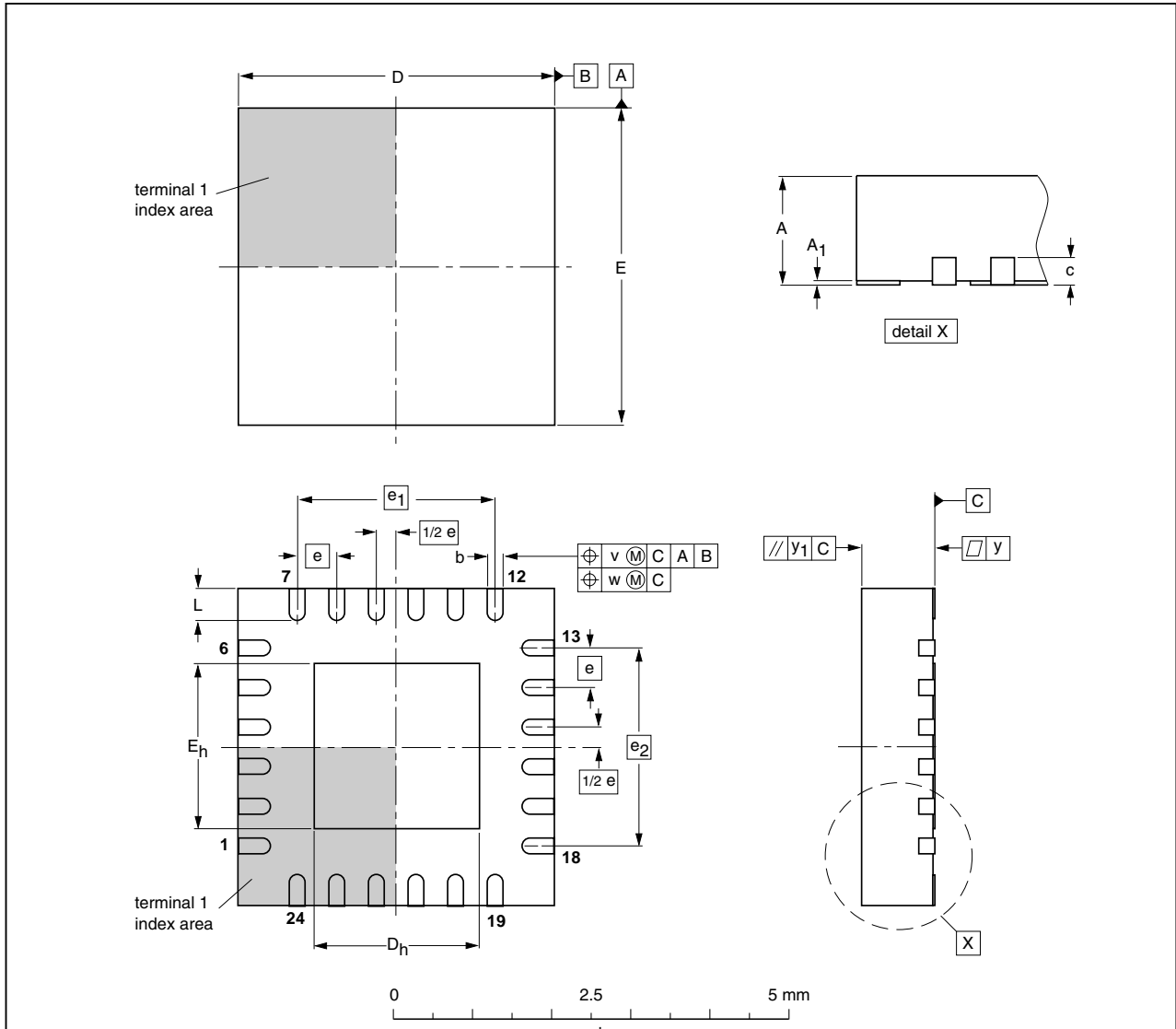
001aal731

Fig 8. Application diagram with single ended source for IN(REF) and single ended load, loop filter is type 3

16. Package outline

HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm

SOT616-1



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾ max.	A ₁	b	c	D ⁽¹⁾	D _h	E ⁽¹⁾	E _h	e	e ₁	e ₂	L	v	w	y	y ₁
mm	1	0.05 0.00	0.30 0.18	0.2	4.1 3.9	2.25 1.95	4.1 3.9	2.25 1.95	0.5	2.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT616-1	---	MO-220	---			01-08-08- 02-10-22

Fig 9. Package outline SOT616-1 (HVQFN24)

17. Abbreviations

Table 13. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
CP	Charge Pump
K _u band	K-under band
LSB	Least Significant Bit
MSB	Most Significant Bit
PFD	Phase Frequency Detector
PLL	Phase-Locked Loop
VCO	Voltage Controlled Oscillator
VSAT	Very Small Aperture Terminal

18. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TFF1115HN v.1	20110324	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

19.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

19.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any

liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

19.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

20. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

21. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Quick reference data	1
5	Ordering information	2
6	Marking	2
7	Block diagram	2
8	Functional diagram	3
9	Pinning information	4
9.1	Pinning	4
9.2	Pin description	4
10	Functional description	5
10.1	PLL	5
10.2	Output buffer	6
10.3	Lock detector	6
10.4	Reference input (IN(REF)_P, IN(REF)_N)	7
10.5	Divider settings (NSL2, NSL1, NSL0)	8
11	Limiting values	8
12	Recommended operating conditions	9
13	Thermal characteristics	9
14	Characteristics	9
15	Application information	11
16	Package outline	13
17	Abbreviations	14
18	Revision history	14
19	Legal information	15
19.1	Data sheet status	15
19.2	Definitions	15
19.3	Disclaimers	15
19.4	Trademarks	16
20	Contact information	16
21	Contents	17

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2011.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 24 March 2011

Document identifier: TFF11115HN