SY87813L

3.3V, 28Mbps to 1.3Gbps AnyRate® Clock and Data Recovery

General Description

The SY87813L is a complete clock recovery and data retiming integrated circuit for data rates from 28Mbps up to 1.3Gbps NRZ. The device is ideally suited for SONET/SDH/ATM and Fibre Channel applications and other high-speed data transmission systems.

Clock recovery and data retiming is performed by synchronizing the on-chip VCO directly to the incoming data stream. The VCO center frequency is controlled by the reference clock frequency and the selected divide ratio. On-chip clock generation is performed through the use of a frequency multiplier PLL with a byte rate source as reference.

The SY87813L also includes a link fault detection circuit.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

AnyRate®

Features

- 3.3V power supply
- SONET/SDH/ATM compatible
- Clock and data recovery from 28Mbps up to 1.3Gbps NRZ data stream; clock generation from 28MHz to 1.3GHz
- Two on-chip PLLs: one for clock generation and another for clock recovery
- Selectable reference frequencies
- Differential PECL high-speed serial I/O
- Line receiver input: no external buffering needed
- Link fault indication
- 100K ECL-compatible I/O
- Industrial temperature range (–40°C to +85°C)
- Available in 32-pin EPAD-TQFP

Applications

- SONET/SDH/ATM OC-1 and OC-3, OC-12, OC-24
- Fibre Channel, ESCON, SMPTE 259
- Gigabit Ethernet/Fast Ethernet
- Proprietary architecture up to 1.3Gbps
- CEPT E-3/E-4/E-5

Markets

- Telecom/Datacom
- Fiber optics
- Storage networks

AnyRate is a registered trademark of Micrel, Inc.

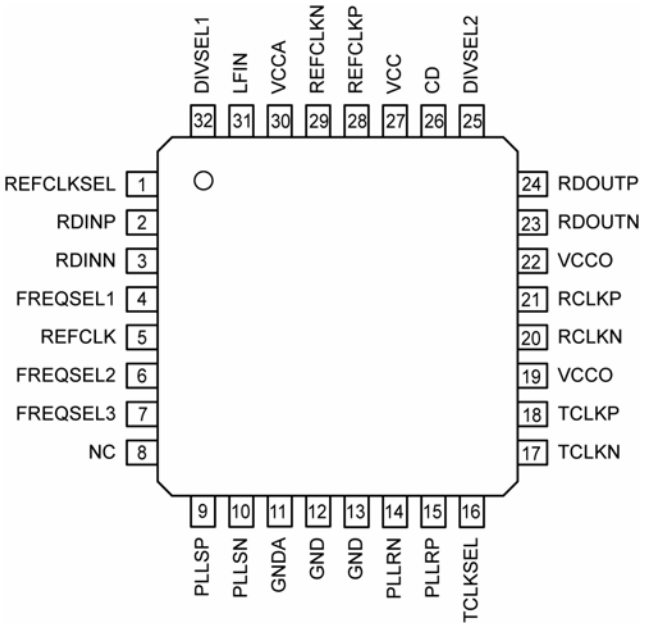
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY87813LHG	H32-1	Industrial	SY87813LHG with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY87813LHGTR[2]	H32-1	Industrial	SY87813LHG with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

Pin Configuration



32-Pin EPAD-TQFP (H32-1)

Pin Description

Pin Number	Pin Name	Pin Name
1	REFCLKSEL	REFCLK Select (TTL Input). This input selects the single-ended TTL REFCLK input or the differential PECL REFCLKP/REFCLKN inputs. REFCLKSEL = HIGH selects PECL inputs.
2 3	RDINP, RDINN	Serial Data Input. Differential PECL: These built-in line receiver inputs are connected to the differential receive serial data stream. An internal receive PLL recovers the embedded clock (RCLK) and data (RDOUT) information. The incoming data rate can be within one of eight frequency ranges depending upon the state of the FREQSEL pins. See “Frequency Selection” Table.
4 6 7	FREQSEL1 FREQSEL2 FREQSEL3	Frequency Select. TTL Inputs: These inputs select the output clock frequency range as shown in the “Frequency Selection” Table.
5 28 29	REFCLK, REFCLKP, REFCLKN	Reference Clock. (Input): These inputs are used as the reference for the internal frequency synthesizer and the “training” frequency for the receiver PLL to keep it centered in the absence of data coming in on the RDIN inputs. REFCLK is single-ended TTL and REFCLKP and REFCLKN are differential PECL inputs selected by the REFCLKSEL pin
26	CD	Carrier Detect. PECL Input: This input controls the recovery function of the Receive PLL and can be driven by the carrier detect output of optical modules or from external transition detection circuitry. When this input is HIGH, the input data stream (RDIN) is recovered normally by the Receive PLL. When this input is LOW the data on the inputs RDIN will be internally forced to a constant LOW, the data outputs RDOUT will remain LOW, the Link Fault Indicator output LFIN forced LOW and the clock recovery PLL forced to lock onto the clock frequency generated from REFCLK.
8	NC	No connect.
9 10	PLLSP PLLSN	Clock Synthesis PLL Loop Filter: External loop filter pins for the clock synthesis PLL.
11	GNDA	Analog Ground.
12, 13	GND	Ground. Ground pin and exposed pad must be connected to the same ground plane.
15 14	PLLRP PLLRN	Clock Recovery PLL Loop Filter. External loop filter pins for the receiver PLL.
16	TCLKSEL	Clock Select. TTL Input: This input is used to select either the recovered clock of the receiver PLL (TCLKSEL = HIGH) or the clock of the frequency synthesizer (TCLKSEL = LOW) to the TCLK outputs.
18 17	TCLKP, TCLKN	Clock Output (Differential PECL): The PECL 100k outputs represent either the recovered clock (TCLKSEL = HIGH) used to sample the recovered data (RDOUT) or the transmit clock of the frequency synthesizer (TCLKSEL = LOW). These outputs must be terminated with 50Ω to V_{CC}-2V or equivalent. This applies even if these outputs are not used.
19, 22	VCCO	Output Supply Voltage. Bypass with 0.1µF//0.01µF low ESR capacitors as close to V_{CC} pins as possible.[1]
21 20	RCLKP, RCLKN	Clock Output (Differential PECL): These PECL 100k outputs represent the recovered clock used to sample the recovered data (RDOUT).
24 23	RDOUTP RDOUTN	Receive Data Output (Differential PECL): These PECL 100k outputs represent the recovered data from the input data stream (RDIN). This recovered data is specified against the rising edge of RCLK. These outputs must be terminated with 50Ω to V_{CC}-2V or equivalent. This applies even if these outputs are not used.
32 25	DIVSEL1 DIVSEL2	Divider Select. TTL Inputs: These inputs select the ratio between the output clock frequency (RCLK/TCLK) and the REFCLK input frequency as shown in the “Reference Frequency Selection” Table.

Note:

1. VCC, VCCA, VCCO must be the same value.

Pin Description (continued)

Pin Number	Pin Name	Pin Name
27	VCC	Supply Voltage. Bypass with 0.1µF//0.01µF low ESR capacitors as close to V_{CC} pins as possible.(1)
30	VCCA	Analog Supply Voltage. Bypass with 0.1µF//0.01µF low ESR capacitors as close to V_{CC} pins as possible.(1)
31	LFIN	Link Fault Indicator (TTL Output): This output indicates the status of the input data stream RDIN. Active HIGH signal is indicating when the internal clock recovery PLL has locked onto the incoming data stream. LFIN will go HIGH if CD is HIGH and RDIN is within the frequency range of the Receive PLL (900ppm).

Note:

1. VCC, VCCA, VCCO must be the same value.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... -0.5V to +4.0V
Input Voltage (V_{IN}) ..... -0.5V to V_{CC}
Output Current (I_{OUT})
  Continuous ..... ±50mA
  Surge ..... ±100mA
Lead Temperature (soldering, 20sec.) ..... +260°C
Storage Temperature (T_s) ..... -65°C to +150°C

Operating Ratings[2]

Input Voltage (V_{CC}) ..... +3.15V to +3.45V
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Thermal Resistance[3]
  EPAD-TQFP (θ_{JA})
  0lfpm airflow ..... 27.6°C/W
  200lfpm airflow ..... 22.6°C/W
  500lfpm airflow ..... 20.7°C/W

DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage		3.15	3.3	3.45	V
I_{CC}	Power Supply Current			120	165	mA

PECL 100K DC Electrical Characteristics[4]

$V_{CC} = V_{CCO} = V_{CCA} = 3.3V \pm 5\%$; $R_L = 50\Omega$ to V_{CC}-2V; $T_A = –40°C$ to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		V_{CC}-1.165		V_{CC}-0.880	V
V_{IL}	Input LOW Voltage		V_{CC}-1.810		V_{CC}-1.475	V
V_{OH}	Output HIGH Voltage		V_{CC}-1.085		V_{CC}-0.880	V
V_{OL}	Output LOW Voltage		V_{CC}-1.830		V_{CC}-1.620	V
V_{OSW}	Output Voltage Swing		600	750	900	mV
I_{IL}	Input LOW Current	$V_{IN} = V_{IL}$ (Min)	0.5			µA

TTL DC Electrical Characteristics[4]

$V_{CC} = V_{CCO} = V_{CCA} = 3.3V \pm 5\%$; $T_A = –40°C$ to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage				0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = -0.4mA	2.0			V
V_{OL}	Output LOW Voltage	I_{OL} = 4mA			0.5	V
I_{IH}	Input HIGH Current	$V_{IN} = 2.7V$, V_{CC} = Max. $V_{IN} = V_{CC}$, V_{CC} = Max.	-175		 +100	µA µA
I_{IL}	Input LOW Current	$V_{IN} = 0.5V$, V_{CC} = Max.	-300			µA
I_{OS}	Output Short-Circuit Current	V_{OUT} = 0V, (Max., 1 sec.)	-15		-100	mA

Notes:

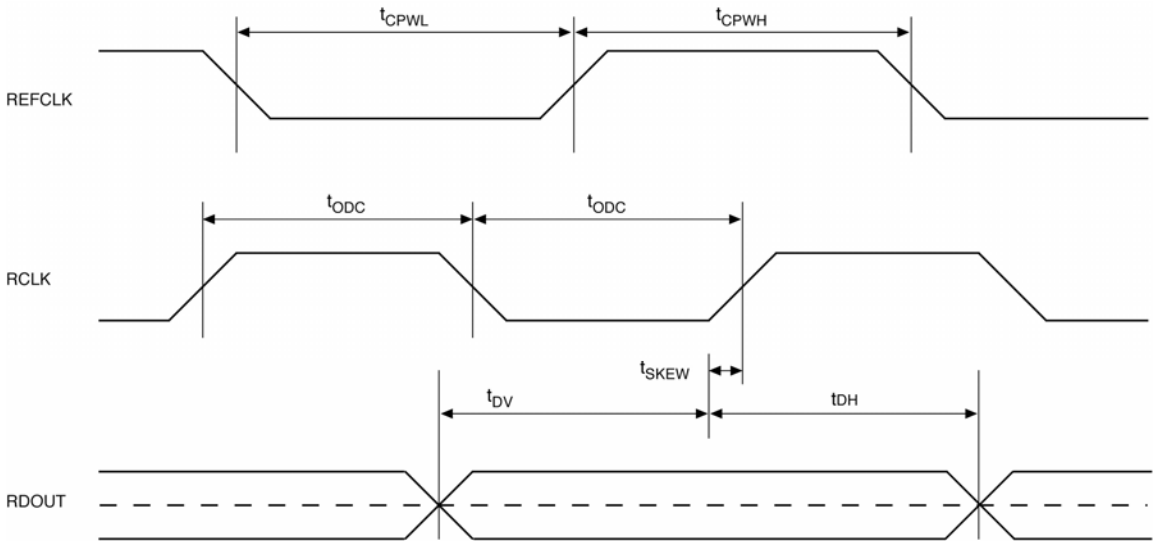
1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Using JEDEC standard test boards with die attach pad soldered to PCB. See www.amkor.com for additional package details.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics

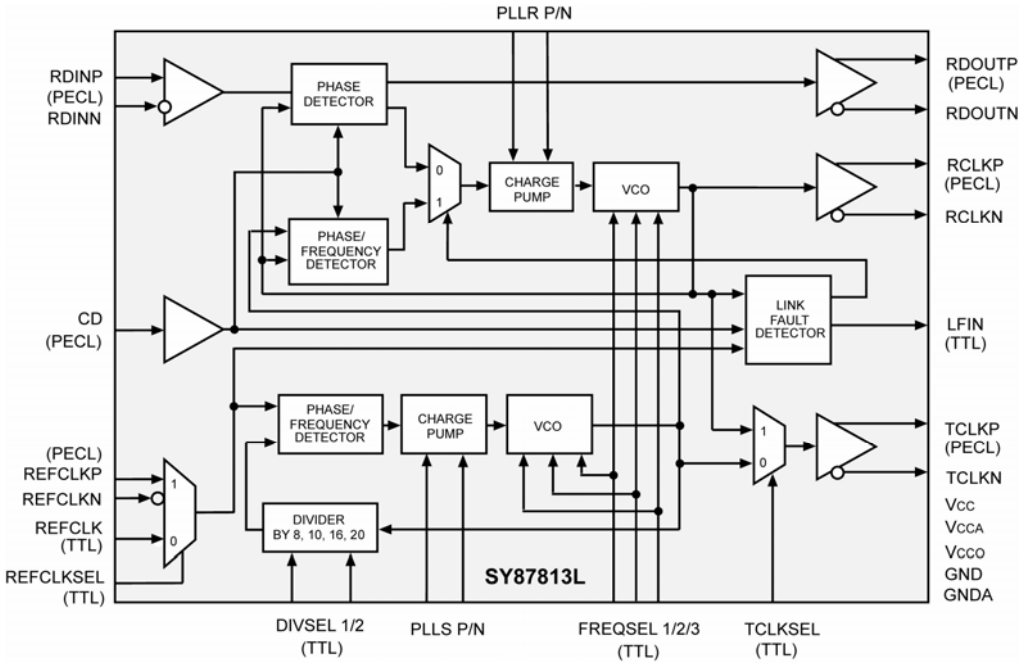
V_{CC} = V_{CCO} = V_{CCA} = 3.3V ±5%; R_L = 50Ω to V_{CC}-2V; T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{VCO}	VCO Center Frequency	f_{REFCLK} x Byte Rate	650		1300	MHz
Δf_{VCO}	VCO Center Frequency Tolerance	Nominal		5		%
t_{ACQ}	Acquisition Lock Time				15	µs
t_{CPWH}	REFCLK Pulse Width HIGH		3			ns
t_{CPWL}	REFCLK Pulse Width LOW		3			ns
t_{IRFT}	REFCLK TTL Input Rise Time			0.5	2	ns
t_{IRFP}	REFCLKN, REFCLKP PECL Input Rise/Fall Time (20% to 80%)				1.0	ns
t_{ODC}	Output Duty Cycle (RCLK/TCLK)		45		55	% of UI
t_r, t_f	PECL Output Rise/Fall Time (20% to 80%)		100		400	ps
t_{SKEW}	Recovered Clock Skew		-200		+200	ps
t_{DV}	Data Valid		1/(2xf_{RCLK}) -200			ps
t_{DH}	Data Hold		1/(2xf_{RCLK}) -200			ps

Timing Waveforms



Functional Block



Functional Description

Clock Recovery

Clock recovery, as shown in the block diagram, generates a clock that is at the same frequency as the incoming data bit rate at the serial data input. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency detector. Output pulses from the detector indicate the required direction of phase correction. These pulses are smoothed by a filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock.

Frequency, stability, without incoming data, is guaranteed by an alternate reference input (REFCLK or REFCLKP/N) that the PLL locks onto when data is lost. If the frequency of the incoming signal varies by greater than approximately 900ppm with respect to the synthesizer frequency, the PLL will be declared out of lock, and the PLL will lock to the reference clock.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal.

Lock Detect

The SY87813L contains a link fault indication circuit, which monitors the integrity of the serial data inputs. If the recovered serial data from RDIN is at the correct data rate (within 900ppm of the synthesizer frequency), the Link Fault Indicator (LFIN) output will then be asserted HIGH indicating an in-lock condition and will remain HIGH as long as this condition is met.

In the event that the recovered serial data is not at the correct data rate (greater than 900ppm difference from the synthesizer frequency), then LFIN output will go LOW indicating an out-of-lock condition. This condition will force the Clock and Data Recovery PLL (CDR) to lock onto the synthesizer frequency until it is within the correct frequency range (less than 900ppm difference from the synthesizer frequency). Once the CDR is within the correct frequency range, it will again lock onto the RDIN input.

Frequency Selection Table[1]

FREQSEL1	FREQSEL2	FREQSEL3	f_{VCO}/f_{RCLK}	f_{RCLK} (MHz)
0	0	0	1	650 - 1300
0	0	1	2	325 - 650
0	1	0	4	163 - 325
0	1	1	6	109 - 216
1	0	0	8	82 - 162
1	0	1	12	55 - 108
1	1	0	16	41 - 81
1	1	1	24	28 - 54

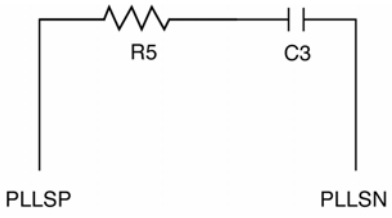
Note:

1. SY87813L operates from 28MHz to 1300MHz.

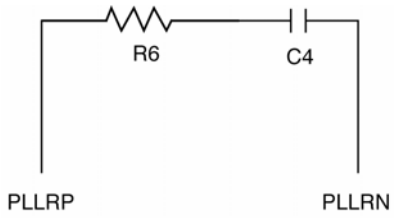
Reference Frequency Selection

DIVSEL1	DIVSEL2	f_{RCLK}/f_{REFCLK}
0	0	8
0	1	10
1	0	16
1	1	20

Loop Filter Components[2]



R5 = 350Ω
C3 = 1.0µF (X7R Dielectric)

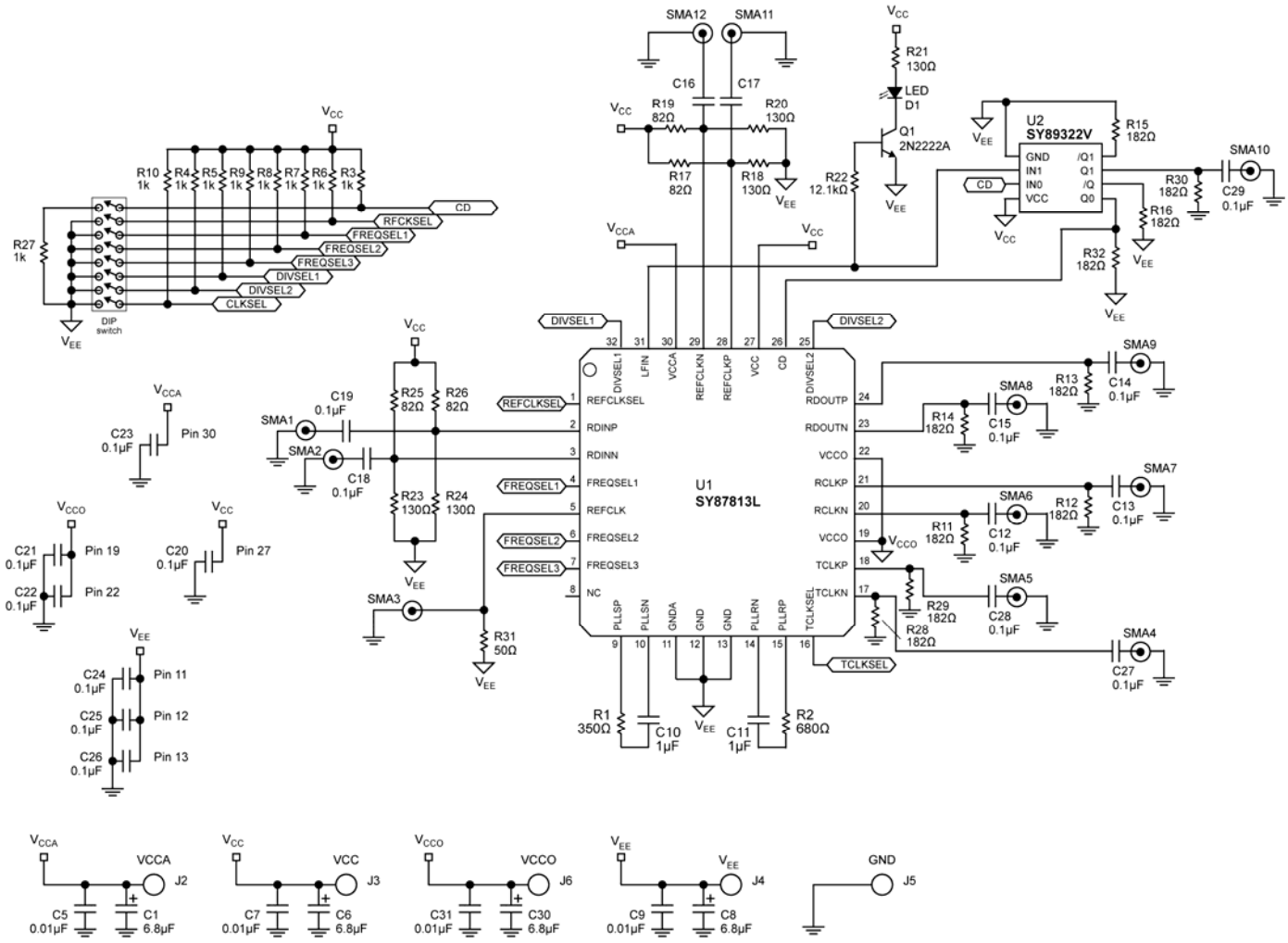


R6 = 680Ω
C4 = 1.0µF (X7R Dielectric)

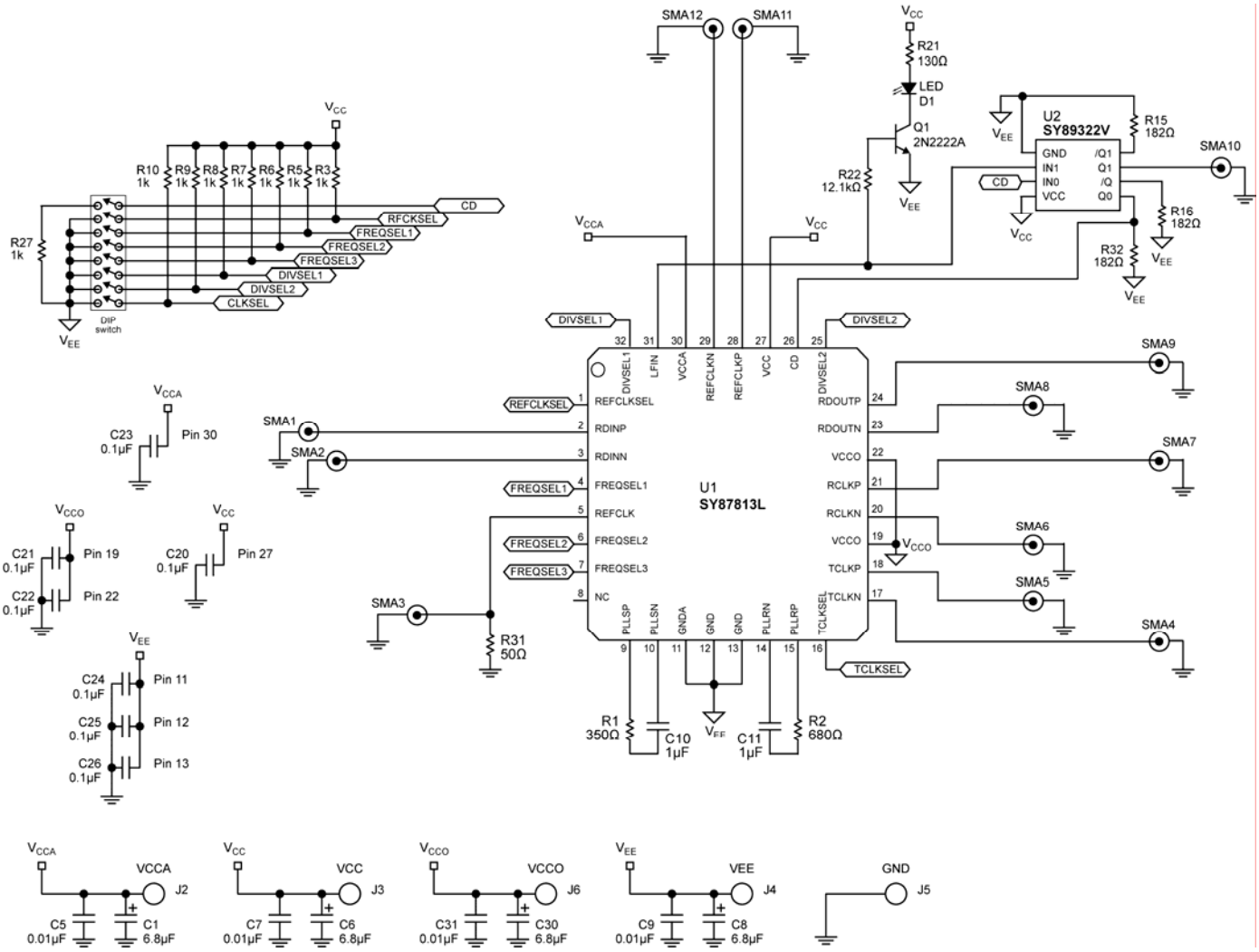
Note:

2. Suggested values. Values may vary for different applications.

Application Example AC-Coupled I/O



Application Example DC-Coupled I/O



Related Product and Support Documentation

Part Number	Function	Data Sheet Link
SY87701AL	3.3V, 28Mbps to 1.3Gbps AnyRate® Clock and Data Recovery	www.micrel.com/product-info/products/sy87701al.shtml
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

Bill of Materials (AC-Coupled)

Item	Part Number	Manufacturer	Description	Qty.
C6	293D685X0025B2T	Vishay[1]	6.8µF, 25V, Tantalum Capacitor, Size B	1
C7	VJ206Y103JXJAT	Vishay[1]	0.01µF Ceramic Capacitor, Size 1206, X7R Dielectric	1
C10, C11	VJ0603Y105JXJAT	Vishay[1]	1.0µF Ceramic Capacitor, Size 0603, X7R Dielectric	2
C12-C15, C18, C19, C27, C28	VJ0402Y104JXJAT	Vishay[1]	0.1µF Ceramic Capacitor, Size 0402, X7R Dielectric	8
C20-C26	VJ0402Y104JXJAT	Vishay[1]	0.01µF Ceramic Capacitor, Size 0402, X7R Dielectric	7
D1	P301-ND	Panasonic[2]	LED Diode, T-1 3/4, Red Clear	1
D2	P300-ND/P301-ND	Vishay[1]	T-1 3/4, Red LED	1
J2, J3, J4, J6	111-0702-001	Johnson Components[3]	Red, Insulated Thumb Nut Binding Post (Jumped Together)	4
J5	BLM21A102F	Murata[4]	Black, Insulated Thumb Nut Binding Post, GND (Jumped to V_{EE})	1
Q1	459-2598-5-ND	NTE[5]	2N2222A Buffer/Driver Transistor, NPN	1
R1	CRCW04023500F	Vishay[1]	350Ω Resistor, 2%, Size 0402	1
R2	CRCW04026800F	Vishay[1]	680Ω Resistor, 2%, Size 0402	1
R3–R10	CRCW04021001F	Vishay[1]	1kΩ Pull-up Resistor, 2%, Size 0402	8
R11-R16, R28-R30, R32	CRCW04021820F	Vishay[1]	182Ω Resistor, 2%, Size 0402	10
R21	CRCW06031300F	Vishay[1]	130Ω Resistor, 2%, Size 0603	1
R22	CRCW04021820F	Vishay[1]	12.1kΩ Resistor, 2%, Size 0402	1
R23, R24	CRCW04021300F	Vishay[1]	130Ω Resistor, 2%, Size 0402	2
R25, R26	CRCW04022825F	Vishay[1]	82Ω Resistor, 2%, Size 0402	2
R27	CRCW0402OOR0F	Vishay[1]	0Ω Resistor, 2%, Size 0402	1
R31	CRCW04025000F	Vishay[1]	50Ω Resistor, 2%, Size 0402	1
SMA1-SMA10	142-0701-851	Johnson Components[3]	End Launch SMA Jack	10
SP1-SP6			Solder Jump Option	6
SW1	CT2068-ND	CTS[6]	8-Position, Top Actuated Slide Dip Switch	1
U1	**SY87813L**	**Micrel, Inc.**[7]	**Low-Power 3.3V 28Mbps to 1300Mbps AnyRate® Clock and Data Recovery**	1
U2	**SY89322V**	**Micrel, Inc.**[7]	**3.3/5V Dual LVTTL/LVCMOS-to-Differential LVPECL Translator**	1

Notes:

1. Vishay: www.vishay.com.
2. Panasonic: www.panasonic.com.
3. Johnson Components: www.johnson-components.com.
4. Murata: www.murata.com.
5. NTE: www.nte.com.
6. CTS: www.cts.com.
7. **Micrel, Inc: www.micrel.com.**

Bill of Materials (DC-Coupled)

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C6	293D685X0025B2T	Vishay[1]	6.8µF, 25V, Tantalum Capacitor, Size B	1
C7	VJ206Y103JXJAT	Vishay[1]	0.01µF Ceramic Capacitor, Size 1206, X7R Dielectric	1
C10, C11	VJ0603Y105JXJAT	Vishay[1]	1.0µF Ceramic Capacitor, Size 0603, X7R Dielectric	2
C12-C15, C18, C19, C27, C28, C29	VJ0402Y104JXJAT	Vishay[1]	0.1µF Ceramic Capacitor, Size 0402, X7R Dielectric	8
C20-C26	VJ0402Y104JXJAT	Vishay[1]	0.01µF Ceramic Capacitor, Size 0402, X7R Dielectric	7
D1	P301-ND	Panasonic[2]	LED Diode, T-1 3/4, Red Clear	1
D2	P300-ND/P301-ND	Vishay[1]	T-1 3/4, Red LED	1
J2, J3, J4, J6	111-0702-001	Johnson Components[3]	Red, Insulated Thumb Nut Binding Post (Jumped Together)	4
J5	BLM21A102F	Johnson Components[3]	Black, Insulated Thumb Nut Binding Post, GND (Jumped to V_{EE})	1
Q1	459-2598-5-ND	NTE[5]	2N2222A Buffer/Driver Transistor, NPN	1
R1	CRCW04023500F	Vishay[1]	350Ω Resistor, 2%, Size 0402	1
R2	CRCW04026800F	Vishay[1]	680Ω Resistor, 2%, Size 0402	1
R3–R10	CRCW04021001F	Vishay[1]	1kΩ Pull-up Resistor, 2%, Size 0402	8
R15, R16, R30, R32	CRCW04021820F	Vishay[1]	182Ω Resistor, 2%, Size 0402	10
R21	CRCW06031300F	Vishay[1]	130Ω Resistor, 2%, Size 0603	1
R22	CRCW04021820F	Vishay[1]	12.1kΩ Resistor, 2%, Size 0402	1
R23, R24	CRCW04022825F	Vishay[1]	82Ω Resistor, 2%, Size 0402	2
R27	CRCW0402OOR0F	Vishay[1]	0Ω Resistor, 2%, Size 0402	1
R31	CRCW04025000F	Vishay[1]	50Ω Resistor, 2%, Size 0402	1
SMA1-SMA10	142-0701-851	Johnson Components[3]	End Launch SMA Jack	10
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U2	**SY89322V**	**Micrel, Inc.**[7]	**3.3/5V Dual LVTTL/LVCMOS-to-Differential LVPECL Translator**	1

Notes:

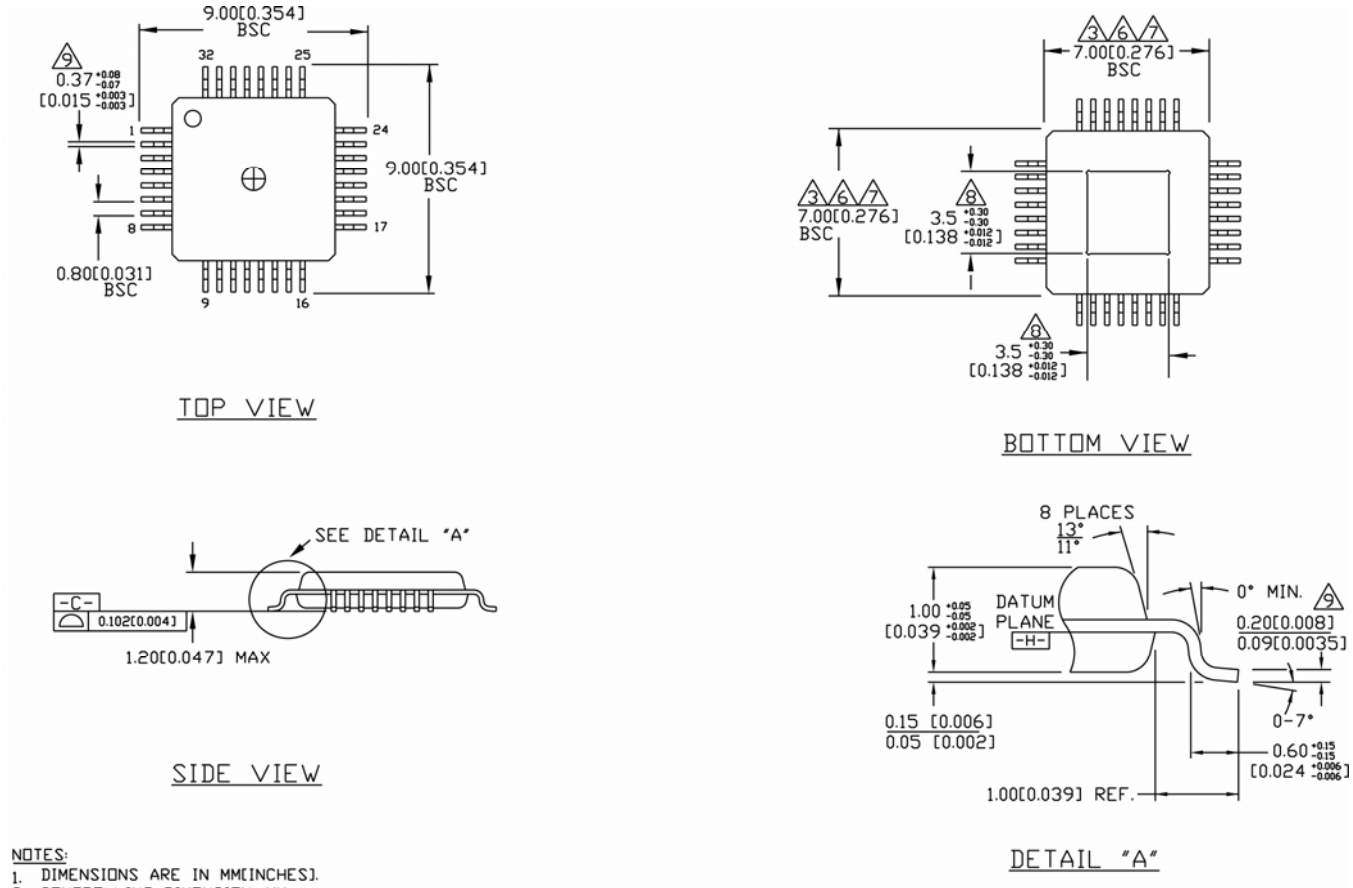
5. Vishay: www.vishay.com.
6. Panasonic: www.panasonic.com.
7. Johnson Components: www.johnson-components.com.
8. Murata: www.murata.com.
5. NTE: www.nte.com.
6. CTS: www.cts.com.
7. **Micrel, Inc: www.micrel.com.**

Appendix A

Layout and General Suggestions

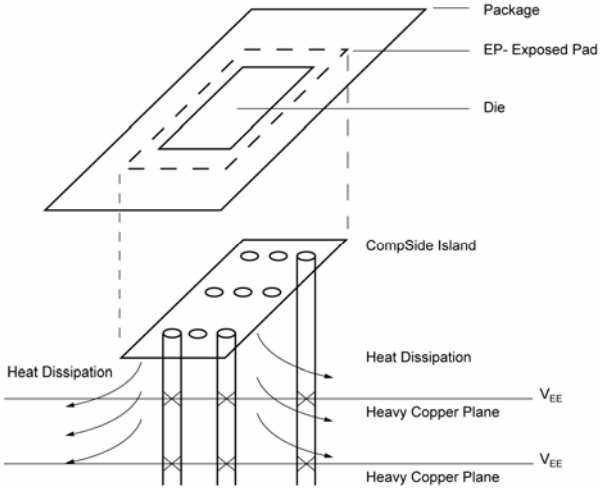
1. Establish controlled impedance stripline, microstrip, or coplanar construction techniques.
2. Signal paths should have approximately the same width as the device pads.
3. All differential paths are critical timing paths, where skew should be matched to within ±10ps.
4. Signal trace impedance should not vary more than ±5%. If in doubt, perform TDR analysis of all high-speed signal traces.
5. Maintain compact filter networks as close to filter pins as possible. Provide ground plane relief under filter path to reduce stray capacitance. Be careful of crosstalk coupling into the filter network.
6. Maintain low jitter on the REFCLK input. Isolate the XTAL oscillator from power supply noise by adequately decoupling. Keep XTAL oscillator close to device, and minimize capacitive coupling from adjacent signals.
7. Higher speed operation may require use of fundamental-tone (third-overtone typically has more jitter) crystal-based oscillator for optimum performance. Evaluate and compare candidates by measuring TXCLK jitter.
8. All unused outputs must be terminated. To conserve power, unused PECL outputs can be terminated with a 1kΩ resistor to V_{EE}.

Package Information



NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.254 [0.010].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN.
6. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H-
7. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.
8. EXPOSED PAD SHALL BE COPLANAR WITH PACKAGE BOTTOM WITHIN 0.05mm
   EXPOSED PAD: Cu WITH Sn/Pb PLATING
9. DIMENSION INCLUDES LEAD FINIS

32-Pin EPAD-TQFP (Die Up) (H32-1)



PCB Thermal Consideration for 32-Pin EPAD-TQFP

Package Notes:

1. Package meets Leve 2 moisture sensitivity classification and is shipped in dry-pack form.
2. Exposed pad must be soldered to a ground for proper thermal management.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http:/www.micrel.com

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