



3.3V Phase-Lock Loop Clock Driver

General Description

The **ICSVF2510** is a high performance, low skew, low jitter clock driver. It uses a phase lock loop (PLL) technology to align, in both phase and frequency, the CLKIN signal with the CLKOUT signal. It is specifically designed for use with synchronous SDRAMs. The **ICSVF2510** operates at 3.3V VCC and drives up to ten clock loads.

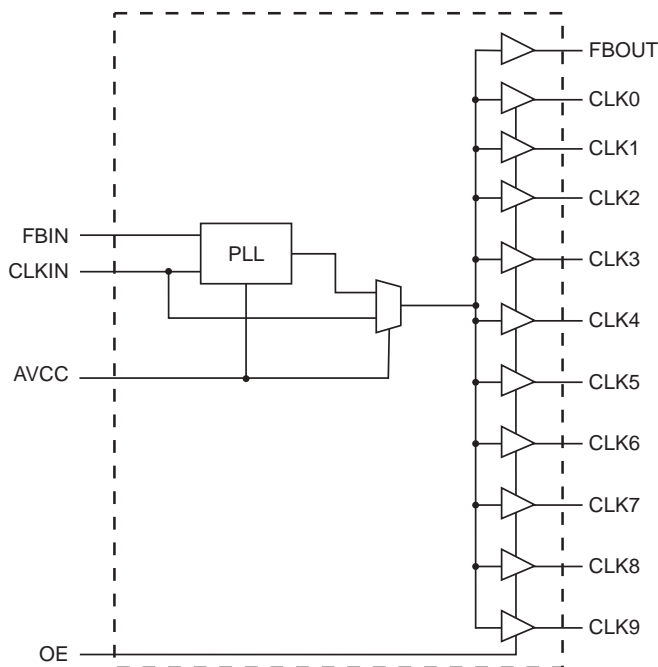
One bank of ten outputs provide low-skew, low-jitter copies of CLKIN. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at CLKIN. Outputs can be enabled or disabled via control (OE) inputs. When the OE inputs are high, the outputs align in phase and frequency with CLKIN; when the OE inputs are low, the outputs are disabled to the logic low state.

The **ICSVF2510** does not require external RC filter components. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost. The test mode shuts off the PLL and connects the input directly to the output buffer. This test mode, the **ICSVF2510** can be use as low skew fanout clock buffer device. The **ICSVF2510** comes in 24 pin 173mil Thin Shrink Small-Outline package (TSSOP) package.

Features

- Meets or exceeds PC133 registered DIMM specification 1.1
- Spread Spectrum Clock Compatible
- Distributes one clock input to one bank of ten outputs
- Operating frequency 20MHz to 200MHz
- External feedback input (FBIN) terminal is used to synchronize the outputs to the clock input
- No external RC network required
- Operates at 3.3V Vcc
- Plastic 24-pin 173mil TSSOP package

Block Diagram



Pin Configuration

| | | | |
|-------|----|----|-------|
| AGND | 1 | 24 | CLKIN |
| VCC | 2 | 23 | AVCC |
| CLK0 | 3 | 22 | VCC |
| CLK1 | 4 | 21 | CLK9 |
| CLK2 | 5 | 20 | CLK8 |
| GND | 6 | 19 | GND |
| GND | 7 | 18 | GND |
| CLK3 | 8 | 17 | CLK7 |
| CLK4 | 9 | 16 | CLK6 |
| VCC | 10 | 15 | CLK5 |
| OE | 11 | 14 | VCC |
| FBOUT | 12 | 13 | FBIN |

24 Pin TSSOP

4.40 mm. Body, 0.65 mm. Pitch



Pin Descriptions

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|--------------|-----------------|------|---|
| 1 | AGND | PWR | Analog Ground |
| 2, 10, 14 | VCC | PWR | Power Supply (3.3V) |
| 3 | CLK0 | OUT | Buffered clock output. |
| 4 | CLK1 | OUT | Buffered clock output. |
| 5 | CLK2 | OUT | Buffered clock output. |
| 6, 7, 18, 19 | GND | PWR | Ground |
| 8 | CLK3 | OUT | Buffered clock output. |
| 9 | CLK4 | OUT | Buffered clock output. |
| 11 | OE ¹ | IN | Output enable (has internal pull_up). When high, normal operation. When low, clock outputs are disabled to a logic low state. |
| 12 | FBOUT | OUT | Feedback output |
| 13 | FBIN | IN | Feedback input |
| 15 | CLK5 | OUT | Buffered clock output. |
| 16 | CLK6 | OUT | Buffered clock output. |
| 17 | CLK7 | OUT | Buffered clock output. |
| 20 | CLK8 | OUT | Buffered clock output. |
| 21 | CLK9 | OUT | Buffered clock output. |
| 22 | VCC | PWR | Power Supply (3.3V) digital supply. |
| 23 | AVCC | IN | Analog power supply (3.3V). When input is ground PLL is off and bypassed. |
| 24 | CLKIN | IN | Clock input |

Note:

1. Weak pull-ups on these inputs

Functionality

| INPUTS | | OUTPUTS | | | PLL Shutdown |
|-------------|------|-----------|--------|--------|--------------|
| OE | AVCC | CLK (9:0) | FBOUT | Source | |
| 0 | 3.33 | 0 | Driven | PLL | N |
| 1 | 3.33 | Driven | Driven | PLL | N |
| Buffer Mode | | | | | |
| 0 | 0 | 0 | Driven | CLKIN | Y |
| 1 | 0 | Driven | Driven | CLKIN | Y |

Test mode:

When AVCC is 0, shuts off the PLL and connects the input directly to the output buffers



Absolute Maximum Ratings

- Supply Voltage (AVCC) AVCC < (V_{CC} + 0.7 V)
- Supply Voltage (VCC) 4.3 V
- Logic Inputs GND –0.5 V to V_{CC} + 0.5 V
- Ambient Operating Temperature 0°C to +70°C
- Storage Temperature –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - OUTPUT

T_A = 0 - 70°C; V_{DD} = V_{DDL} = 3.3 V +/-10%; C_L = 30 pF; R_L = 500 Ohms (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------------------|-------------------------------------|--|-----|------|-----|-------|
| Output High Voltage | V _{OH} | I _{OH} = -8 mA | 2.4 | 2.9 | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 8 mA | | 0.25 | 0.4 | V |
| Output High Current | I _{OH} | V _{OH} = 2.4 V | | 27 | | mA |
| | | V _{OH} = 2.0 V | | 39 | | |
| Output Low Current | I _{OL} | V _{OL} = 0.8 V | | 26 | | mA |
| | | V _{OL} = 0.55 V | | 19 | | |
| Rise Time ¹ | T _r | V _{OL} = 0.8 V, V _{OH} = 2.0 V | 0.5 | 1.1 | 2.1 | ns |
| Fall Time ¹ | T _f | V _{OH} = 2.0 V, V _{OL} = 0.8 V | 0.5 | 1.1 | 2.7 | ns |
| Duty Cycle ¹ | D _t | V _T = 1.5 V; C _L =30 pF | 48 | 50 | 52 | % |
| Cycle to Cycle jitter ¹ | T _{CYC} - T _{CYC} | at 66-100 MHz ; loaded outputs | | | 75 | ps |
| Absolute Jitter ¹ | T _{JABS} | 10000 cycles; C _L = 30 pF | | | 100 | ps |
| Skew ¹ | T _{sk} | V _T = 1.5 V (Window) Output to Output | | | 100 | ps |
| Phase error ¹ | T _{pe} | V _T = V _{dd} /2; CLKIN-FBIN | -75 | | 75 | ps |
| Delay Input-Output ¹ | D _{R1} | V _T = 1.5 V; PLL_EN = 0 | | 3.3 | 3.7 | ns |

¹ Guaranteed by design, not 100% tested in production.



Electrical Characteristics - Input & Supply

$T_A = 0 - 70^\circ\text{C}$; Supply Voltage $V_{DD} = 3.3\text{ V} \pm 10\%$ (unless otherwise stated)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------|------------|---|----------------|-----|----------------|---------------|
| Input High Voltage | V_{IH} | | 2 | | $V_{DD} + 0.3$ | V |
| Input Low Voltage | V_{IL} | | $V_{SS} - 0.3$ | | 0.8 | V |
| Input High Current | I_{IH} | $V_{IN} = V_{DD}$ | | 0.1 | 100 | μA |
| Input Low Current | I_{IL} | $V_{IN} = 0\text{ V}$; | | 19 | 50 | μA |
| Operating current | I_{DD}^1 | $C_L = 0\text{ pF}$; $F_{IN} @ 66\text{MHz}$ | | | 170 | mA |
| Input Capacitance | C_{IN}^1 | Logic Inputs | | 4 | | pF |

¹Guaranteed by design, not 100% tested in production.

Timing requirements over recommended ranges of supply voltage and operating free-air temperature

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|-----------|----------------------------------|-----------------|------|------|---------------|
| F_{OP} | Operating frequency | | 20 | 200 | MHz |
| F_{CLK} | Input clock frequency | | 25 | 200 | MHz |
| | Input clock frequency duty cycle | | 40 | 60 | % |
| | Stabilization time | After power up | | 15 | μs |

Note: Time required for the PLL circuit to obtain phase lock of its feedback signal to its reference signal.

In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK.

Until phase lock is obtained, the specifications for parameters given in the switching characteristics table are not applicable.



PARAMETER MEASUREMENT INFORMATION

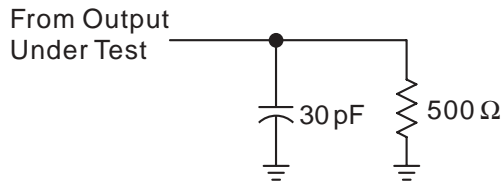


Figure 1. Load Circuit for Outputs

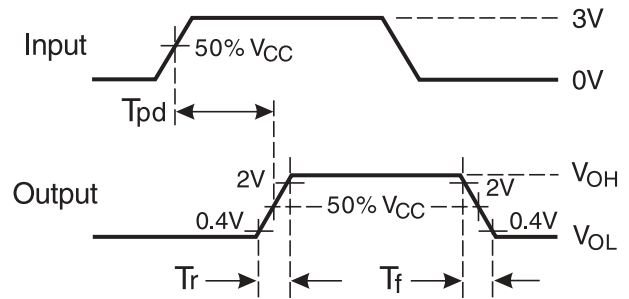


Figure 2. Voltage Waveforms Propagation Delay Times

Notes:

1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: $PRR \leq 133\text{MHz}$, $Z_O = 50\ \Omega$, $T_r \leq 1.2\text{ns}$, $T_f \leq 1.2\text{ns}$.
3. The outputs are measured one at a time with one transition per measurement.

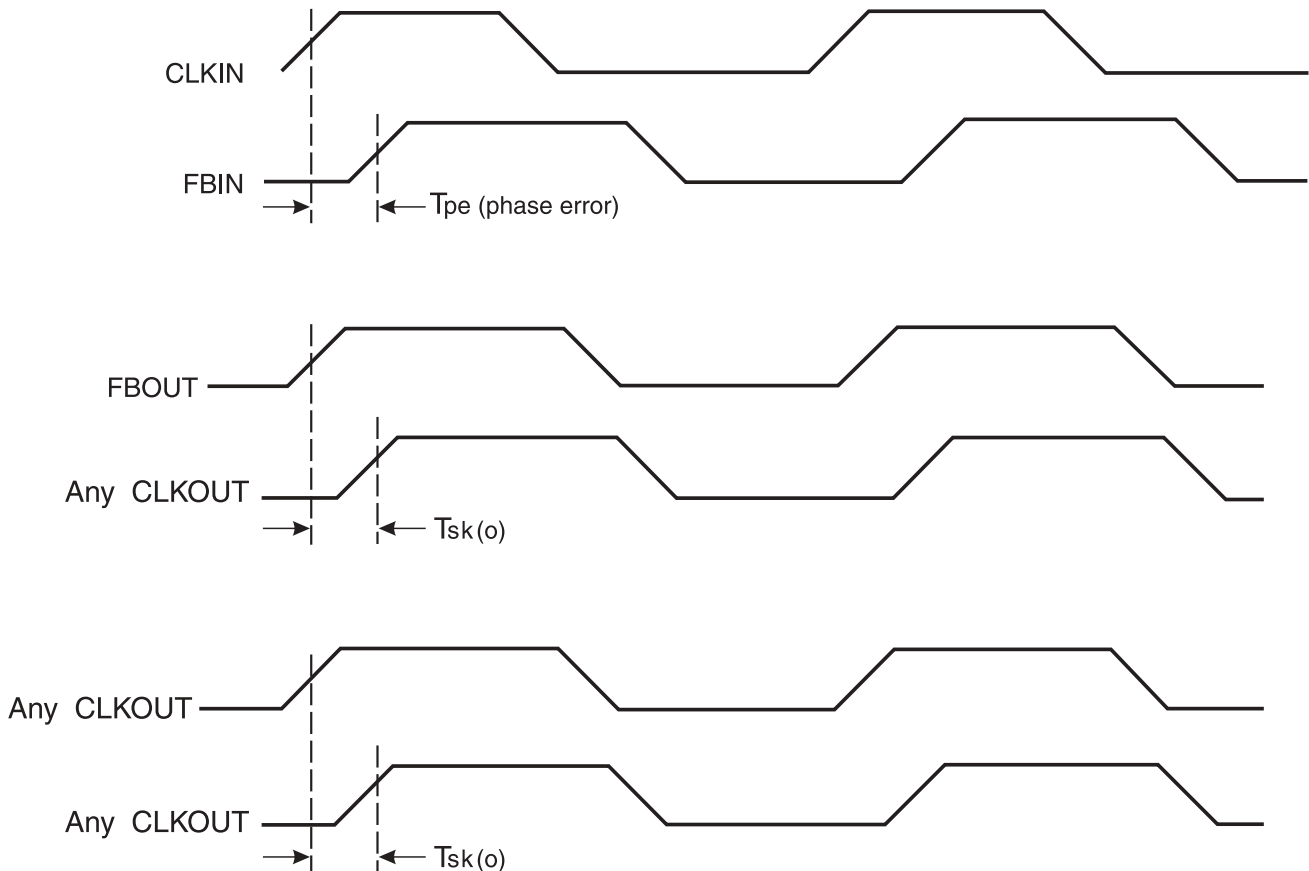


Figure 3. Phase Error and Skew Calculations



General Layout Precautions:

An ICS2509C is used as an example. It is similar to the ICSVF2510. The same rules and methods apply.

- 1) Use copper flooded ground on the top signal layer under the clock buffer. The area under U1 in figure 1 on the right is an example. Every ground pin goes to a ground via. The vias are not visible in figure 1.
- 2) Use power vias for power and ground. Vias 20 mil or larger in diameter have lower high frequency impedance. Vias for signals may be minimum drill size.
- 3) Make all power and ground traces are as wide as the via pad for lower inductance.
- 4) VAA for pin 23 has a low pass RC filter to decouple the digital and analog supplies. C9-12 may be replaced with a single low ESR (0.8 ohm or less) device with the same total capacitance. R2 may be replaced with a ferrite bead. The bead should have a DC resistance of at least 0.5 ohms. 1 ohm is better. It should have an impedance of at least 300 ohms at 100MHz. 600 ohms at 100MHz is better.
- 5) Notice that ground vias are never shared.
- 6) All VCC pins have a decoupling capacitor. Power is always routed from the plane connection via to the capacitor pad to the VCC pin on the clock buffer.
- 7) Component R1 is located at the clock source.
- 8) Component C1, if used, has the effect of adding delay.
- 9) Component C7, if used, has the effect of subtracting delay. Delaying the FBIn clock will cause the output clocks to be earlier. A more effective method is to use the propagation time of a trace between FBOut and FBIn.

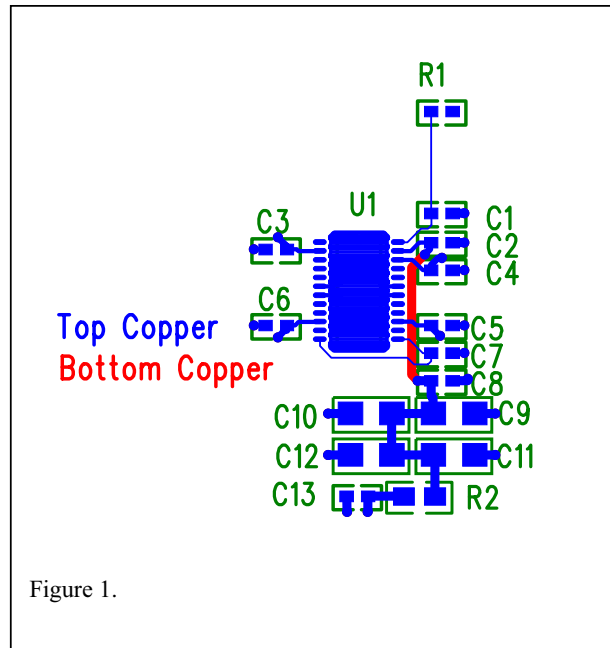
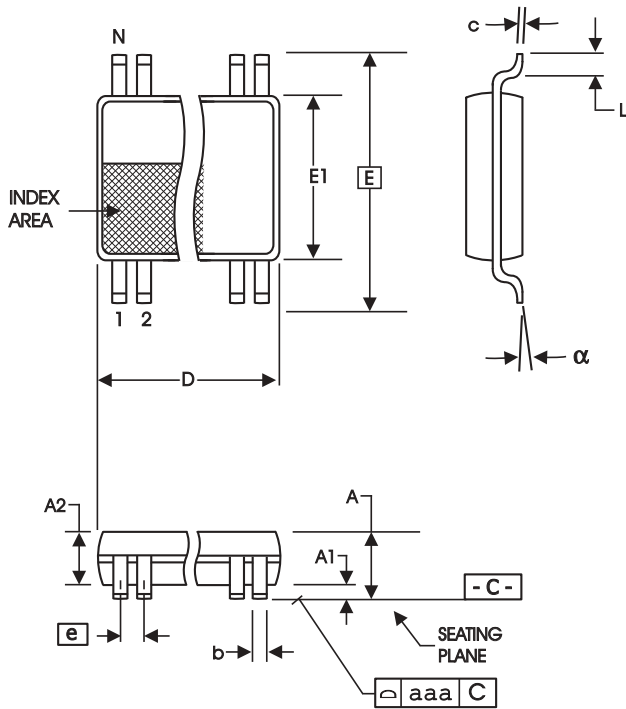


Figure 1.

Component Values:

C1, C7= As necessary for delay adjust
 C[6:2] = .01uF
 C8, C13 = 0.1uF
 C[12:9] = 4.7uF
 R1 = 10 ohm. Locate at driver
 R2 = 10 ohm.



| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|--------|-------------------------------------|------|--------------------------------|------|
| | MIN | MAX | MIN | MAX |
| A | -- | 1.20 | -- | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.19 | 0.30 | .007 | .012 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 6.40 BASIC | | 0.252 BASIC | |
| E1 | 4.30 | 4.50 | .169 | .177 |
| e | 0.65 BASIC | | 0.0256 BASIC | |
| L | 0.45 | 0.75 | .018 | .030 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | .004 |

VARIATIONS

| N | D mm. | | D (inch) | |
|----|-------|------|----------|------|
| | MIN | MAX | MIN | MAX |
| 24 | 7.70 | 7.90 | .303 | .311 |

Reference Doc.: JEDEC Publication 95, MO-153
10-0035

4.40 mm. Body, 0.65 mm. pitch TSSOP
(173 mil) (0.0256 Inch)

Ordering Information

ICSVF2510yG-T

Example:

ICS XXXX y G - PPP - T

