

# Advanced Regulating Pulse Width Modulators

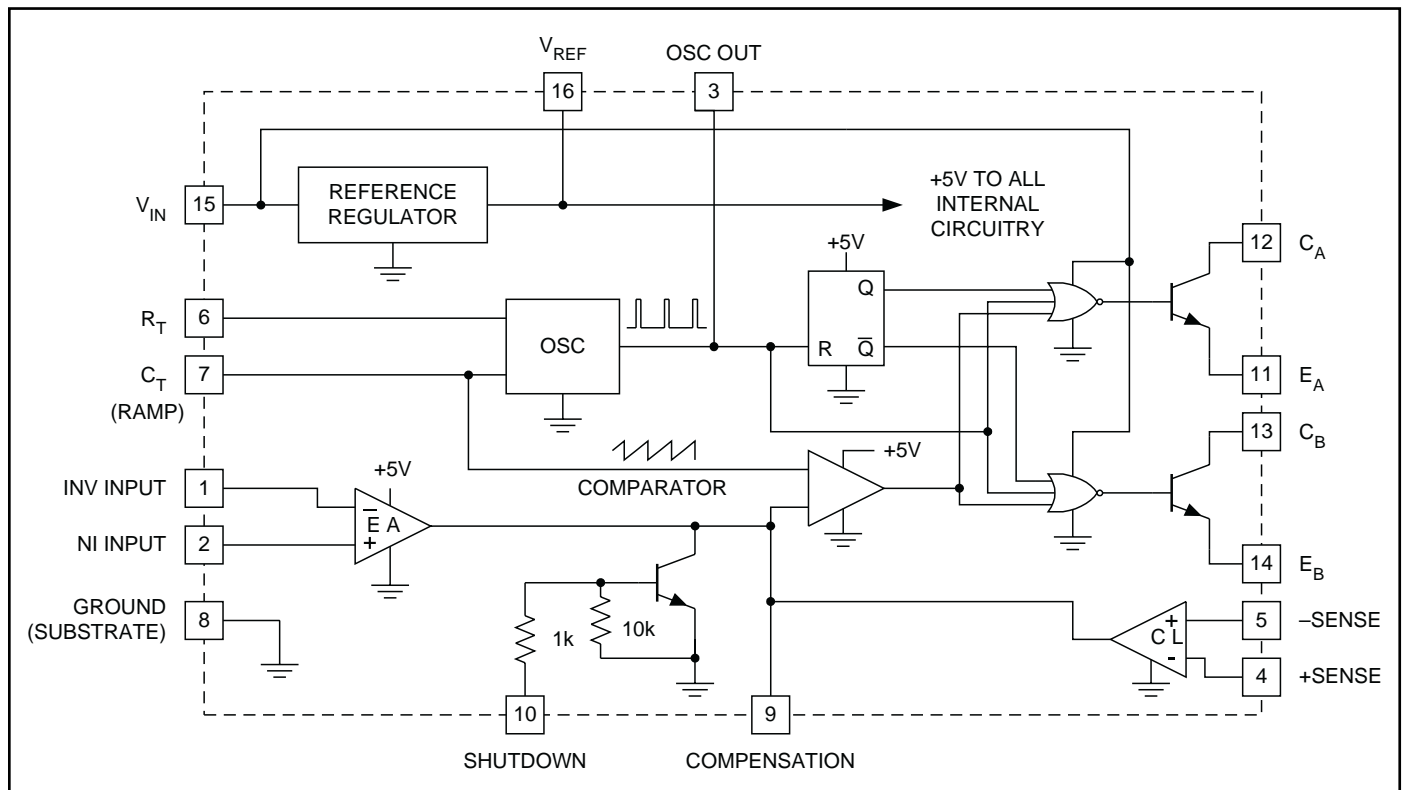
## FEATURES

- Complete PWM Power Control Circuitry
- Uncommitted Outputs for Single-ended or Push-pull Applications
- Low Standby Current...8mA Typical
- Interchangeable with SG1524, SG2524 and SG3524, Respectively

## DESCRIPTION

The UC1524, UC2524 and UC3524 incorporate on a single monolithic chip all the functions required for the construction of regulating power supplies, inverters or switching regulators. They can also be used as the control element for high-power-output applications. The UC1524 family was designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allow either single-ended or push-pull applications. Each device includes an on-chip reference, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shut-down circuitry. The UC1524 is characterized for operation over the full military temperature range of -55°C to +125°C. The UC2524 and UC3524 are designed for operation from -25°C to +85°C and 0° to +70°C, respectively.

## BLOCK DIAGRAM





**ELECTRICAL CHARACTERISTICS:** Unless otherwise stated, these specifications apply for  $T_A = -55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  for the UC1524,  $-25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  for the UC2524, and  $0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  for the UC3524,  $V_{IN} = 20\text{V}$ , and  $f = 20\text{kHz}$ ,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	UC1524/UC2524			UC3524			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>Error Amplifier Section (cont.)</b>								
Common Mode Rejection Ratio	$T_J = 25^{\circ}\text{C}$		70			70		dB
Small Signal Bandwidth	$A_v = 0\text{dB}$ , $T_J = 25^{\circ}\text{C}$		3			3		MHz
Output Voltage	$T_J = 25^{\circ}\text{C}$	0.5		3.8	0.5		3.8	V
<b>Comparator Section</b>								
Duty-Cycle	% Each Output On	0		45	0		45	%
Input Threshold	Zero Duty-Cycle		1			1		V
	Maximum Duty-Cycle		3.5			3.5		V
Input Bias Current			1			1		$\mu\text{A}$
<b>Current Limiting Section</b>								
Sense Voltage	Pin 9 = 2V with Error Amplifier Set for Maximum Out, $T_J = 25^{\circ}\text{C}$	190	200	210	180	200	220	mV
Sense Voltage T.C.			0.2			0.2		$\text{mV}/^{\circ}\text{C}$
Common Mode Voltage		-1		+1	-1		+1	V
<b>Output Section (Each Output)</b>								
Collector-Emitter Voltage		40			40			V
Collector Leakage Current	$V_{CE} = 40\text{V}$		0.1	50		0.1	50	$\mu\text{A}$
Saturation Voltage	$I_C = 50\text{mA}$		1	2		1	2	V
Emitter Output Voltage	$V_{IN} = 20\text{V}$	17	18		17	18		V
Rise Time	$R_C = 2\text{k}\Omega$ , $T_J = 25^{\circ}\text{C}$		0.2			0.2		$\mu\text{s}$
Fall Time	$R_C = 2\text{k}\Omega$ , $T_J = 25^{\circ}\text{C}$		0.1			0.1		$\mu\text{s}$
<b>Total Standby Current (Note)</b>	$V_{IN} = 40\text{V}$		8	10		8	10	mA

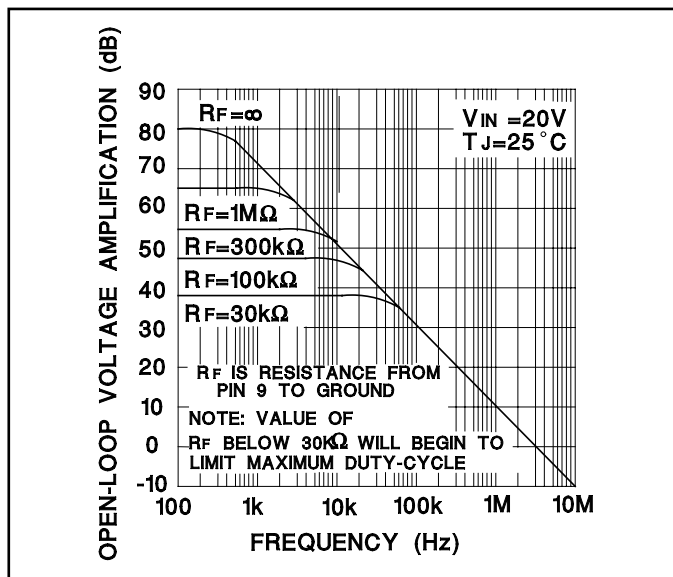
Note: Excluding oscillator charging current, error and current limit dividers, and with outputs open.

## PRINCIPLES OF OPERATION

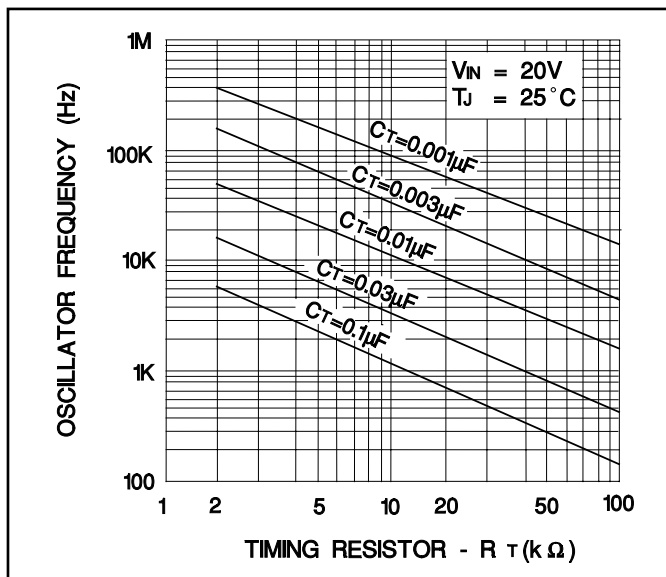
The UC1524 is a fixed-frequency pulse-width-modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor ( $R_T$ ), and one timing capacitor ( $C_T$ ),  $R_T$  establishes a constant charging current for  $C_T$ . This results in a linear voltage ramp at  $C_T$ , which is fed to the comparator providing linear control of the output pulse width by the error amplifier. The UC1524 contains an on-board 5V regulator that serves as a reference as well as powering the UC1524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generate a feedback signal to the error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at  $C_T$ . The resulting modulated pulse out of the high-gain comparator is then steered to

the appropriate output pass transistor ( $Q_1$  or  $Q_2$ ) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both outputs are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the value of  $C_T$ . The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current limiting and shutdown circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier or to provide additional control to the regulator.

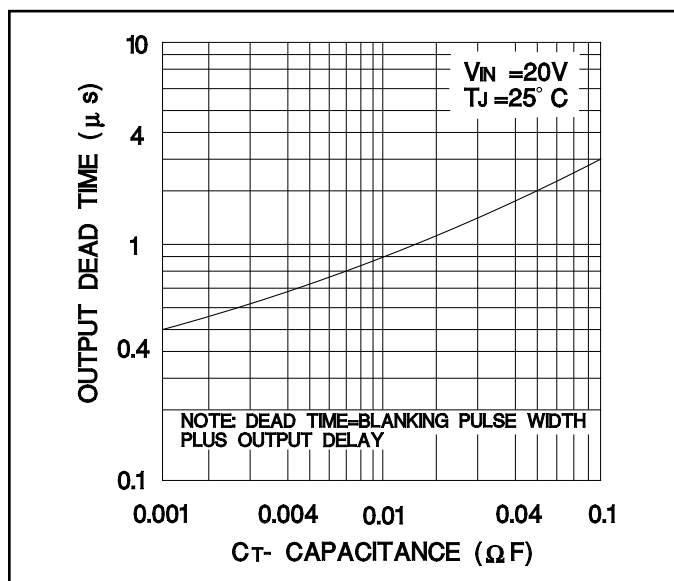
TYPICAL CHARACTERISTICS



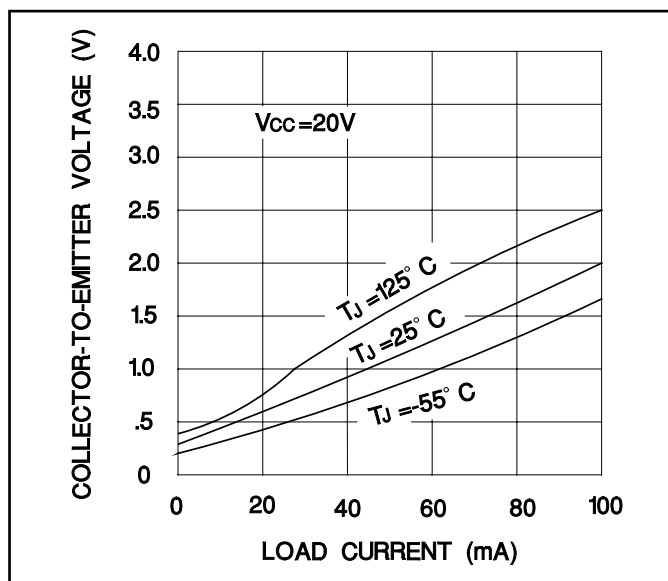
Open-loop voltage amplification of error amplifier vs frequency.



Oscillator frequency vs timing components.



Output dead time vs timing capacitance value.



Output saturation voltage vs load current.

## APPLICATION INFORMATION

### Oscillator

The oscillator controls the frequency of the UC1524 and is programmed by  $R_T$  and  $C_T$  according to the approximate formula:

$$f' \frac{1.18}{R_T C_T}$$

where  $R_T$  is in  $k\Omega$   
 $C_T$  is in  $mF$   
 $f$  is in  $kHz$

Practical values of  $C_T$  fall between 0.001mF and 0.1mF. Practical values of  $R_T$  fall between 1.8k $\Omega$  and 100k $\Omega$ . This results in a frequency range typically from 120Hz to 500kHz.

### Blanking

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse width is controlled by the value of  $C_T$ . If small values of  $C_T$  are required for frequency control, the oscillator output pulse width may still be increased by applying a shunt capacitance of up to 100pF from pin 3 to ground. If still greater dead-time is required, it should be accomplished by limiting the maximum duty cycle by clamping the output of the error amplifier. This can easily be done with the circuit in Figure 1:

### Synchronous Operation

When an external clock is desired, a clock pulse of approximately 3V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2k $\Omega$ . In this configuration  $R_T$   $C_T$  must be selected for a clock period slightly greater than that of the external clock.

If two or more UC1524 regulators are to operated synchronously, all oscillator output terminals should be tied together, all  $C_T$  terminals connected to single timing capacitor, and the timing resistor connected to a single  $R_T$  terminal. The other  $R_T$  terminals can be left open or shorted to  $V_{REF}$ . Minimum lead lengths should be used between the  $C_T$  terminals.

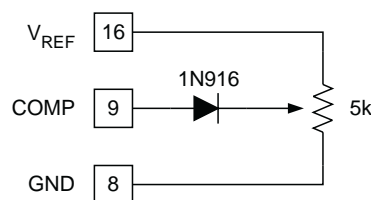


Figure 1. Error amplifier clamp.

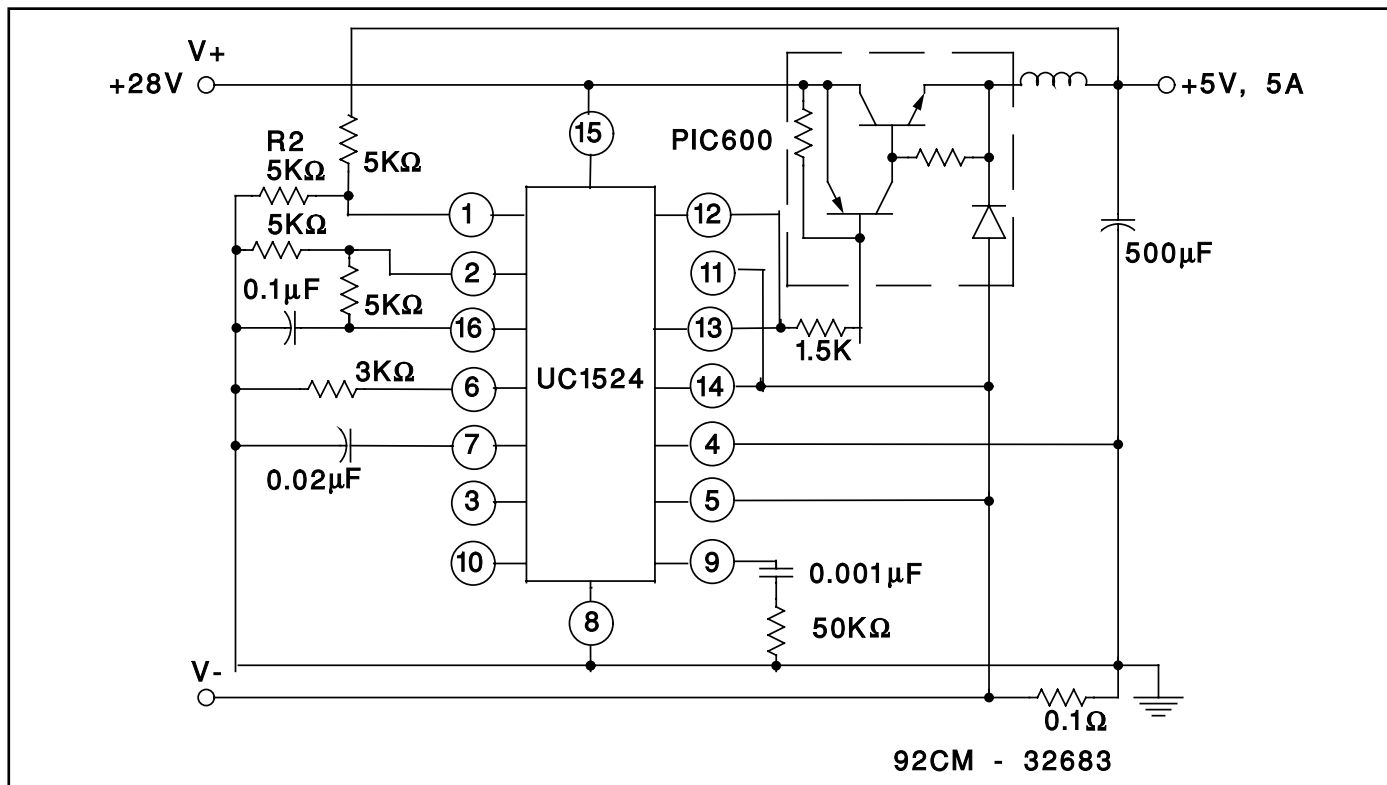


Figure 2. Single-ended LC switching regulator circuit.

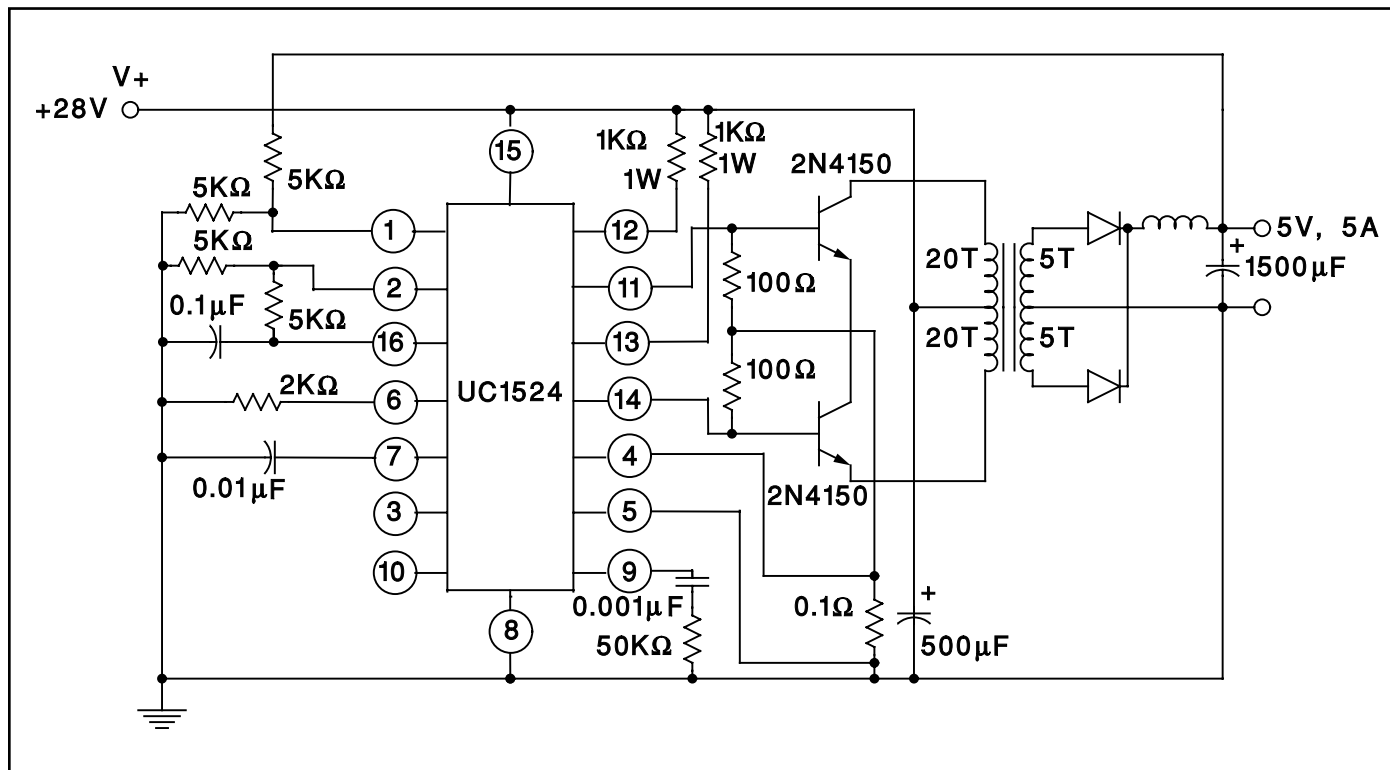


Figure 3. Push-pull transformer coupled circuit.

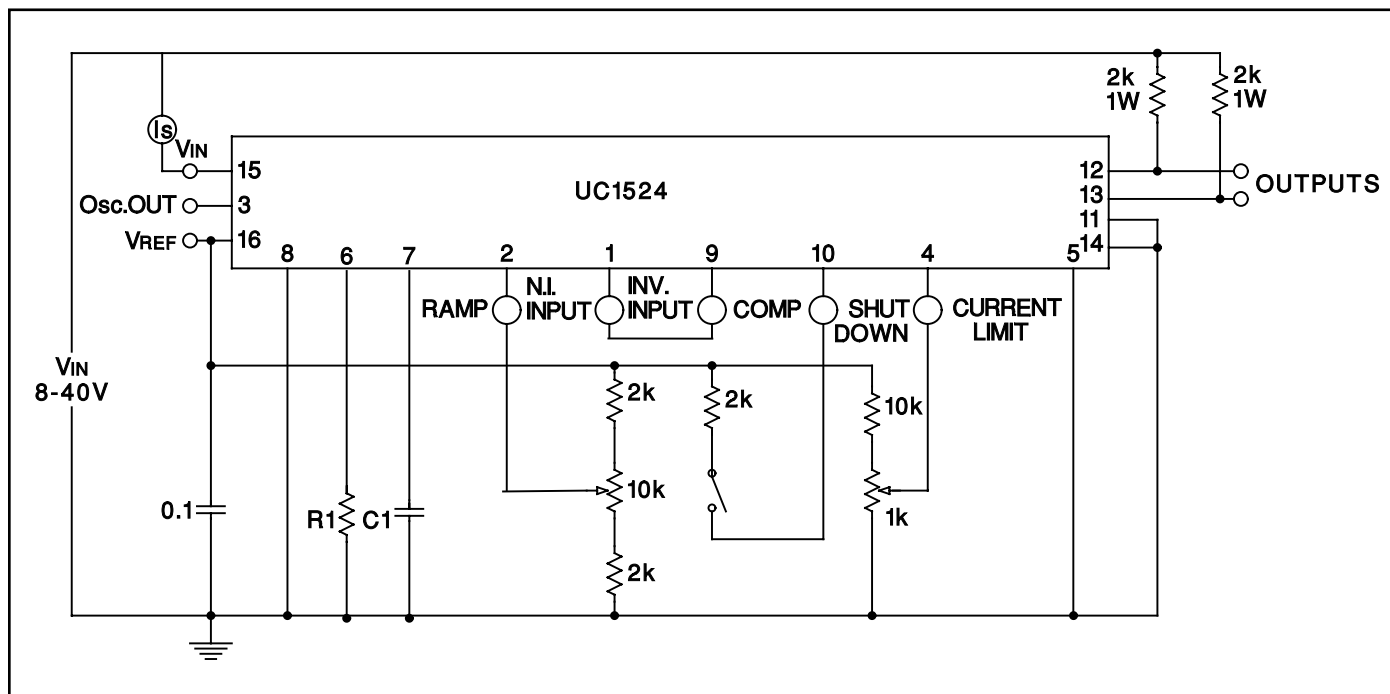


Figure 4. Open loop test circuit.

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## UC3524, ADVANCED REGULATING PULSE WIDTH MODULATORS

Device Status: Active

- > [Description](#)
- > [Features](#)
- > [Datasheets](#)
- > [Pricing/Samples/Availability](#)
- > [Application Notes](#)
- > [Applications](#)

Parameter Name	UC3524
Reference Voltage (V)	5
Shutdown	Yes
Pulse - by - Pulse Isense	No
Output Type	Dual Alternating, Uncommitted
Output Current (mA)	100
Frequency (max) (kHz)	300
Vref tol (%)	8
Duty Cycle (max) (%)	50
Shutdown Current (uA)	8000
Startup Current (uA)	8000
Operating Supply (max) (V)	40
Operating Supply (min) (V)	8
PWM Outputs (#)	2
Error Amplifier GBW (mHz)	3

### Description



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To view the following documents, [Acrobat Reader 3.x](#) is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

## Datasheets

Full datasheet in Acrobat PDF: [slus180b.pdf](#) (277 KB)

Full datasheet in Zipped PostScript: [slus180b.psz](#) (273 KB)

## Pricing/Samples/Availability

<u>Orderable Device</u>	<u>Package</u>	<u>Pins</u>	<u>Temp (°C)</u>	<u>Status</u>	<u>Price/unit USD (100-999)</u>	<u>Pack Qty</u>	<u>DSCC Number</u>	<u>Availability / Samples</u>
UC3524D	<u>D</u>	16	0 TO 70	ACTIVE	1.80	1		<a href="#">Check stock or order</a>
UC3524DTR	<u>D</u>	16	0 TO 70	ACTIVE	1.64	1		<a href="#">Check stock or order</a>
UC3524DW	<u>DW</u>	16	0 TO 70	ACTIVE	2.11	1		<a href="#">Check stock or order</a>
UC3524DWTR	<u>DW</u>	16		ACTIVE	1.90	1		<a href="#">Check stock or order</a>
UC3524J	<u>J</u>	16	0 TO 70	ACTIVE	4.76	1		<a href="#">Check stock or order</a>
UC3524N	<u>N</u>	16	0 TO 70	ACTIVE	1.72	1		<a href="#">Check stock or order</a>

## Application Reports

- [ELECTROSTATIC DISCHARGE APPLICATION NOTE \(SSYA008 - Updated: 05/05/1999\)](#)
- [THERMAL CHARACTERISTICS OF LINEAR AND LOGIC PACKAGES USING JEDEC PCB DESIGNS \(SZZA017A - Updated: 09/10/1999\)](#)

**Table Data Updated on: 8/11/2000**