A Product Line of
Diodes Incorporated

PI6C4911502D

High-Performance Differential Fanout Buffer

Features

- 2 LVPECL outputs with two individual dividers
- Up to 1.5GHz output frequency
- Low additive phase jitter:
  - Supports LVPECL, LVDS, CML, HCSL inputs
- Separate input output supply voltage for level shifting
- 2.5V/3.3V power supply
- Industrial temperature support
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.
  https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - 16-Pin, TQFN Package (ZH)

Description

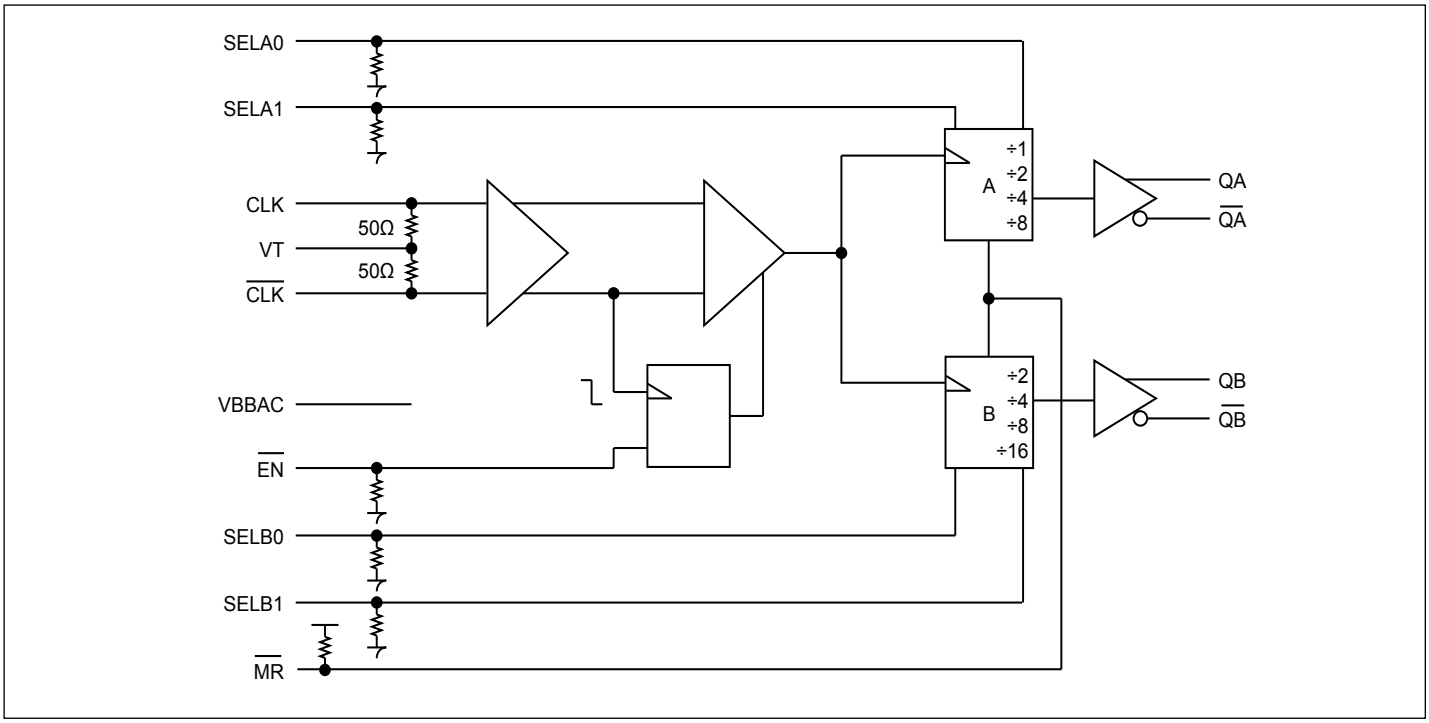
The PI6C4911502D is a high-performance fanout buffer device which supports up to 1.5GHz frequency. It also integrates two dividers with user-configurable output dividers on a per-output basis, which provides great flexibility to users. This device is ideal for systems that needs scale-down clock signals to multiple destinations.

Applications

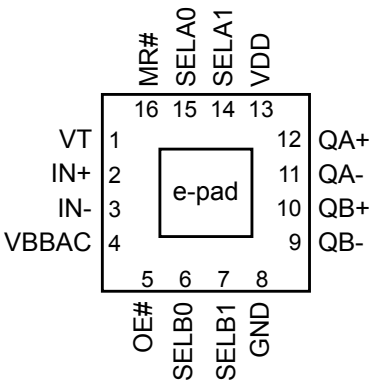
- Networking Systems, including Switches and Routers
- High-Frequency Backplane-Based Computing and Telecom Platforms

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Block Diagram



Pin Configuration



Pin Description

Pin #	Pin Name	Type	Description
1	VT		Internal 100Ω center-tapped termination pin for input clock
2, 3	IN+	Input	Differential input
	IN-		
4	VBBAC		Output reference for capacitor coupled inputs only
5	OE#	Input	Synchronous output enable, active low
6, 7	SELB0	Input	Bank B divider select pins
	SELB1		
8	GND	Power	Ground
9, 10	QB-	Output	Bank B LVPECL output pair
	QB+		
11, 12	QA-	Output	Bank A LVPECL output pair
	QA+		
13	V_{DD}	Power	Power supply pin
14, 15	SELA1	Input	Bank A divider select pins
	SELA0		
16	MR#	Input	Master reset
	EPAD	Power	Ground, must connect thermal vias (=> 4) to GND plane

Function Table

Table 1: Output Enable and Master Reset Function

IN	OE#	MR#	Output State
Rising edge	0	1	Output Enabled
Falling edge	1	1	Hold Output
X	X	0	Reset Output

Table 2: Output A Divide Function

SELA1	SELA0	QA Output
0	0	Divide by 1
0	1	Divide by 2
1	0	Divide by 4
1	1	Divide by 8

Table 3: Output B Divide Function

SELB1	SELB0	QB Output
0	0	Divide by 2
0	1	Divide by 4
1	0	Divide by 8
1	1	Divide by 16

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature..... -55°C to +150°C
Supply Voltage to Ground Potential (V_{DD}, V_{DDO}) -0.5V to +4.6V
Inputs (Referenced to GND) ..... -0.5V to V_{DD}+0.5V
Clock Output (Referenced to GND)..... -0.5V to V_{DD}+0.5V
Latch up 200mA
ESD Protection (Input) ..... 2000V min (HBM)
Junction Temperature ..... 125°C max

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Power Supply Characteristics and Operating Conditions

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{DD}	Core Supply Voltage		2.375		3.465	V
I_{DD}	Power Supply Current	Outputs unloaded		70		mA
T_A	Ambient Operating Temperature(1)		-40		85	°C
I_{BB}	Sink Source Current			±0.5		mA
V_{BBAC}	Output Voltage Reference @ 100µA V_{DD} = 3.3V V_{DD} = 2.5V			 1960 1160		mV

Note 1: Either T_A or T_B used as operating condition.

DC Electrical Specifications - Differential Inputs

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_{IH}	Input High Current	Input = V_{DD}			240	µA
I_{IL}	Input Low Current	Input = GND	-150			µA
C_{IN}	Input Capacitance			6		pF
V_{IH}	Input High Voltage				V_{DD}+0.3	V
V_{IL}	Input Low Voltage		-0.3			V
V_{ID}	Input Differential Amplitude PK-PK	Slew rate > 0.7V/ns for minimum input signal	0.15		1.3	V
V_{CM}	Common Model Input Voltage		0.25		V_{DD}-1.2	V

DC Electrical Specifications - LVCMOS Inputs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IH}	Input High Current	Input = V_{DD}			150	µA
I_{IL}	Input Low Current	Input = GND	-150			µA
V_{IH}	Input High Voltage	V_{DD}=3.3V	2.0		V_{DD}+0.3	V
V_{IL}	Input Low Voltage	V_{DD}=3.3V	-0.3		0.8	V
V_{IH}	Input High Voltage	V_{DD}=2.5V	1.7		V_{DD}+0.3	V
V_{IL}	Input Low Voltage	V_{DD}=2.5V	-0.3		0.7	V

DC Electrical Specifications - LVPECL Outputs

2.5V ± 5%

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	LVPECL test diagram	V_{DDO}-1.2		V_{DDO}-0.7	V
V_{OL}	Output Low Voltage	LVPECL test diagram	V_{DDO}-1.9		V_{DDO}-1.4	V

3.3V ± 5%

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage	LVPECL test diagram	V_{DDO}-1.2		V_{DDO}-0.7	V
V_{OL}	Output Low Voltage	LVPECL test diagram	V_{DDO}-2.0		V_{DDO}-1.4	V

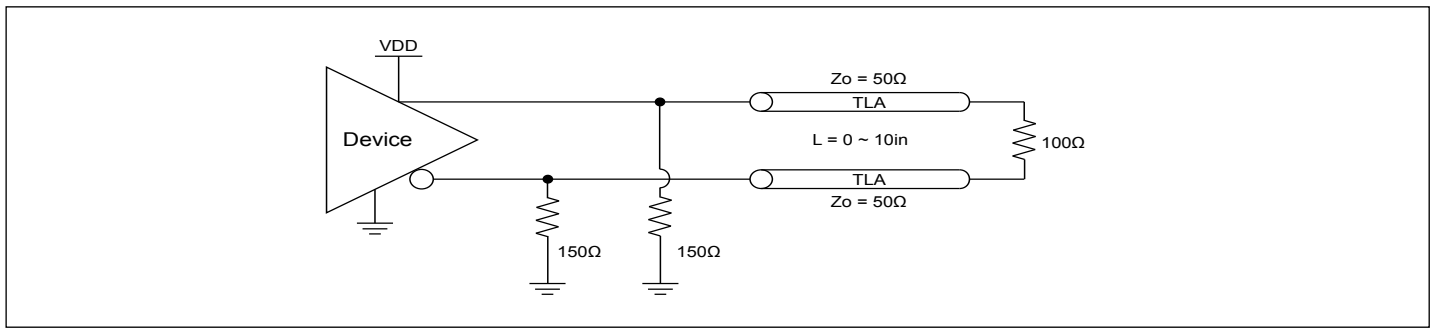
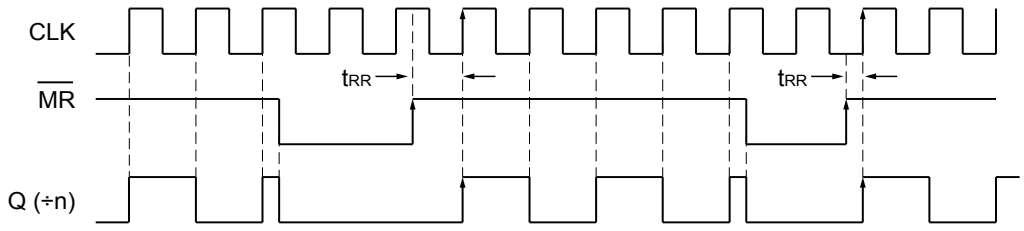


Figure 1: LVPECL Test Diagram

AC Electrical Specifications – Differential Outputs

Parameter	Description	Conditions		Min.	Typ.	Max.	Units
F_{OUT}	Clock Output Frequency	LVPECL				1500	MHz
T_r	Output Rise Time, 3.3V power supply @ 1GHz	From 20% to 80%	LVPECL	100	140	200	ps
	Output Rise Time, 2.5V power supply @ 1GHz			100	140	220	
T_f	Output Fall Time, 3.3V power supply @ 1GHz	From 80% to 20%	LVPECL	100	160	200	ps
	Output Fall Time, 2.5V power supply @ 1GHz			100	160	220	
T_{ODC}	Output Duty Cycle	Frequency <650MHz, $V_{ID} \geq 400mV$	LVPECL (<250MHz)	48		52	%
		Frequency <1GHz, $V_{ID} \geq 400mV$	LVPECL	45		55	
		Frequency <1.5GHz, $V_{ID} \geq 400mV$	LVPECL	40		60	
V_{PP}	Output Swing Single-Ended	LVPECL Outputs @ <1GHz		600		800	mV
		LVPECL Outputs @ >1GHz		400		700	
T_j	Buffer output jitter RMS	156.25MHz, 12kHz to 20MHz				1	ps
		156.25MHz, 10kHz to 1MHz				1	ps
T_{SK}	Output Skew				10	30	ps
T_{PD}	Propagation Delay	@ 3.3V, 100MHz			800		ps
T_{OD}	Valid to HiZ					80	ns
T_{OE}	Output Enable Time					2 input clock cycle	ns



Note: On the rising edge of $\overline{MR}$, Q goes HIGH after the first rising edge of CLK

Figure 2: Master Reset Timing Diagram

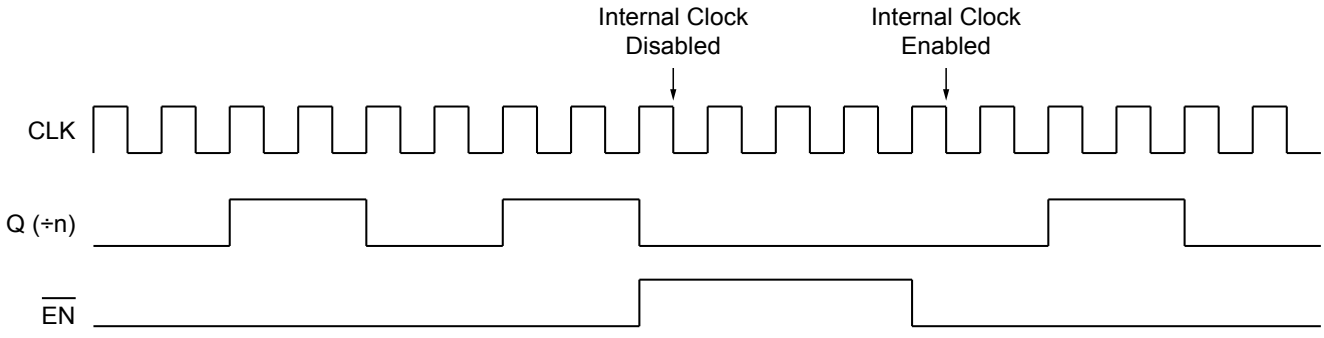


Figure 3: Output Enable Timing Diagram

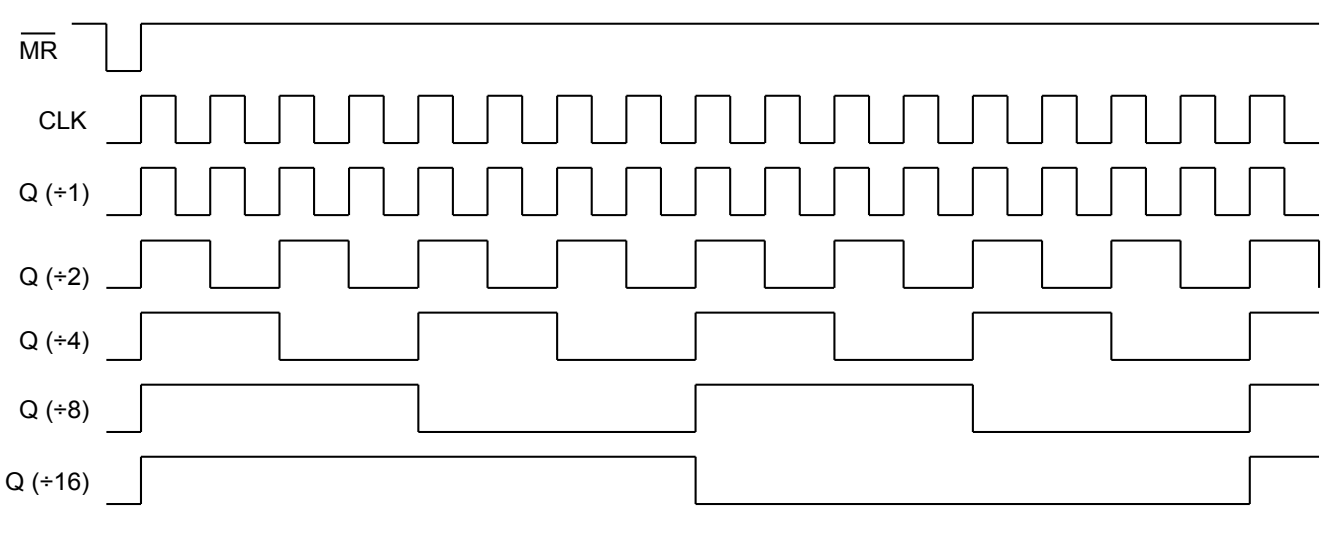
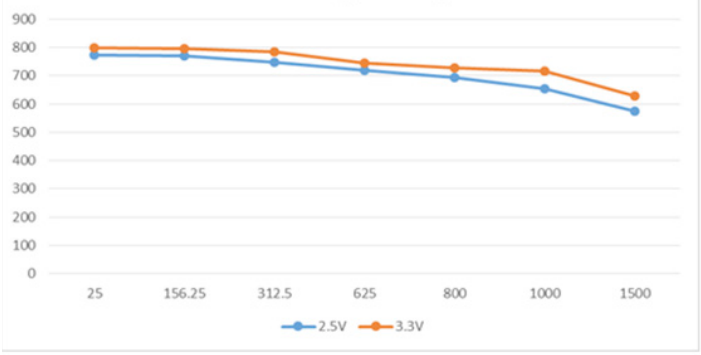
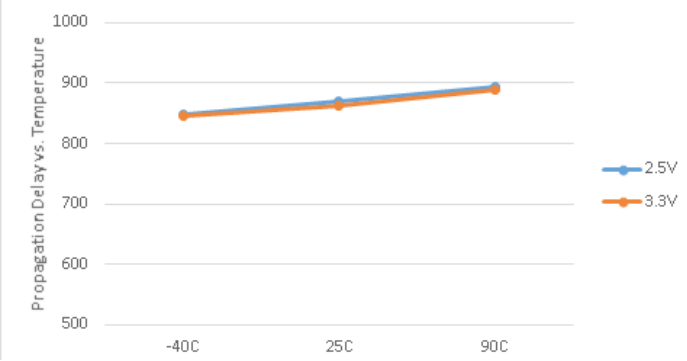


Figure 4: Timing Diagram

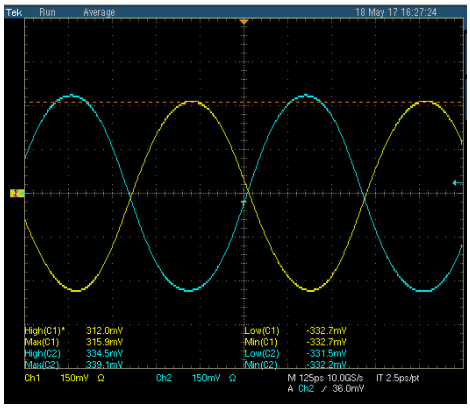
LVPECL Output Swing vs Frequency



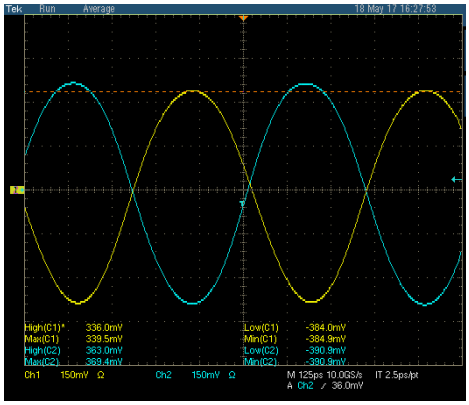
Propagation Delay vs Temperature



1.5GHz LVPECL Waveform



2.5V LVPECL Waveform

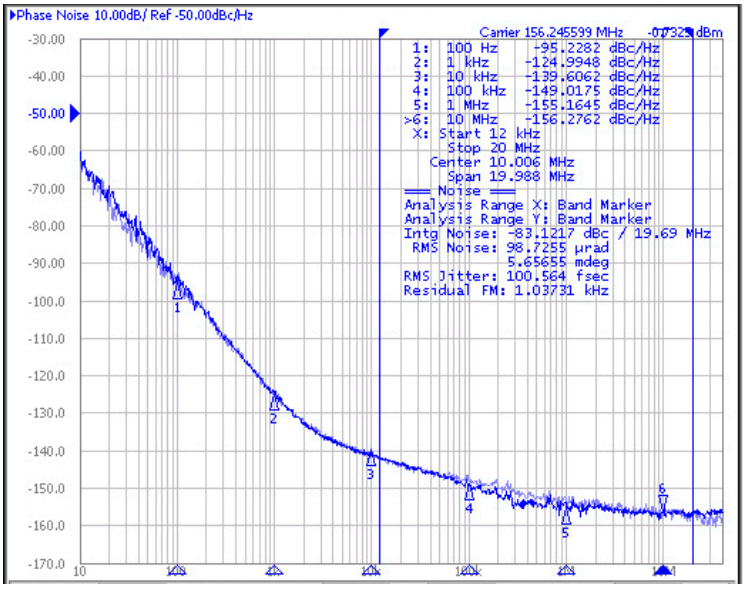


3.3V LVPECL Waveform

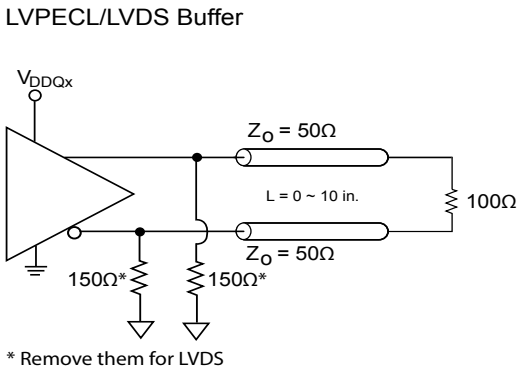
Phase Noise and Additive Jitter

Output Phase Noise (Dark Blue) vs Input Phase Noise (Light Blue)

Additive jitter is calculated at 156.25MHz ~ 27fs RMS (12kHz to 20MHz). Additive jitter = $\sqrt{(\text{Output jitter}^2 - \text{Input jitter}^2)}$.



Configuration Test Load Board Termination for LVPECL Outputs

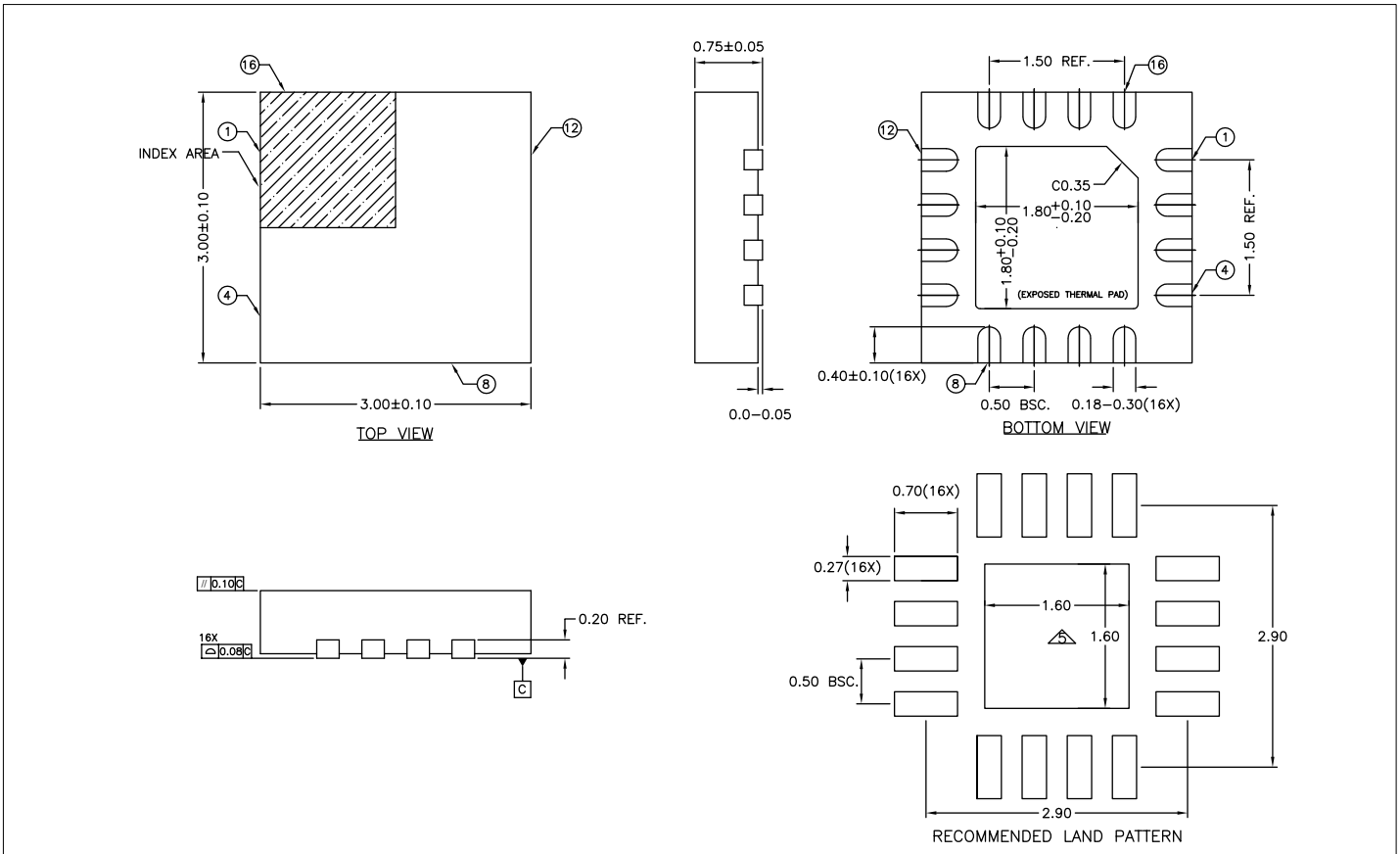


Part Marking

Top mark not available at this time. To obtain advance information regarding the top mark, please contact your local sales representative.

Packaging Mechanical

16-TQFN (ZH)



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO–220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL IS RECOMMENDED).

20-1297

	DATE: 06/17/20
DESCRIPTION: 16-contact, TQFN (W-QFN3030-16)	
PACKAGE CODE: ZH (ZH16)	
DOCUMENT CONTROL #: PD-2047	REVISION: F

For latest package information:

See http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/.

Ordering Information

Ordering Code	Package Code	Package Description	Operating Temperature
PI6C4911502DZHIEX	ZH	16-Contact, W-QFN3030-16 (TQFN)	-40°C to 85°C

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. I = Industrial
5. E = Pb-free and Green
6. X suffix = Tape/Reel

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