2.5V, 2GHz ANY DIFF. IN-TO-LVDS PROGRAMMABLE CLOCK DIVIDER/ FANOUT BUFFER W/INTERNAL TERMINATION

Precision Edge® SY89872U

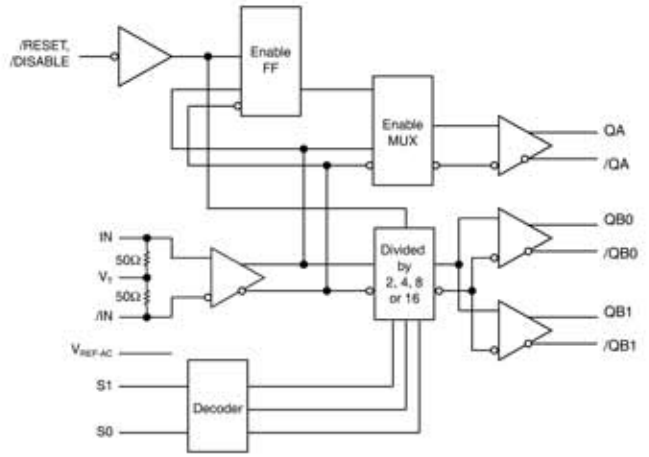
FEATURES

- Guaranteed AC performance over temperature and voltage:
  - >2GHz f_{MAX}
  - < 750ps t_{PD} (matched delay between banks)
  - < 15ps within-device skew
  - < 200ps rise/fall time
- Low jitter design
  - 265fs RMS phase jitter
- Unique input termination and VT pin for DC-coupled and AC-coupled inputs: any differential inputs (LVPECL, LVDS, CML, HSTL)
- Precision differential LVDS outputs
- Matched delay: all outputs have matched delay, independent of divider setting
- TTL/CMOS inputs for select and reset/disable
- Two output banks (matched delay)
  - Bank A: Buffered copy of input clock (undivided)
  - Bank B: Divided output (÷2, ÷4, ÷8, ÷16), two copies
- 2.5V power supply
- Wide operating temperature range: –40°C to +85°C
- Available in 16-pin (3mm x 3mm) QFN package

APPLICATIONS

- OC-3 to OC-192 SONET/SDH applications
- Transponders
- Oscillators
- SONET/SDH line cards

FUNCTIONAL BLOCK DIAGRAM



United States Patent No. RE44,134

Precision Edge is a registered trademark of Micrel, Inc.

Precision Edge®

DESCRIPTION

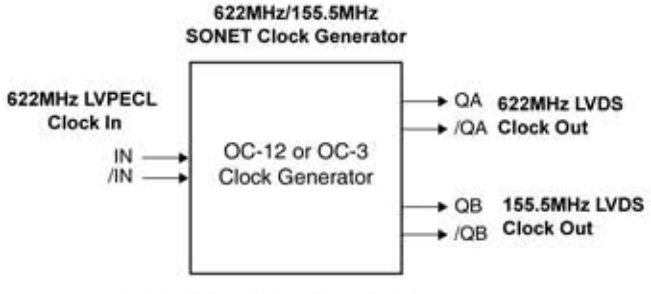
This 2.5V low-skew, low-jitter, precision LVDS output clock divider accepts any high-speed differential clock input (AC or DC-coupled) CML, LVPECL, HSTL or LVDS and divides down the frequency using a programmable divider ratio to create a frequency-locked, lower speed version of the input clock. The SY89872U includes two output banks. Bank A is an exact copy of the input clock (pass through) with matched propagation delay to Bank B, the divided output bank. Available divider ratios are 2, 4, 8 and 16. In a typical 622MHz clock system this would provide availability of 311MHz, 155MHz, 77MHz or 38MHz auxiliary clock components.

The differential input buffer has a unique internal termination design that allows access to the termination network through a V_T pin. This feature allows the device to easily interface to different logic standards. A V_{REF-AC} reference is included for AC-coupled applications.

The SY89872U is part of Micrel's high-speed Precision Edge® timing and distribution family. For 3.3V applications, consider the SY89873L. For applications that require an LVPECL output, consider the SY89872U.

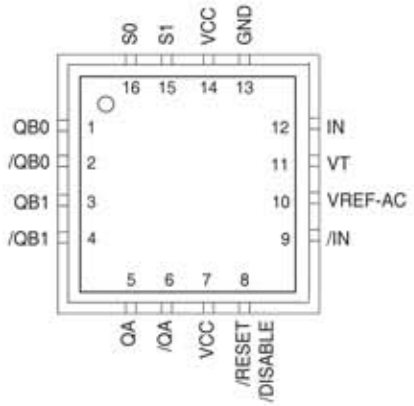
The /RESET input asynchronously resets the divider outputs (Bank B). In the pass-through function (Bank A) the /RESET synchronously enables or disables the outputs on the next falling edge of IN (rising edge of /IN). Refer to the "Timing Diagram."

TYPICAL APPLICATION



Bank A: 622MHz for OC-12 line card
Bank B: 155.5MHz for OC-3 line card (set to divide-by-4)

PACKAGE/ORDERING INFORMATION



16-Pin QFN

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89872UMG	QFN-16	Industrial	872U with Pb-Free bar line indicator	NiPdAu Pb-Free
SY89872UMGTR[2]	QFN-16	Industrial	872U with Pb-Free bar line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
1, 2, 3, 4	QB0, /QB0 QB1, /QB1	Differential LVDS Compatible Outputs: Divide by 2, 4, 8, 16. Unused outputs must be terminated with 100ý across the pin (Q, /Q).
5, 6	QA, /QA	Differential LVDS Compatible Undivided Output Clock.
7, 14	VCC	Positive Power Supply: Bypass with 0.1µF/0.01µF low ESR capacitors.
8	/RESET, /DISABLE	Output Reset and Output Enable/Disable: Internal 25ký pull-up. Input threshold is V_{CC}/2. Logic LOW will reset the divider select, and align Bank A and Bank B edges. In addition, when LOW, Bank A and Bank B will be disabled.
12, 9	IN, /IN	Differential Reference Input Clock: Internal 50ý termination resistors to V_T input. See "Input Interface Applications" section.
10	VREF-AC	Reference Voltage: Equal to V_{CC}–1.4V (approx.), and used for AC-coupled applications. Maximum sink/source current is 0.5mA. See "Input Interface Applications" section.
11	VT	Termination Center-Tap: For DC-coupled CML and LVDS inputs, leave this pin floating. See "Input Interface Applications" section.
13	GND	Ground.
15, 16	S1, S0	Select Pins: LVTTL/CMOS logic levels. Internal 25ký pull-up resistor. Logic HIGH if left unconnected (divided by 16 mode). S0 = LSB. Input threshold is V_{CC}/2.

TRUTH TABLE

/RESET /DISABLE	S1	S0	Bank A Output	Bank B Outputs
1	0	0	Input Clock	Input Clock ÷2
1	0	1	Input Clock	Input Clock ÷4
1	1	0	Input Clock	Input Clock ÷8
1	1	1	Input Clock	Input Clock ÷16
0	X	X	QA = Low, /QA = High[1]	QB0 = Low, /QB0 = High[2] QB1 = Low, /QB1 = High[2]

Note 1. On the next negative transition of the input signal.

Note 2. Asynchronous reset/disable function. (See "Timing Diagram")

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC}) ..... –0.5V to +6.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVDS Output Current (I_{OUT}) ..... ±10mA
Input Current IN, /IN (I_{IN}) ..... ±50mA
V_{REF-AC} Input Sink/Source Current ($I_{VREF-AC}$), **Note 3** . ±2mA
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature (T_S) ..... –65°C to +150°C

Operating Ratings(Note 2)

Supply Voltage Range ..... 2.375V to 2.625V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance
QFN (θ_{JA})
Still-Air ..... 60°C/W
500lfpm ..... 54°C/W
QFN (ψ_{JB}), **Note 4**
Junction-to-Board ..... 32°C/W

Note 1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratlng conditions for extended periods may affect device reliability.

Note 2. The datasheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 3. Due to the limited drive capability use for input of the same package only.

Note 4. Junction-to-board resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.

DC ELECTRICAL CHARACTERISTICS(Note 1, 2)

T_A= –40°C to +85°C; Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage		2.375	2.5	2.625	V
I_{CC}	Power Supply Current	No load, max. V_{CC}		75	110	mA
R_{IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	ý
V_{IH}	Input High Voltage IN, /IN	Note 3	0.1		V_{CC}+0.3	V
V_{IL}	Input Low Voltage IN, /IN	Note 3	–0.3		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing	Notes 3, 4	0.1		V_{CC}	V
V_{DIFF_IN}	Differential Input Voltage Swing	Notes 3, 4, 5	0.2			V
$\|I_{IN}\|$	Input Current IN, /IN	Note 3			45	mA
V_{REF-AC}	Reference Voltage	Note 6	V_{CC} –1.525	V_{CC}–1.425	V_{CC}–1.325	V

Note 1. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

Note 2. Specification for packaged product only.

Note 3. Due to the internal termination (see *"Input Buffer Structure"* section) the input current depends on the applied voltages at IN, /IN and V_T inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit!

Note 4. See "Timing Diagram" for V_{IN} definition. V_{IN} (max.) is specified when V_T is floating.

Note 5. See Figures 1c and 1d for V_{DIFF} definition.

Note 6. Operating using V_{IN} is limited to AC-coupled PECL or CML applications only. Connect directly to V_T pin.

LVDS OUTPUTS DC ELECTRICAL CHARACTERISTICS(Note 1, 2)

V_{CC} = 2.5V ±5%; T_A = –40°C to +85°C; Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT}	Output Voltage Swing	**Note 5**	250	350	450	mV
V_{OH}	Output High Voltage	**Note 3**			1.475	V
V_{OL}	Output Low Voltage	**Note 3**	0.925			V
V_{OCM}	Output Common Mode Voltage	**Note 4**	1.125		1.375	V
ΔV_{OCM}	Change in Common Mode Voltage		–50		50	mV

Note 1. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
Note 2. Specification for packaged product only.
Note 3. Measured as per Figure 1a, 100ý across Q and /Q outputs.
Note 4. Measured as per Figure 1b.
Note 5. See Figure 1c.

LVTTL/CMOS INPUTS DC ELECTRICAL CHARACTERISTICS(Note 1, 2)

V_{CC} = 2.5V ±5%; T_A = –40°C to +85°C; Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0	–	V_{CC}	V
V_{IL}	Input LOW Voltage		0	–	0.8	V
I_{IH}	Input HIGH Current		–125	–	20	µA
I_{IL}	Input LOW Current		–	–	–300	µA

Note 1. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
Note 2. Specification for packaged product only.

AC ELECTRICAL CHARACTERISTICS[Note 1, 2]

V_{CC} = 2.5V ±5%; T_A = –40°C to +85°C; Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Toggle Frequency	Output Swing: ž200mV	2			GHz
	Maximum Input Frequency	Note 3	3.2			GHz
t_{PD}	Differential Propagation Delay IN to Q	Input Swing: <400mV	500	625	750	ps
		Input Swing: ž400mV	450	575	700	ps
t_{SKEW}	Within-Device Skew (differential) (QB0-to-QB1)	Note 4		7	15	ps
	Within-Device Skew (differential) (Bank A-to-Bank B)	Note 4		12	30	ps
	Part-to-Part Skew (differential)	Note 4			250	ps
t_{rr}	Reset Recovery Time	Note 5	600			ps
T_{jitter}	RMS Phase Jitter	Output = 622MHz Integration Range: 12kHz - 20MHz		265		fs
t_r, t_f	Rise / Fall Time (20% to 80%)		70	130	200	ps

Note 1. Measured with 400mV input signal, 50% duty cycle. 100ý termination between Q and /Q, unless otherwise stated.

Note 2. Specification packaged product only.

Note 3. Bank A (pass-through) maximum frequency is limited by the output stage. Bank B (input-to-output ÷2, ÷4, ÷8, ÷16) can accept an input frequency >3GHz, while Bank A will be slew rate limited.

Note 4. Skew is measured between outputs under identical transitions.

Note 5. See *"Timing Diagram."*

LVDS OUTPUT

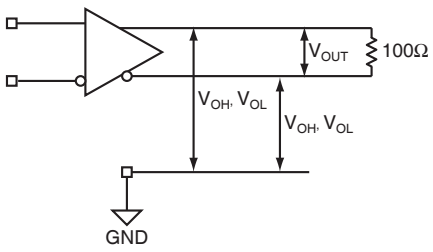


Figure 1a. LVDS Differential Measurement

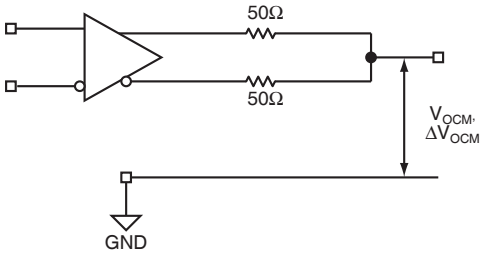


Figure 1b. LVDS Common Mode Measurement

DEFINITION OF SINGLE-ENDED AND DIFFERENTIAL SWING

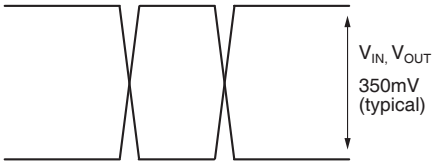


Figure 1c. Single-Ended Swing

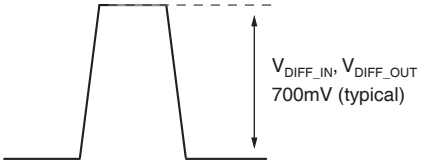
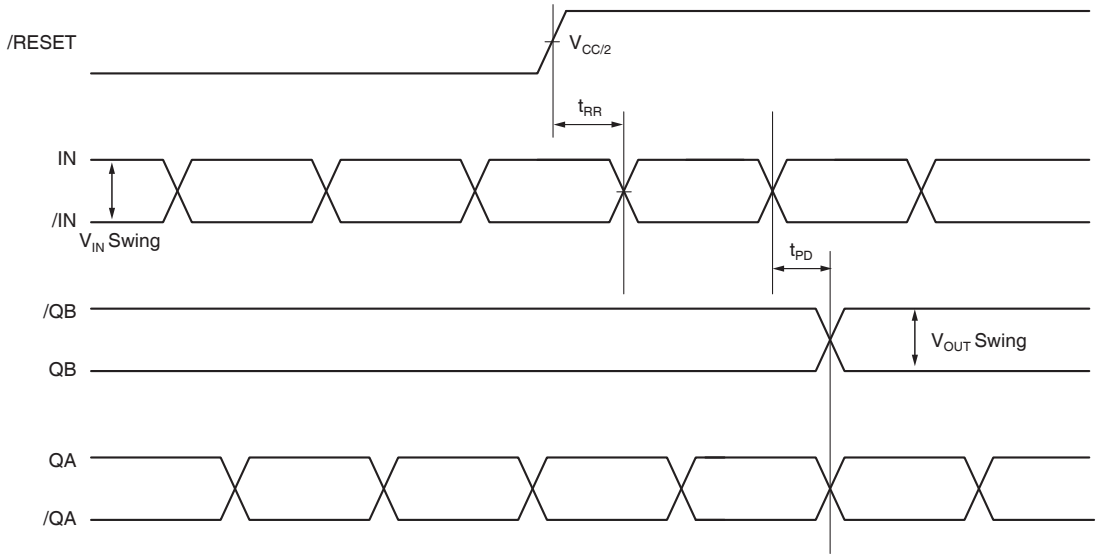


Figure 1d. Differential Swing

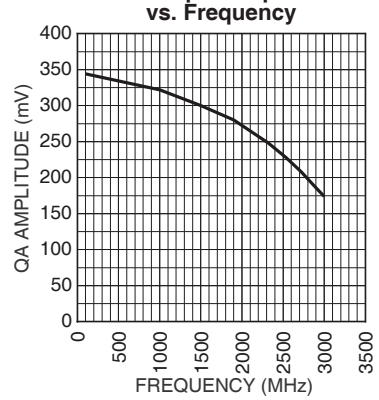
TIMING DIAGRAM



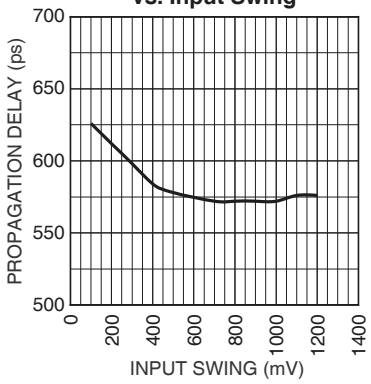
TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 2.5V, V_{IN} = 400mV, T_A = 25°C, unless otherwise stated.

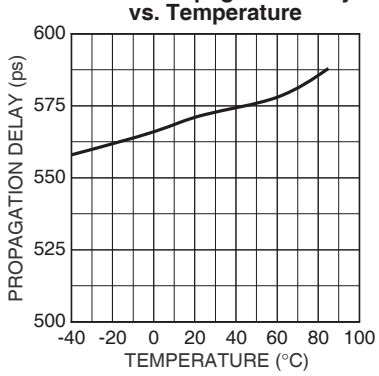
QA Output Amplitude vs. Frequency



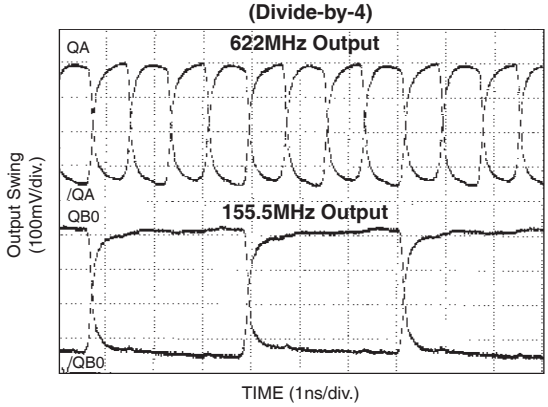
IN to Q Propagation Delay vs. Input Swing



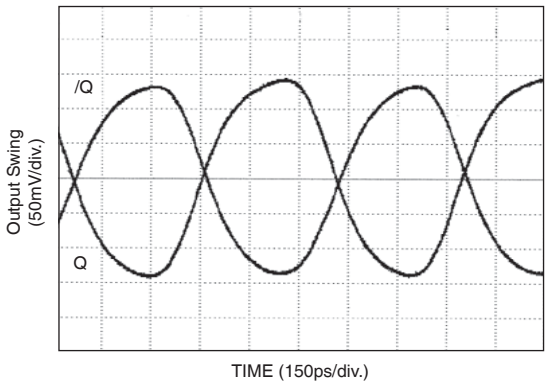
IN to Q Propagation Delay vs. Temperature



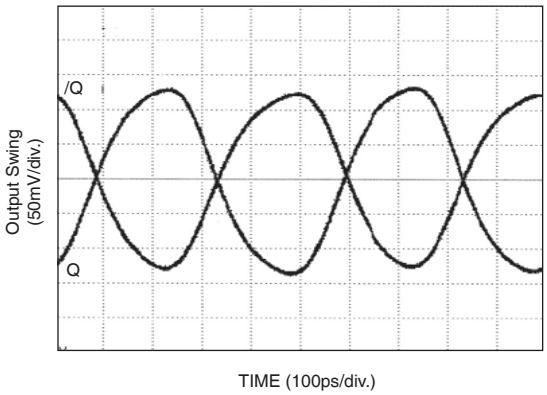
QA @622MHz and QB @155.5MHz (Divide-by-4)



1.25GHz Output



2GHz Output



INPUT BUFFER STRUCTURE

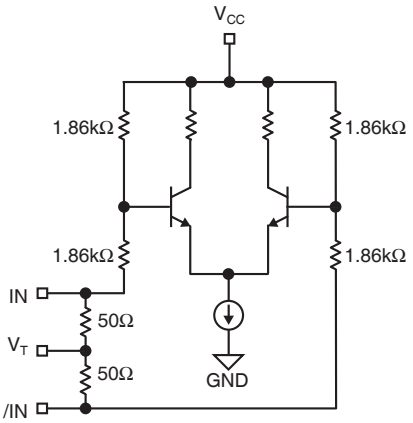


Figure 2a. Simplified Differential Input Buffer

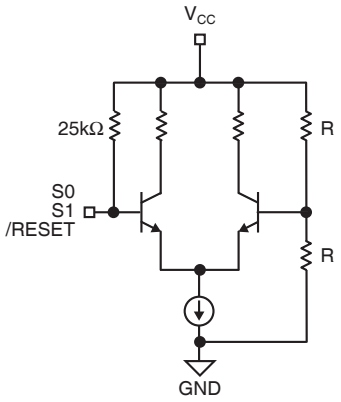


Figure 2b. Simplified TTL/CMOS Input Buffer

INPUT INTERFACE APPLICATIONS

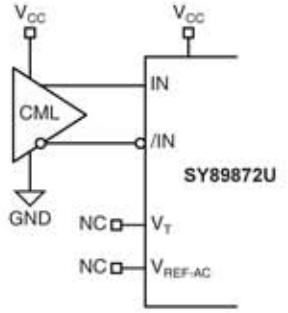


Figure 3a. DC-Coupled CML Input Interface

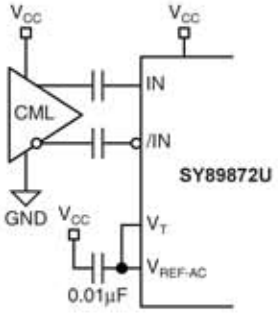


Figure 3b. AC-Coupled CML Input Interface

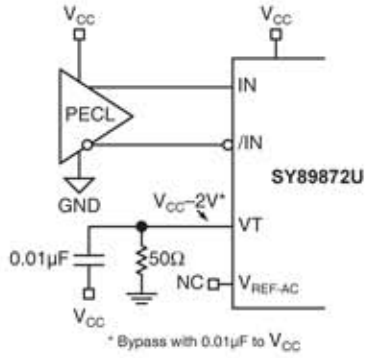


Figure 3c. DC-Coupled PECL Input Interface

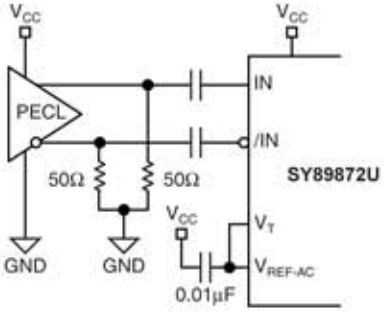


Figure 3d. AC-Coupled PECL Input Interface

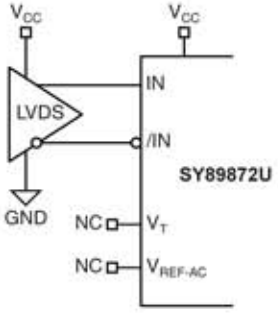


Figure 3e. LVDS Input Interface

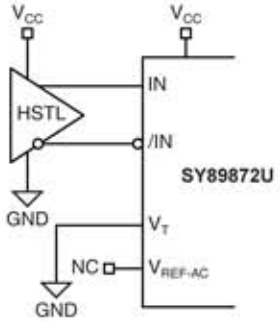
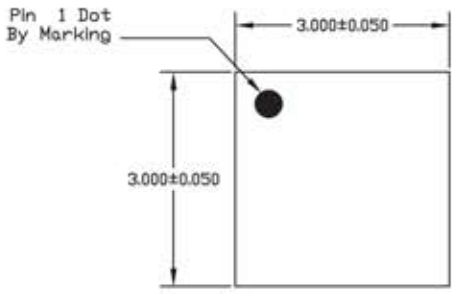


Figure 3f. HSTL Input Interface

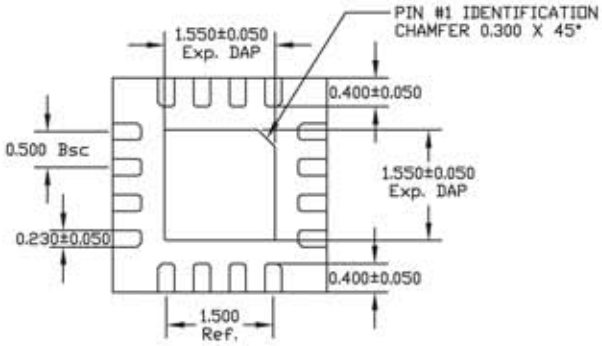
RELATED PRODUCT AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY89871U	2.5GHz Any Diff. In-to-LVPECL Programmable Clock Divider/Fanout Buffer w/Internal Termination	http://www.micrel.com/product-info/products/sy89871u.shtml
SY89873L	3.3V, 2GHz Any Diff. In-to-LVDS Programmable Clock Divider/Fanout Buffer	http://www.micrel.com/product-info/products/sy89873l.shtml
HBW Solutions	New Products and Applications	http://www.micrel.com/product-info/products/solutions.shtml

16-PIN QFN (QFN-16)

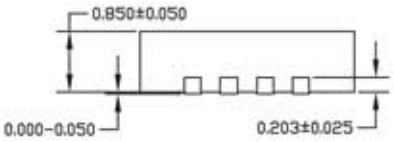


TOP VIEW

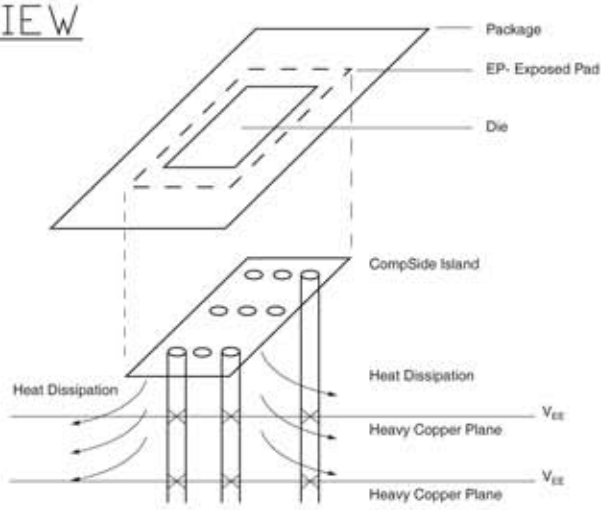


BOTTOM VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



SIDE VIEW



PCB Thermal Consideration for 16-Pin QFN Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

Note 1. Package meets Level 2 moisture sensitivity classification, and is shipped in dry-pack form.

Note 2. Exposed pads must be soldered to a ground for proper thermal management.

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