



LOW SKEW, 1-TO-4 DIFFERENTIAL-TO-LVDS FANOUT BUFFER

ICS889832

GENERAL DESCRIPTION

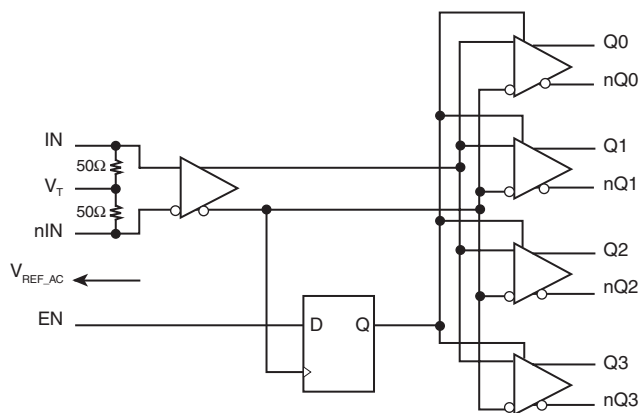


The ICS889832 is a high speed 1-to-4 Differential-to-LVDS Fanout Buffer and is a member of the HiPerClockS™ family of high performance clock solutions from IDT. The ICS889832 is optimized for high speed and very low output skew, making it suitable for use in demanding applications such as SONET, 1 Gigabit and 10 Gigabit Ethernet, and Fibre Channel. The internally terminated differential input and V_{REF_AC} pin allow other differential signal families such as LVPECL, LVDS, and SSTL to be easily interfaced to the input with minimal use of external components. The device also has an output enable pin which may be useful for system test and debug purposes. The ICS889832 is packaged in a small 3mm x 3mm 16-pin VFQFN package which makes it ideal for use in space-constrained applications.

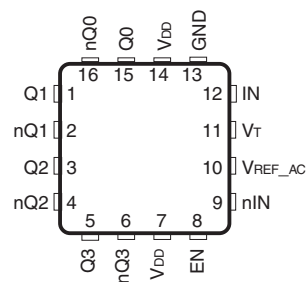
FEATURES

- Four differential LVDS outputs
- IN, nIN pair can accept the following differential input levels: LVPECL, LVDS, SSTL
- 50Ω internal input termination to V_T
- Output frequency: >2GHz
- Output skew: 25ps (maximum)
- Part-to-part skew: 200ps (maximum)
- Additive phase jitter, RMS: <0.2ps (typical)
- Propagation delay: 510ps (maximum)
- 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS889832
16-Lead VFQFN
 3mm x 3mm x 0.925 package body
K Package
 Top View

TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|--------|---------------------|--------|--------|--|
| 1, 2 | Q1, nQ1 | Output | | Differential output pair. LVDS interface levels. |
| 3, 4 | Q2, nQ2 | Output | | Differential output pair. LVDS interface levels. |
| 5, 6 | Q3, nQ3 | Output | | Differential output pair. LVDS interface levels. |
| 7, 14 | V _{DD} | Power | | Positive supply pins. |
| 8 | EN | Input | Pullup | Synchronizing clock enable. When LOW, Q outputs will go LOW and nQ outputs will go HIGH on the next LOW transition at IN inputs. Input threshold is V _{DD} /2V. Includes a 37kΩ pull-up resistor. Default state is HIGH when left floating. The internal latch is clocked on the falling edge of the input signal IN. LVTTTL / LVCMOS interface levels. |
| 9 | nIN | Input | | Inverting differential clock input. 50Ω internal input termination to V _T . |
| 10 | V _{REF_AC} | Output | | Reference voltage for AC-coupled applications. |
| 11 | V _T | Input | | Termination input. |
| 12 | IN | Input | | Non-inverting differential clock input. 50Ω internal input termination to V _T . |
| 13 | GND | Power | | Power supply ground. |
| 15, 16 | Q0, nQ0 | Output | | Differential output pair. LVDS interface levels. |

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---------------------|-----------------------|-----------------|---------|---------|---------|-------|
| R _{PULLUP} | Input Pullup Resistor | | | 37 | | kΩ |

TABLE 3A. CONTROL INPUT FUNCTION TABLE

| Input | Outputs | |
|-------|---------------|----------------|
| | Q0:Q3 | nQ0:nQ3 |
| 0 | Disabled; LOW | Disabled; HIGH |
| 1 | Enabled | Enabled |

After EN switches, the clock outputs are disabled or enabled following a falling input clock edge as shown in Figure 1.

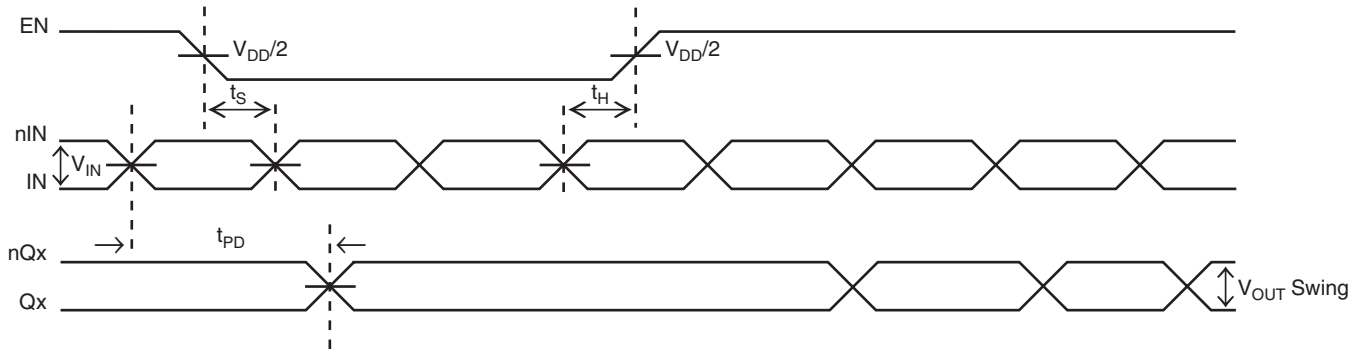


FIGURE 1. EN TIMING DIAGRAM

TABLE 3B. TRUTH TABLE

| Inputs | | | Outputs | |
|--------|-----|----|----------------------|----------------------|
| IN | nIN | EN | Q0:Q3 | nQ0:nQ3 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| X | X | 0 | 0 ^(NOTE1) | 1 ^(NOTE1) |

NOTE 1: On next negative transition of the input signal (IN).

ABSOLUTE MAXIMUM RATINGS

| | |
|---|---------------------------|
| Supply Voltage, V_{DD} | 4.6V |
| Inputs, V_I | -0.5V to $V_{DD} + 0.5$ V |
| Outputs, I_O (LVDS) | |
| Continuous Current | 10mA |
| Surge Current | 15mA |
| Input Current, I_N , nIN | ± 50 mA |
| V_T Current, I_{VT} | ± 100 mA |
| Input Sink/Source, I_{REF_AC} | ± 0.5 mA |
| Operating Temperature Range, T_A | -40°C to +85°C |
| Storage Temperature, T_{STG} | -65°C to 150°C |
| Package Thermal Impedance, θ_{JA} (Junction-to-Ambient) | 88.5°C/W (0 mps) |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 2.5V \pm 5\%$; $T_A = -40^\circ\text{C}$ TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-------------------------|-----------------|---------|---------|---------|-------|
| V_{DD} | Positive Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| I_{DD} | Power Supply Current | | | | 120 | mA |

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = 2.5V \pm 5\%$; $T_A = -40^\circ\text{C}$ TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|--------------------------------------|---------|---------|----------------|---------------|
| V_{IH} | Input High Voltage | | 1.7 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | 0 | | 0.7 | V |
| I_{IH} | Input High Current | EN $V_{DD} = V_{IN} = 2.625V$ | | | 5 | μA |
| I_{IL} | Input Low Current | EN $V_{DD} = 2.625V, V_{IN} = 0V$ | -150 | | | μA |

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = 2.5V \pm 5\%$; $T_A = -40^\circ\text{C}$ TO 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------|----------------------------------|-----------------------|-----------------|-----------------|-----------------|----------|
| R_{IN} | Differential Input Resistance | (IN, nIN) IN-to-VT | 40 | 50 | 60 | Ω |
| V_{IH} | Input High Voltage | (IN, nIN) | 1.2 | | V_{DD} | V |
| V_{IL} | Input Low Voltage | (IN, nIN) | 0 | | $V_{IH} - 0.15$ | V |
| V_{IN} | Input Voltage Swing | | 0.15 | | 2.8 | V |
| V_{REF_AC} | Reference Voltage | | $V_{DD} - 1.42$ | $V_{DD} - 1.37$ | $V_{DD} - 1.32$ | V |
| V_{DIFF_IN} | Differential Input Voltage Swing | | 0.3 | | 3.4 | V |
| I_{IN} | Input Current; NOTE 1 | (IN, nIN) | | | 35 | mA |

NOTE 1: Guaranteed by design.

TABLE 4D. LVDS DC CHARACTERISTICS, $V_{DD} = 2.5V \pm 5\%$; $T_A = -40^{\circ}C$ TO $85^{\circ}C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------|-----------------|---------|---------|---------|-------|
| V_{OD} | Differential Output Voltage | | 0.3 | 0.4 | 0.5 | mV |
| ΔV_{OD} | V_{OD} Magnitude Change | | | | 50 | mV |
| V_{OS} | Offset Voltage | | 1 | 1.25 | 1.5 | V |
| ΔV_{OS} | V_{OS} Magnitude Change | | | | 50 | mV |

TABLE 5. AC CHARACTERISTICS, $V_{DD} = 2.5V \pm 5\%$; $T_A = -40^{\circ}C$ TO $85^{\circ}C$

| Symbol | Parameter | Condition | Minimum | Typical | Maximum | Units |
|--------------|--|-------------------------------------|---------|---------|---------|-------|
| f_{MAX} | Maximum Output Frequency | | | >2 | | GHz |
| t_{PD} | Propagation Delay; (Differential); NOTE 1 | | 275 | 390 | 510 | ps |
| $t_{sk(o)}$ | Output Skew; NOTE 2, 4 | | | | 25 | ps |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 3, 4 | | | | 200 | ps |
| t_{jit} | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section | Integration Range: 12kHz - 20MHz | | <0.2 | | ps |
| t_R/t_F | Output Rise/Fall Time | 20% to 80% | 70 | 150 | 235 | ps |
| t_S | Clock Enable Setup Time | EN to IN, nIN | 300 | | | ps |
| t_H | Clock Enable Hold Time | EN to IN, nIN | 300 | | | ps |

All parameters are measured at ≤ 1 GHz unless otherwise noted.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

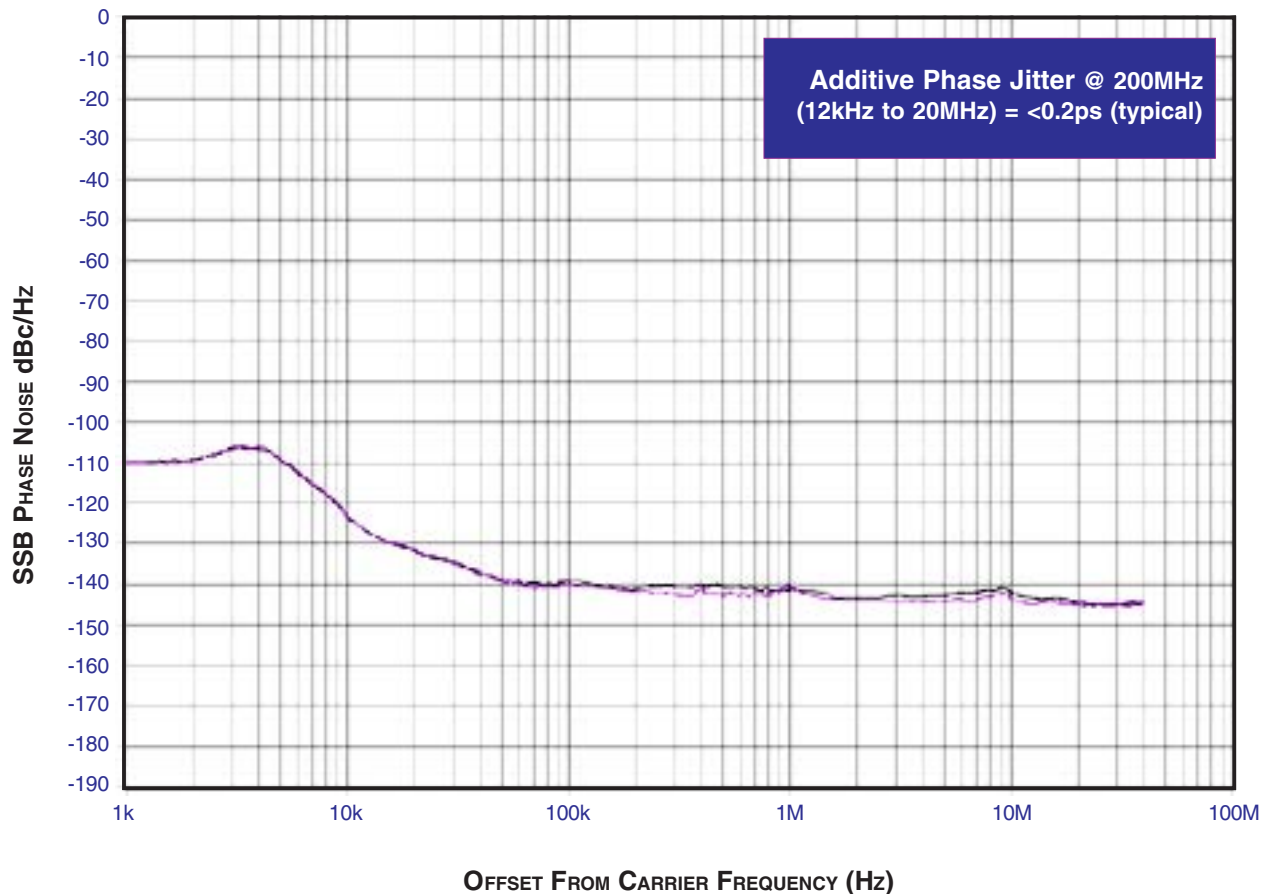
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise***. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz

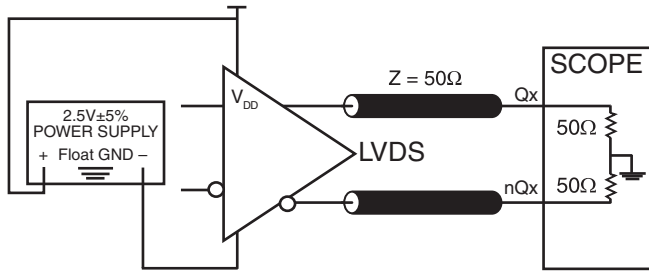
band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



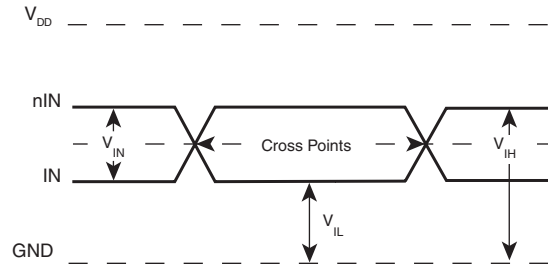
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the

device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

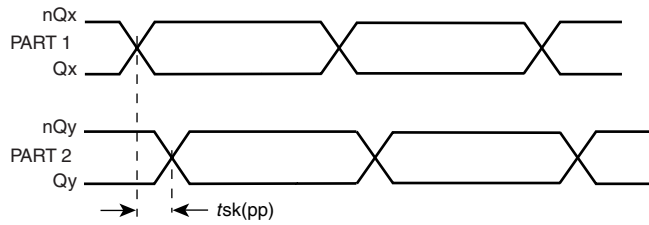
PARAMETER MEASUREMENT INFORMATION



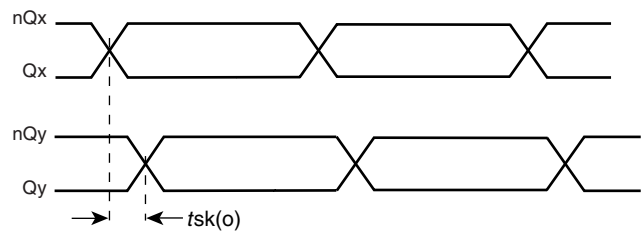
OUTPUT LOAD AC TEST CIRCUIT



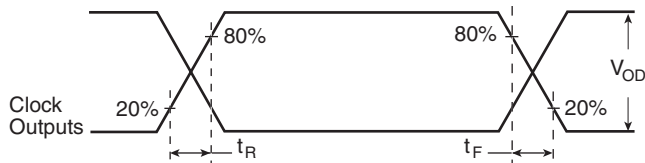
DIFFERENTIAL INPUT LEVEL



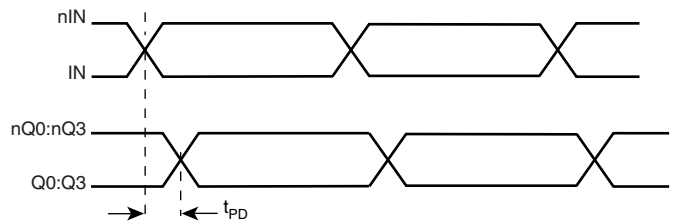
PART-TO-PART SKEW



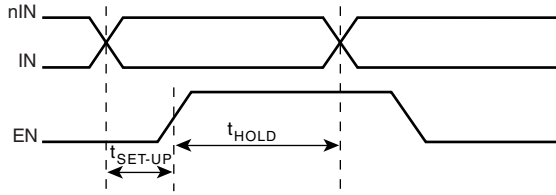
OUTPUT SKEW



OUTPUT RISE/FALL TIME

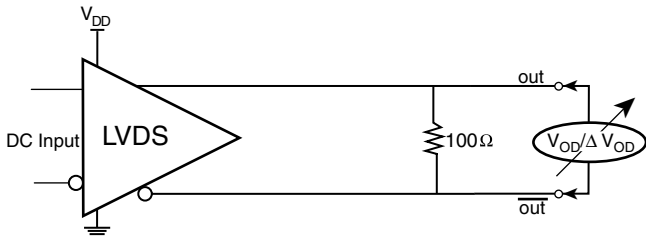


PROPAGATION DELAY

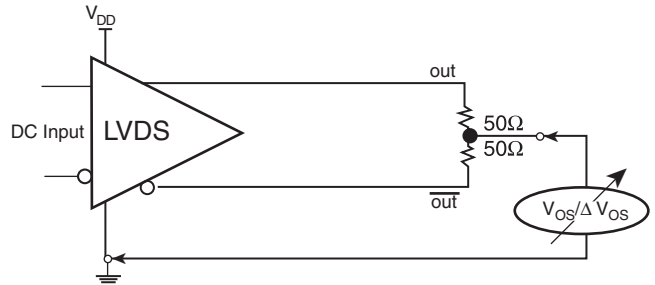


SETUP & HOLD TIME

SINGLE ENDED & DIFFERENTIAL INPUT VOLTAGE SWING



DIFFERENTIAL OUTPUT VOLTAGE SETUP



OFFSET VOLTAGE SETUP

APPLICATION INFORMATION

LVPECL INPUT WITH BUILT-IN 50Ω TERMINATIONS INTERFACE

The IN/nIN with built-in 50Ω terminations accepts LVDS, LVPECL, LVHSTL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 1A to 1f show interface examples for the HiPerClockS IN/nIN input with built-in 50Ω terminations driven by the most common

driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

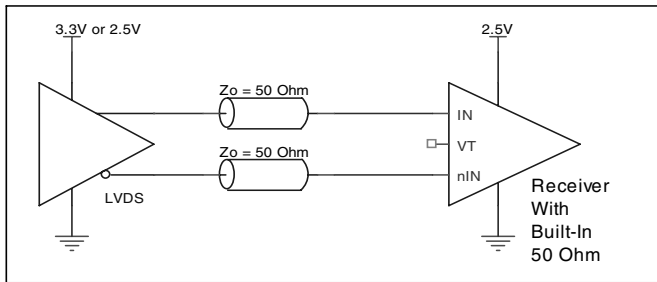


FIGURE 1A. HiPerClockS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVDS DRIVER

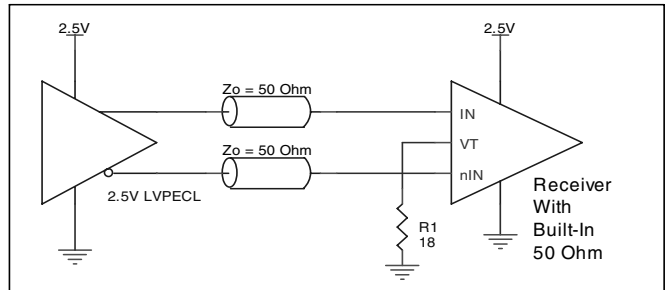


FIGURE 1B. HiPerClockS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVPECL DRIVER

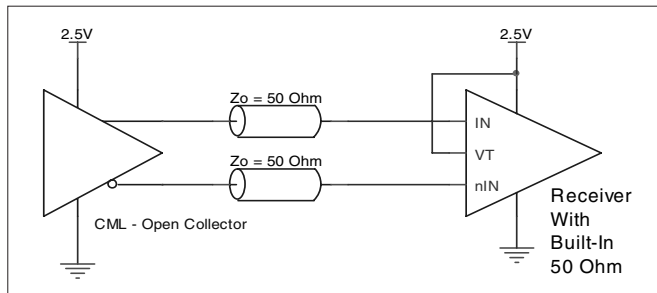


FIGURE 1C. HiPerClockS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN OPEN COLLECTOR CML DRIVER

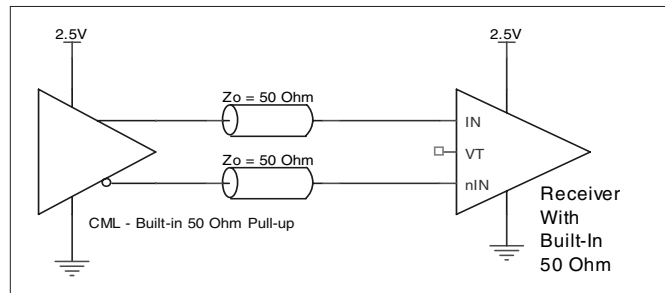


FIGURE 1D. HiPerClockS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A CML DRIVER WITH BUILT-IN 50Ω PULLUP

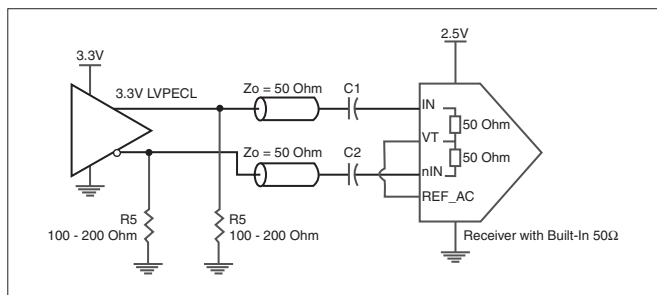


FIGURE 1E. HiPerClockS IN/nIN INPUT WITH BUILT-IN 50Ω

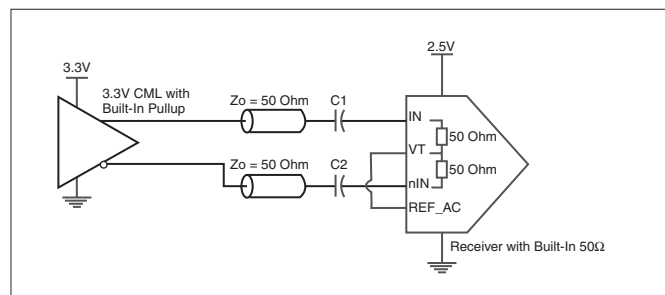


FIGURE 1F. HiPerClockS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A 3.3V CML DRIVER WITH BUILT-IN PULLUP

RECOMMENDATIONS FOR UNUSED OUTPUT PINS

OUTPUTS:

LVDS Outputs

All unused LVDS outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

2.5V LVDS DRIVER TERMINATION

Figure 2 shows a typical termination for LVDS driver in characteristic impedance of 100Ω differential (50Ω single)

transmission line environment. For buffer with multiple LVDS driver, it is recommended to terminate the unused outputs.

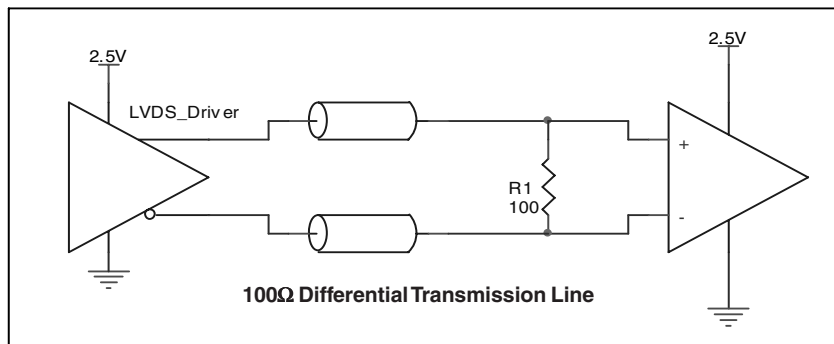


FIGURE 2. TYPICAL LVDS DRIVER TERMINATION

VFQFN EPAD THERMAL RELEASE PATH

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”)

are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

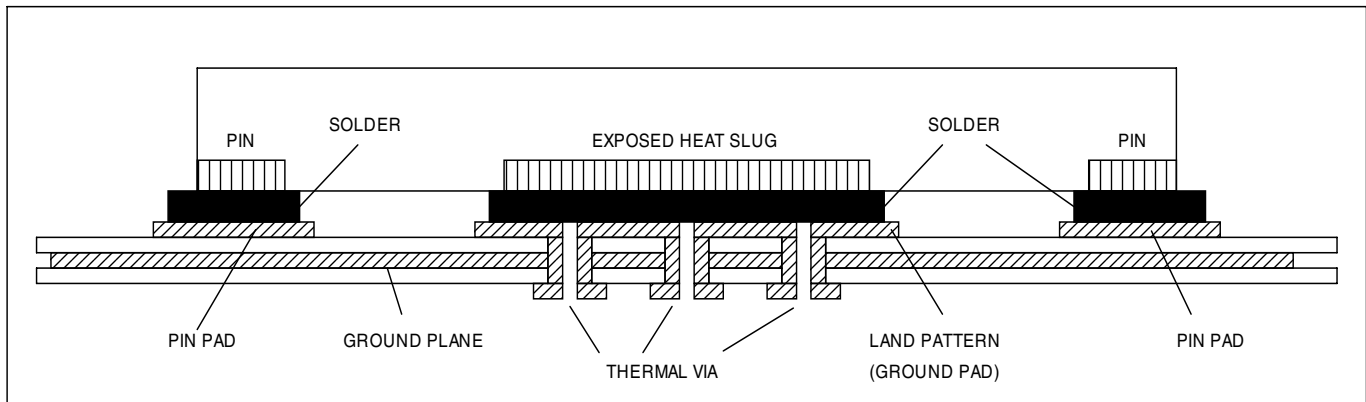


FIGURE 3. P.C.ASSEMBLY FOR EXPOSED PAD THERMAL RELEASE PATH –SIDE VIEW (DRAWING NOT TO SCALE)

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS889832. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS889832 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 2.5V + 5\% = 2.625V$, which gives worst case results.

- $Power_{-MAX} = V_{DD_MAX} * I_{DD_MAX} = 2.625V * 120mA = 315mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClocks™ devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 88.5°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:
 $85^\circ C + 0.315W * 88.5^\circ C/W = 112.9^\circ C$. This is well below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 16-PIN VFQFN, FORCED CONVECTION

| θ_{JA} vs. 0 Air Flow (Meters per Second) | | | |
|--|----------|----------|----------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 88.5°C/W | 77.3°C/W | 69.4°C/W |

RELIABILITY INFORMATION

TABLE 7. θ_{JA} vs. AIR FLOW TABLE FOR 16 LEAD VFQFN

| θ_{JA} vs. 0 Air Flow (Meters per Second) | | | |
|--|----------|----------|----------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 88.5°C/W | 77.3°C/W | 69.4°C/W |

TRANSISTOR COUNT

The transistor count for ICS889832 is: 206

Pin compatible with SY89832U

PACKAGE OUTLINE - K SUFFIX FOR 16 LEAD VFQFN

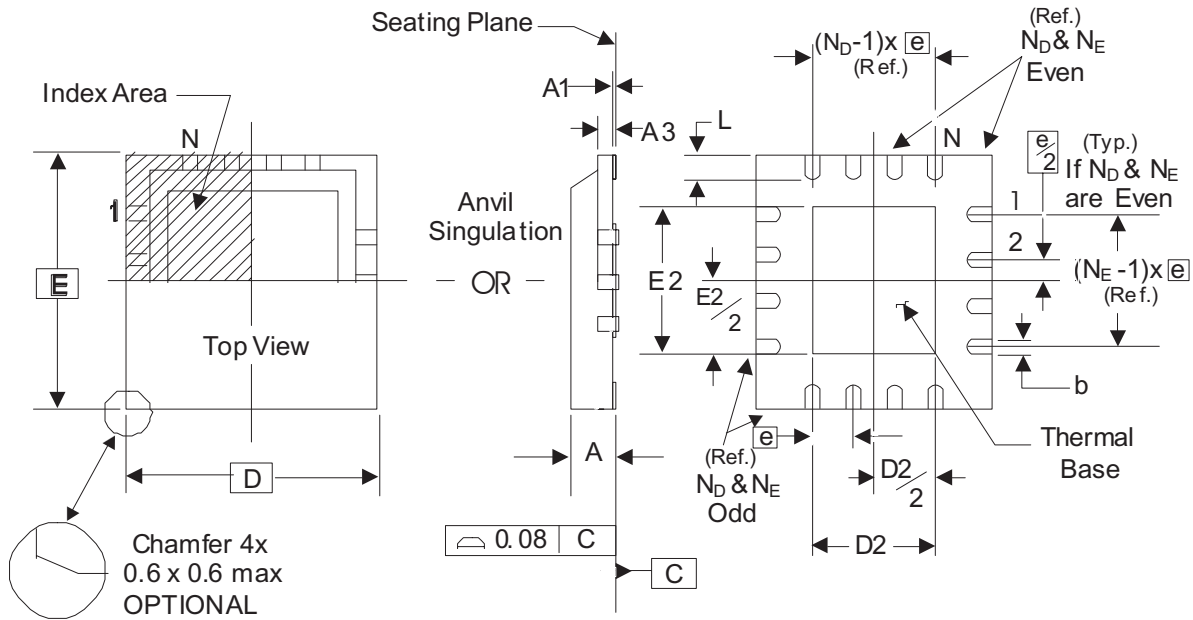


TABLE 8. PACKAGE DIMENSIONS

| JEDEC VARIATION | | |
|-------------------------------|----------------|---------|
| ALL DIMENSIONS IN MILLIMETERS | | |
| SYMBOL | MINIMUM | MAXIMUM |
| N | 16 | |
| A | 0.80 | 1.0 |
| A1 | 0 | 0.05 |
| A3 | 0.25 Reference | |
| b | 0.18 | 0.30 |
| e | 0.50 BASIC | |
| N_D | 4 | |
| N_E | 4 | |
| D | 3.0 | |
| D2 | 1.0 | 1.8 |
| E | 3.0 | |
| E2 | 1.0 | 1.8 |
| L | 0.30 | 0.50 |

Reference Document: JEDEC Publication 95, MO-220

TABLE 9. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|---------|---------------------------|--------------------|---------------|
| 889832AK | 832A | 16 Lead VFQFN | tube | -40°C to 85°C |
| 889832AKT | 832A | 16 Lead VFQFN | 2500 tape & reel | -40°C to 85°C |
| 889832AKLF | 32AL | 16 Lead "Lead-Free" VFQFN | tube | -40°C to 85°C |
| 889832AKLFT | 32AL | 16 Lead "Lead-Free" VFQFN | 2500 tape & reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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REVISION HISTORY SHEET

| Rev | Table | Page | Description of Change | Date |
|-----|----------------|------|--|---------|
| A | T8 | 13 | Package Dimensions - corrected D2/E2 minimum from 0.25mm to 1.0mm. | 1/22/07 |
| | T9 | 14 | Ordering Information table - added lead-free marking. | |
| A | T6 T7 T9 | 4 | Absolute Maximum Ratings - updated Package Thermal Impedance. | 1/30/08 |
| | | 11 | Updated <i>VFQFN Thermal Release Path</i> section. | |
| | | 12 | Updated <i>Thermal Resistance Table and Junction Temperature calculation</i> . | |
| | | 13 | Updated <i>Reliability Information</i> . | |
| | | 14 | Updated <i>Package Outline</i> . | |
| | T9 | 15 | Corrected <i>Lead-Free Part/Order Number</i> . | |
| | | | | |

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For Sales

800-345-7015
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480-763-2056

Corporate Headquarters

Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Japan

NIPPON IDT KK
Sanbancho Tokyu Bld. 7F,
8-1 Sanbancho
Chiyoda-ku, Tokyo 102-0075
+81 3 3221 9822
+81 3 3221 9824 (fax)

Asia

Integrated Device Technology
IDT (S) Pte. Ltd.
1 Kallang Sector, #07-01/06
Kolam Ayer Industrial Park
Singapore 349276
+65 6 744 3356
+65 6 744 1764 (fax)

Europe

IDT Europe, Limited
321 Kingston Road
Leatherhead, Surrey
KT22 7TU
England
+44 (0) 1372 363 339
+44 (0) 1372 378851 (fax)