

## Low Voltage 1.2V/1.8V/2.5V CML 1:2 Fanout Buffer, 6.4 Gbps with Equalization

### Features

- 1.2V/1.8V/2.5V CML 1:2 Fanout Buffer
- Equalizes 9, 18, 27 inches of FR4
- Guaranteed AC Performance over Temperature and Voltage:
  - DC- to > 6.4 Gbps Throughput
  - DC- to > 4.5 GHz Clock Throughput
  - <280 ps Propagation Delay (IN-to-Q)
  - <15 ps Within-Device Skew
  - <80 ps Rise/Fall Times
- Ultra-Low Jitter Design
  - 1 ps<sub>RMS</sub> Random Jitter
- High Speed CML Outputs
- 2.5V ±5% V<sub>CC</sub>, 1.2V/1.8V/2.5V ±5% V<sub>CCO</sub> Power Supply Operation
- Industrial Temperature Range: -40°C to +85°C
- Available in 16-pin (3 mm x 3 mm) QFN Package

### Applications

- Data Distribution: OC-48, OC-48+FEC
- SONET Clock and Data Distribution
- Fibre Channel Clock and Data Distribution
- Gigabit Ethernet Clock and Data Distribution

### Markets

- Storage
- ATE
- Test and Measurement
- Enterprise Networking Equipment
- High-End Servers
- Access
- Metro Area Network Equipment

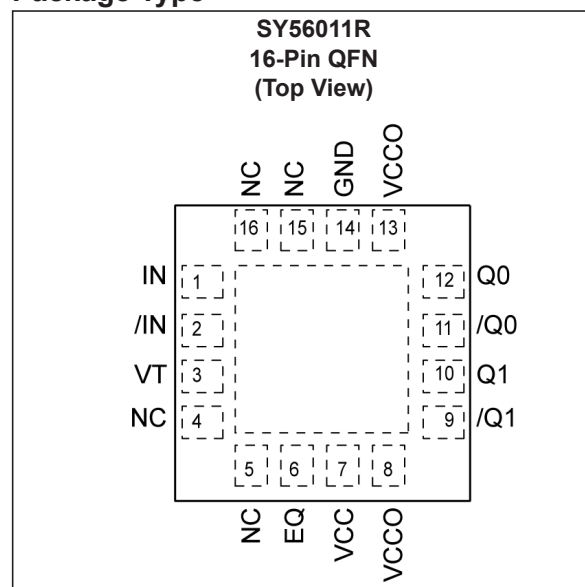
### General Description

The SY56011R is a fully differential, low voltage 1.2V/1.8V/2.5V CML 1:2 Fanout Buffer with input equalization. The SY56011R can process clock signals as fast as 4.5 GHz or data patterns up to 6.4 Gbps.

The differential input includes a unique, 3-pin input termination architecture that interfaces to CML differential signals, without any level-shifting or termination resistor networks in the signal path. The differential input can also accept AC-coupled LVPECL and LVDS signals. Input voltages as small as 200 mV (400 mV<sub>PP</sub>) are applied before the 9", 18", or 27" FR4 transmission line. For AC-coupled input interface applications, an internal voltage reference is provided to bias the VT pin. The outputs are CML, with extremely fast rise/fall times guaranteed to be less than 80 ps.

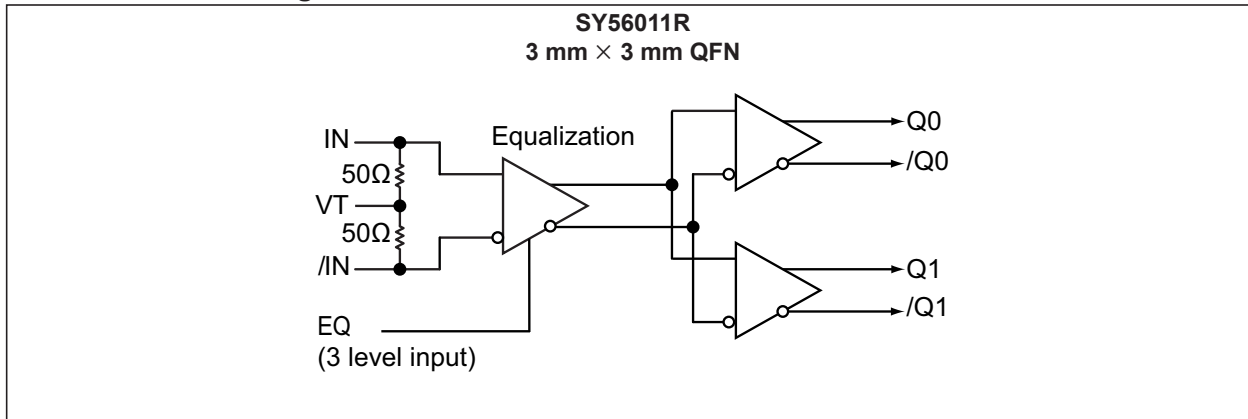
The SY56011R operates from a 2.5V ±5% core supply and a 1.2V, 1.8V, or 2.5V ±5% output supply and is guaranteed over the full industrial temperature range (-40°C to +85°C). The SY56011R is part of the high speed, Precision Edge<sup>®</sup> product line.

### Package Type



# SY56011R

## Functional Block Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Supply Voltage ( $V_{CC}$ )	-0.5V to +3.0V
Supply Voltage ( $V_{CCO}$ )	-0.5V to +3.0V
$V_{CC} - V_{CCO}$	<1.8V
$V_{CCO} - V_{CC}$	<0.5V
Input Voltage ( $V_{IN}$ )	-0.5V to $V_{CC}$
CML Output Voltage ( $V_{OUT}$ )	0.6V to +3.0V
Current ( $I_T$ )	
Source or sink current on VT pin	±100 mA
Input Current	
Source or sink current on (IN, /IN)	±50 mA

### Operating Ratings ††

Supply Voltage ( $V_{CC}$ )	2.375V to 2.625V
( $V_{CCO}$ )	1.14V to 2.625V
Ambient Temperature ( $T_A$ )	-40°C to +85°C

**† Notice:** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

**†† Notice:** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

# SY56011R

## DC ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Characteristics:  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise stated.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Voltage Range	$V_{CC}$	2.375	2.5	2.625	V	—
	$V_{CCO}$	1.14	1.2	1.26		
		1.7	1.8	1.9		
		2.375	2.5	2.625		
Power Supply Current	$I_{CC}$	—	54	75	mA	—
	$I_{CCO}$	—	32	42	mA	—
Input Resistance (IN-to-VT, /IN-to-VT)	$R_{IN}$	45	50	55	$\Omega$	—
Differential Input Resistance (IN-to-/IN)	$R_{DIFF\_IN}$	90	100	110	$\Omega$	—
Input High Voltage (IN, /IN)	$V_{IH}$	1.42	—	$V_{CC}$	V	IN, /IN
Input Low Voltage (IN, /IN)	$V_{IL}$	1.22	—	$V_{IH} - 0.2$	V	IN, /IN
Input Voltage Swing (IN, /IN)	$V_{IN}$	0.2	—	1.0	V	See Figure 5-1, (Note 2), applied to input of transmission line.
Differential Input Voltage Swing ( IN- /IN )	$V_{DIFF\_IN}$	0.4	—	2.0	V	See Figure 5-1, (Note 2), applied to input of transmission line.
Voltage from Input to VT	$V_{T\_IN}$	—	—	1.28	V	—

**Note 1:** The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

**2:**  $V_{IN(max)}$  and  $V_{DIFF-IN(MAX)}$  are specified when VT is floating.

## CML OUTPUTS DC ELECTRICAL CHARACTERISTICS

$V_{CCO} = 1.14\text{V}$  to  $1.26\text{V}$ ,  $R_L = 50\Omega$  to  $V_{CCO}$ ,

$V_{CCO} = 1.7\text{V}$  to  $1.9\text{V}$ ,  $2.375\text{V}$  to  $2.625\text{V}$ ,  $R_L = 50\Omega$  to  $V_{CCO}$  or  $100\Omega$  across the outputs,

$V_{CC} = 2.375\text{V}$  to  $2.625\text{V}$ .  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise stated.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Output HIGH Voltage	$V_{OH}$	$V_{CCO} - 0.020$	$V_{CCO} - 0.010$	$V_{CCO}$	V	$R_L = 50\Omega$ to $V_{CCO}$
Output Voltage Swing	$V_{OUT}$	300	390	475	mV	See Figure 5-1
Differential Output Voltage Swing	$V_{DIFF\_OUT}$	600	780	950	mV	See Figure 5-2
Output Source Impedance	$R_{OUT}$	45	50	55	$\Omega$	—

## THREE LEVEL EQ INPUT DC ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Characteristics:  $V_{CC} = 2.375V$  to  $2.625V$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise indicated,

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Input High Voltage	$V_{IH}$	$V_{CC} - 0.3$	—	—	V	—
Input Low Voltage	$V_{IL}$	0	—	$V_{EE} + 0.3$	V	—
Input High Current	$I_{IH}$	—	—	400	$\mu A$	$V_{IH} = V_{CC}$
Input Low Current	$I_{IL}$	-480	—	—	$\mu A$	$V_{IL} = GND$

**Note 1:** The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

## AC ELECTRICAL CHARACTERISTICS

$V_{CCO} = 1.14V$  to  $1.26V$ ,  $R_L = 50\Omega$  to  $V_{CCO}$ ,

$V_{CCO} = 1.7V$  to  $1.9V$ ,  $2.375V$  to  $2.625V$ ,  $R_L = 50\Omega$  to  $V_{CCO}$  or  $100\Omega$  across the outputs,

$V_{CC} = 2.375V$  to  $2.625V$ .  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise stated.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Maximum Frequency	$f_{MAX}$	6.4	—	—	Gbps	NRZ Data
		4.5	—	—	GHz	$V_{OUT} > 200$ mV, Clock
Propagation Delay IN-to-Q	$t_{PD}$	100	180	280	ps	(Note 1), Figure 4-1
Within Device Skew	$t_{SKEW}$	—	3	15	ps	(Note 2)
Part-to-Part Skew		—	—	100	ps	(Note 3)
Random Jitter	$t_{JITTER}$	—	—	1	$ps_{RMS}$	—
Output Rise/Fall Times (20% to 80%)	$t_r, t_f$	20	50	80	ps	At full output swing.

**Note 1:** Propagation delay is measured with no attenuating transmission line connected to the input.

**2:** Within device skew is measured between two different outputs under identical input transitions

**3:** Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.

**4:** Random jitter is measured with a K28.7 pattern, measured at  $\leq f_{MAX}$ .

# SY56011R

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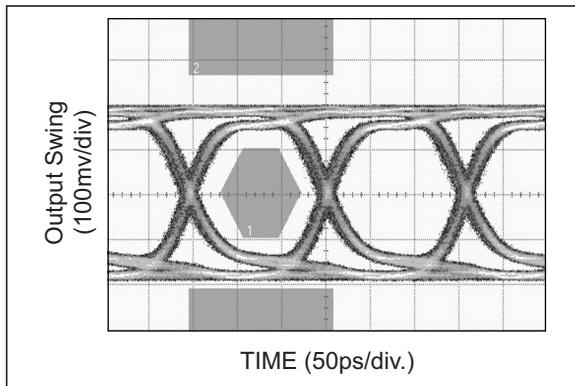
## TEMPERATURE SPECIFICATIONS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
<b>Temperature Ranges</b>						
Maximum Operating Junction Temperature	$T_A$	-40	—	+125	°C	—
Storage Temperature	$T_S$	-65	—	+150	°C	—
Lead Temperature	$T_{LEAD}$	—	—	+260	°C	Soldering, 20 sec.
Ambient Temperature	$T_A$	-40	—	+85	°C	—
<b>Package Thermal Resistance (QFN)</b>						
Junction-to-Ambient	$\theta_{JA}$	—	60	—	°C/W	Still Air
		—	54	—		500 lfpm
Junction-to-Board	$\Psi_{JB}$	—	33	—	°C/W	—

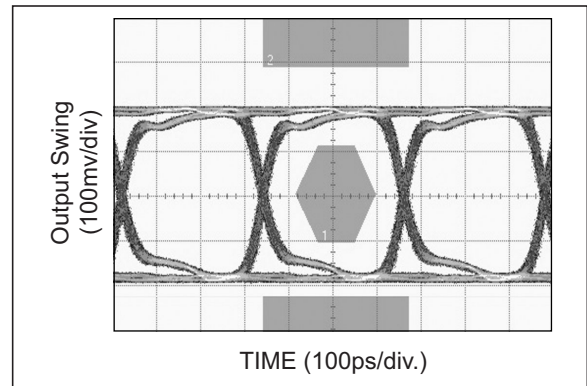
## 2.0 TYPICAL OPERATING CHARACTERISTICS

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

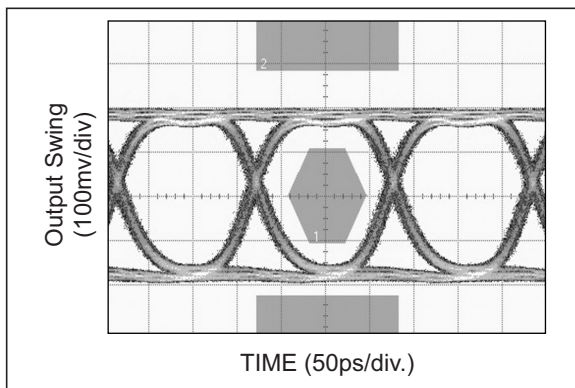
$V_{CC} = 2.5V$ ,  $V_{CCO} = 1.2V$ ,  $GND = 0V$ ,  $V_{IN} = 400\text{ mV}$ ;  $R_L = 50\Omega$  to  $1.2V$ ; Data Pattern:  $2^{23}-1$ ,  $T_A = +25^\circ\text{C}$ , unless otherwise stated.



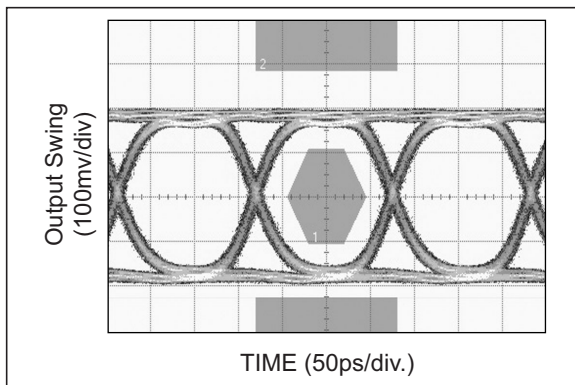
**FIGURE 2-1:** 6.4 Gbps, 24 Inch FR4.



**FIGURE 2-4:** 3.2 Gbps, 24 Inch FR4.



**FIGURE 2-2:** 6.4 Gbps, 18 Inch FR4.



**FIGURE 2-3:** 6.4 Gbps, 9 Inch FR4.

# SY56011R

## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

**TABLE 3-1: PIN FUNCTION TABLE**

Pin Number	Symbol	Description
1, 2	IN, /IN	Differential Input: Signals as small as 200 mV <sub>PK</sub> (400 mV <sub>PP</sub> ) applied to the input of 9, 18, or 27 inches 6 mm FR4 stripline transmission line are then terminated with this differential input. Each input pin internally terminates with 50Ω to the VT pin.
3	VT	Input Termination Center Tap: Each side of the differential input pair terminates to VT pin. This pin provides a center tap to a termination network for maximum interface flexibility. An internal high impedance resistor divider biases VT to allow input AC-coupling. For AC-coupling, bypass VT with 0.1 μF low ESR capacitor to VCC. See <a href="#">Section 7.0, Input Interface Applications</a> .
6	EQ	Three level input for equalization control. High, float, low. See <a href="#">Table 3-2</a>
7	VCC	Positive Power Supply: Bypass with 0.1 μF//0.01 μF low ESR capacitors as close to the VCC pin as possible. Supplies input and core circuitry.
8, 13	VCCO	Output Supply: Bypass with 0.1 μF//0.01 μF low ESR capacitors as close to the VCCO pins as possible. Supplies the output buffers.
14	GND, ePAD	Ground: Exposed pad must be connected to a ground plane that is the same potential as the ground pins.
10, 9 11, 12	/Q1, Q1 /Q0, Q0	CML Differential Output Pairs: Differential buffered copies of the input signal. The output swing is typically 390 mV. See <a href="#">Section 8.0, CML Output Termination</a> for termination information.
4, 5, 15, 16	NC	No connect pins.

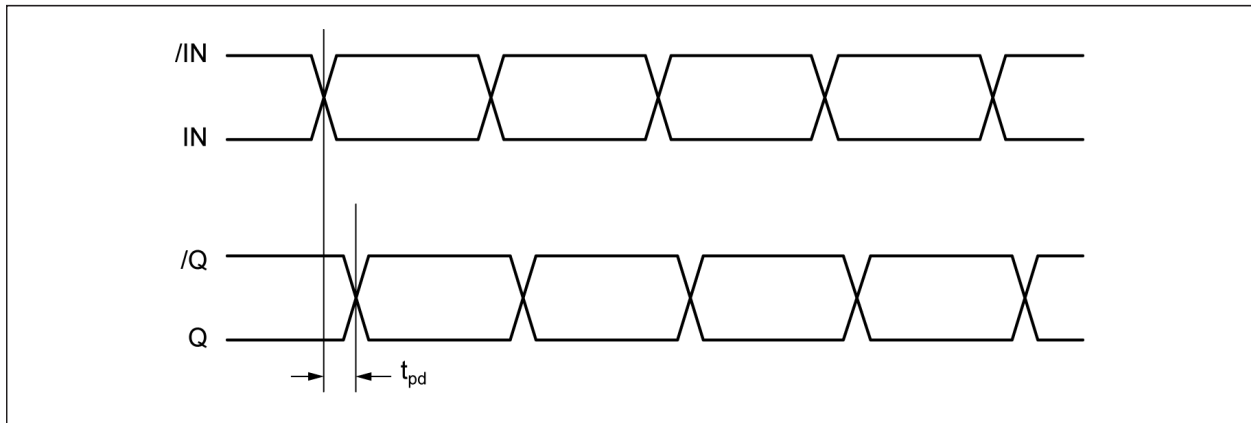
## 3.1 Truth Table

**TABLE 3-2: EQ TRUTH TABLE**

EQ	Equalization FR4 6 mm Stripline
Low	9 Inches
Float	18 Inches
High	27 Inches

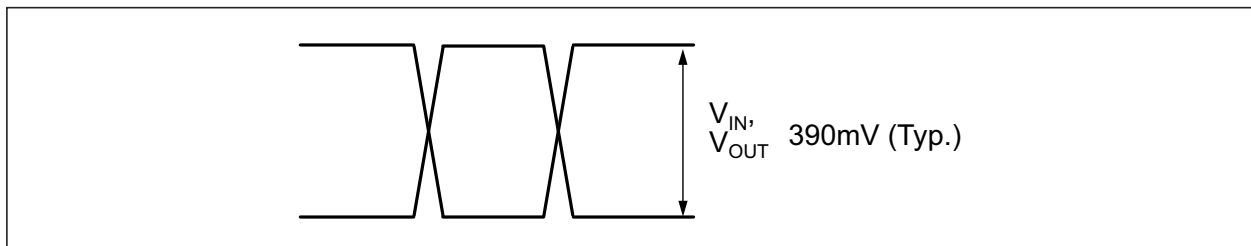


## 4.0 TIMING DIAGRAM

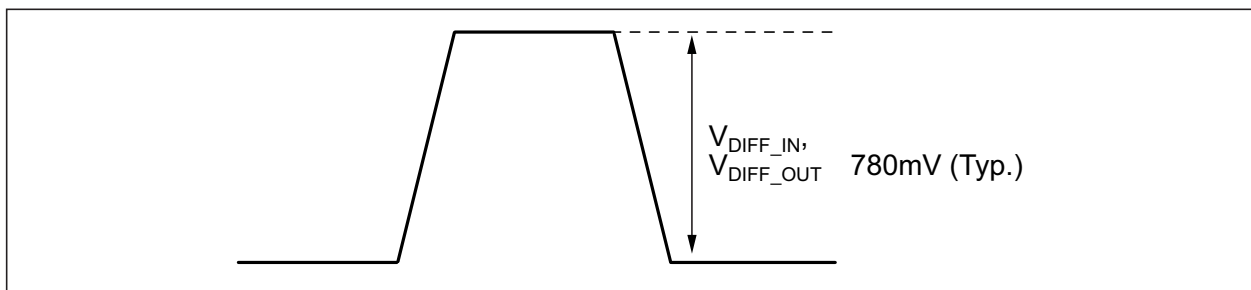


**FIGURE 4-1:** Propagation Delay.

## 5.0 INPUT AND OUTPUT SWING DEFINITIONS

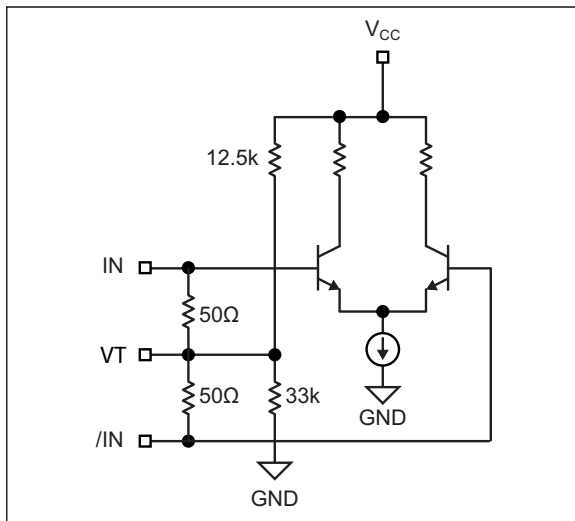


**FIGURE 5-1:** *Single-Ended Swing.*

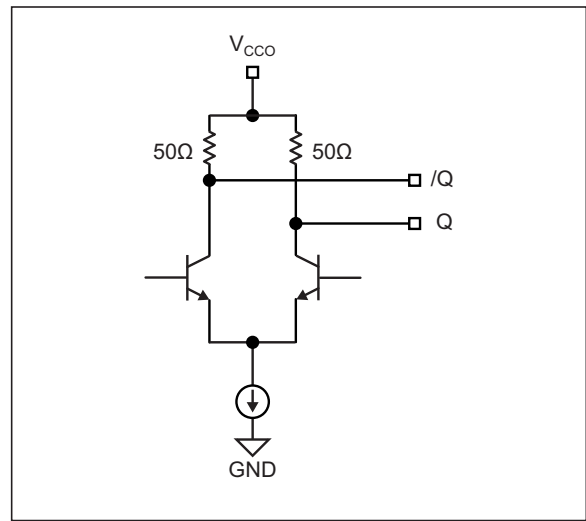


**FIGURE 5-2:** *Differential Swing.*

## 6.0 INPUT AND OUTPUT STRUCTURES



**FIGURE 6-1:** Simplified Differential Input Buffer.



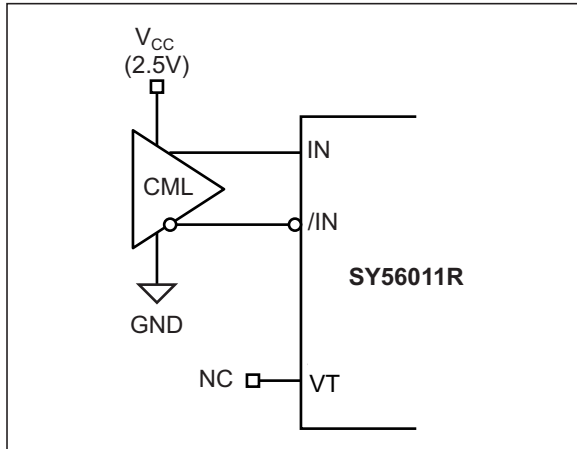
**FIGURE 6-2:** Simplified CML Output Buffer.

# SY56011R

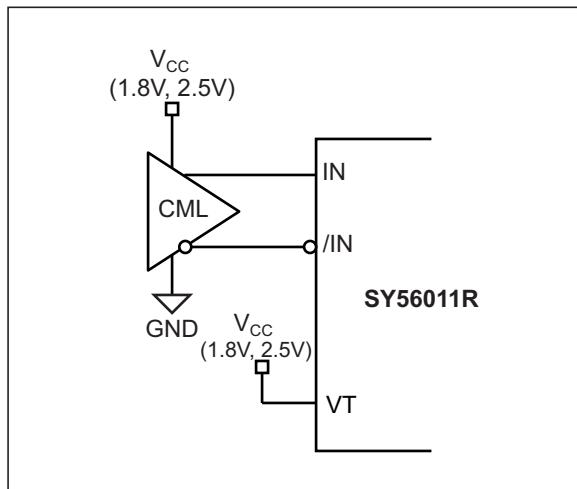
## 7.0 INPUT INTERFACE APPLICATIONS

1.8V CML driver: Terminate input with VT tied to 1.8V. Don't terminate 100Ω differentially.

2.5V CML driver: Terminate input with either VT tied to 2.5V or 100Ω differentially.

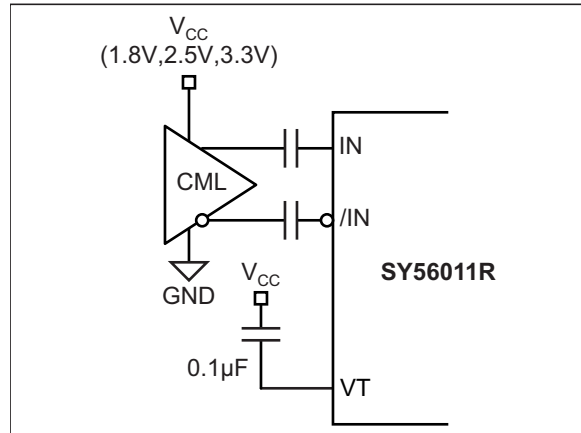


**FIGURE 7-1:** CML Interface 100Ω Differential (DC-Coupled, 2.5V).

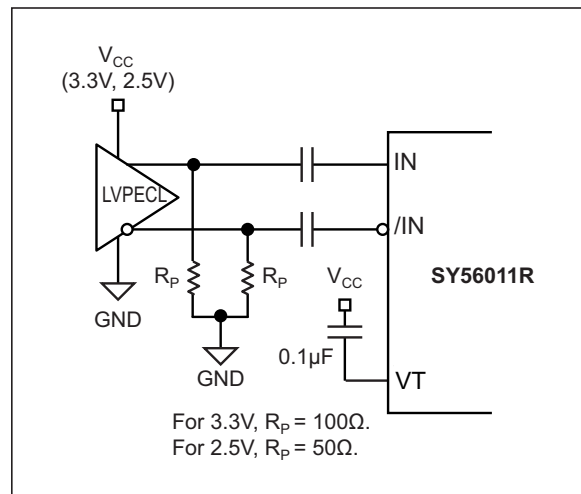


**FIGURE 7-2:** CML Interface 50Ω to VCC (DC-Coupled, 1.8V, 2.5V).

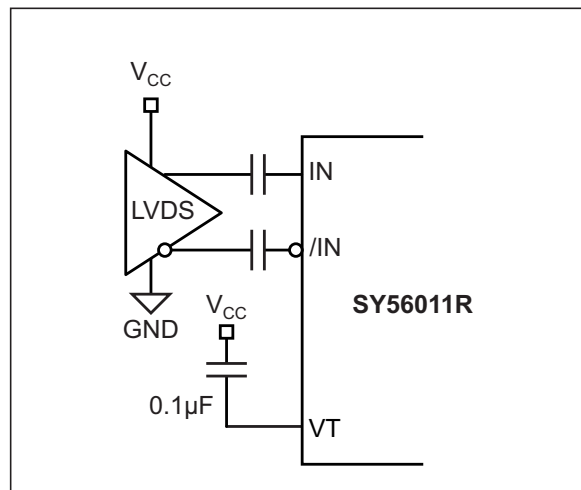
**Note:** The input cannot be DC-coupled from an 1.2V CML driver.



**FIGURE 7-3:** CML Interface (AC-Coupled).



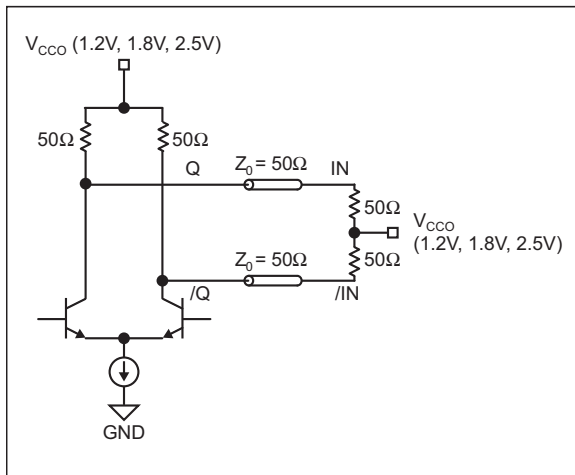
**FIGURE 7-4:** LVPECL Interface (AC-Coupled).



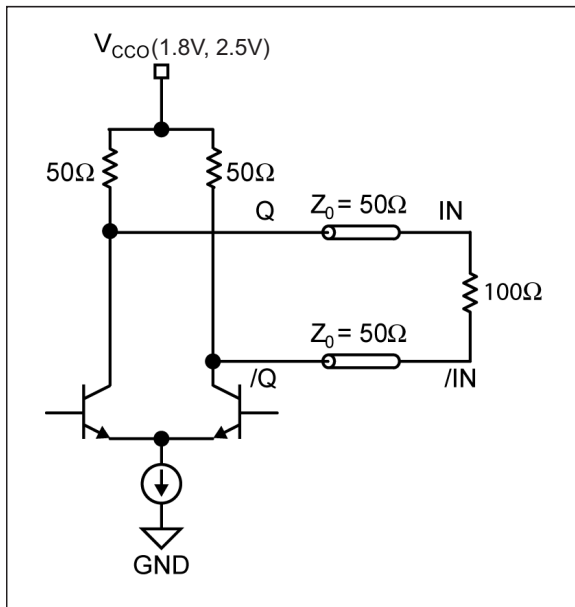
**FIGURE 7-5:** LVDS Interface (AC Coupled).

## 8.0 CML OUTPUT TERMINATION

For  $V_{CCO}$  of 1.2V, **Figure 8-1**, terminate the output with 50Ω to 1.2V, not 100Ω differentially across the outputs. If AC-coupling is used, **Figure 8-4**, terminate into 50 ohms to 1.2V before the coupling capacitor and then connect to a high value resistor to a reference voltage. Any unused output pair needs to be terminated, do not leave floating.

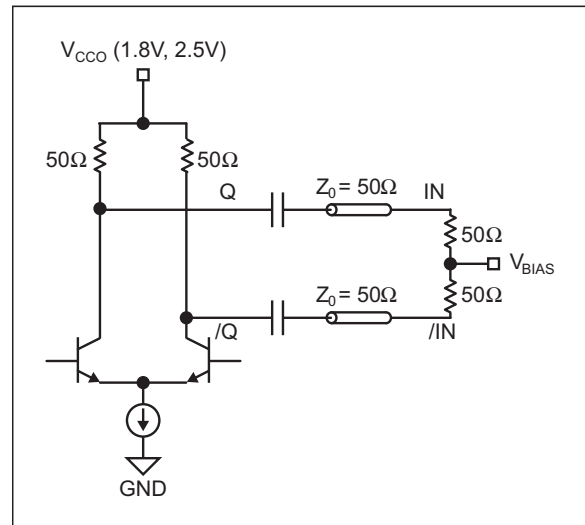


**FIGURE 8-1:** 1.2V, 1.8V, 2.5V CML DC-Coupled Termination.

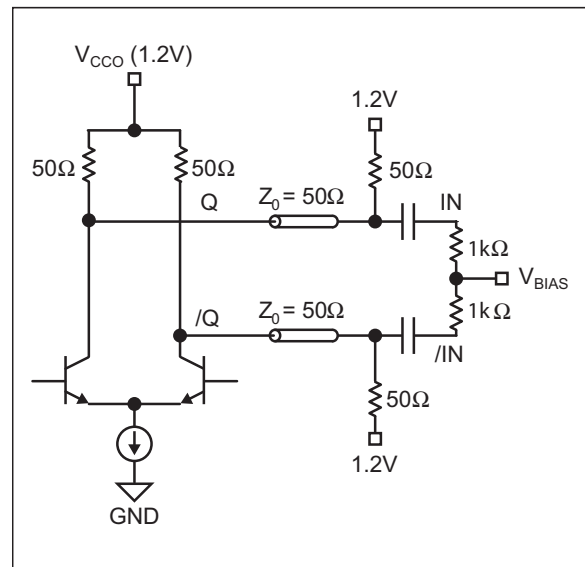


**FIGURE 8-2:** CML DC-Coupled Termination ( $V_{CCO}$  1.8V or 2.5V Only).

For  $V_{CCO}$  of 1.8V or 2.5V, **Figure 8-1** and **Figure 8-2**, terminate either with 50Ω to  $V_{CCO}$  or 100Ω across the outputs. AC-or DC-coupling is fine. For best signal integrity, terminate any unused output pair.



**FIGURE 8-3:** CML AC-Coupled Termination ( $V_{CCO}$  1.8V or 2.5V Only).



**FIGURE 8-4:** CML AC-Coupled Termination ( $V_{CCO}$  1.2V Only).

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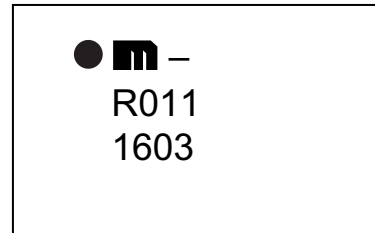
## 9.0 PACKAGING INFORMATION

### 9.1 Package Marking Information

16-Lead QFN\*



Example

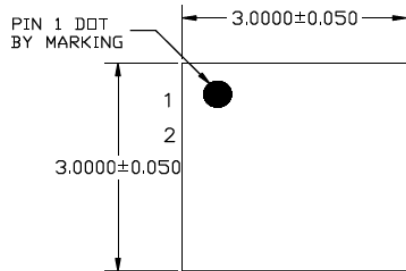


<b>Legend:</b>	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (¯) and/or Overbar (˘) symbol may not be to scale.	

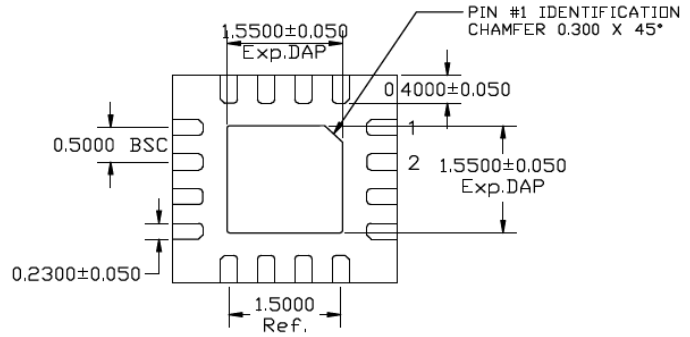
**TITLE**

16 LEAD QFN 3x3mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

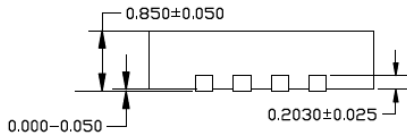
DRAWING #	QFN33-16LD-PL-1	UNIT	MM
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TOP VIEW  
NOTE: 1, 2, 3



BOTTOM VIEW  
NOTE: 1, 2, 3



SIDE VIEW  
NOTE: 1, 2, 3

**NOTE:**

1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076 MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35 MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60 MM IN SIZE, 0.20 MM SPACING.

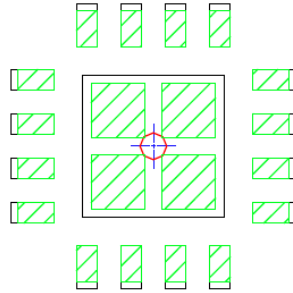
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

# SY56011R

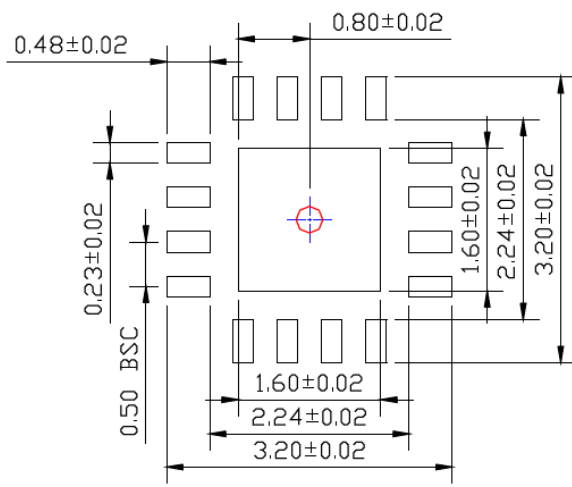
POD-Land Pattern drawing # QFN33-16LD-PL-1

## RECOMMENDED LAND PATTERN

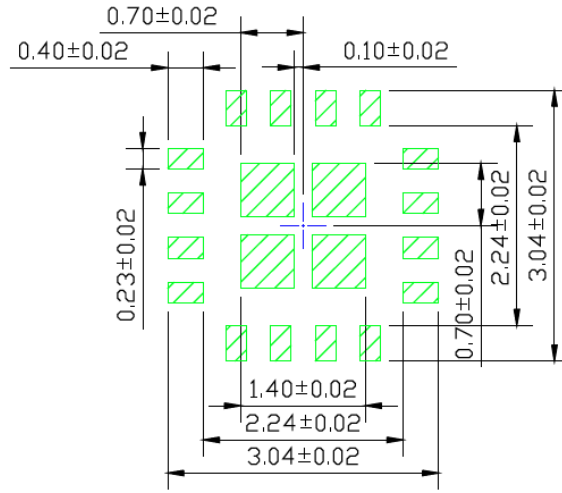
NOTE: 4, 5



STACKED-UP



EXPOSED METAL TRACE



SOLDER STENCIL OPENING

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.



## APPENDIX A: REVISION HISTORY

### Revision A (March 2019)

- Converted to Micrel data sheet SY56011R to Microchip data sheet template DS20006167A.
- Minor text changes throughout.

# SY56011R

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NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	X	X	X	-XX
Device	Output Voltage Option	Package	Temperature Range	Media Type
<b>Device:</b>	SY56011:	Low-Voltage 1.2V/1.8V/2.5V CML 1:2 Fanout Buffer, 6.4 Gbps, with Equalization		
<b>Output Voltage Option:</b>	R =	1.2V/1.8V/2.5V		
<b>Package:</b>	M =	16-Lead 3 mm x 3 mm QFN		
<b>Temperature Range:</b>	G =	-40°C to +85°C (NiPdAu Pb-Free)		
<b>Media Type:</b>	<blank> =	100/Tube		
	TR =	1,000/Reel		

<b>Examples:</b>	
a) SY56011RMG:	1.2V, 1.8V, and 2.5V Output Voltage, 16-Lead 3 mm x 3 mm QFN, -40°C to +85°C, 100/Tube
b) SY56011RMG-TR:	1.2V, 1.8V, and 2.5V Output Voltage, 16-Lead 3 mm x 3 mm QFN, -40°C to +85°C, 1,000/Reel

<b>Note 1:</b>	Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package.
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NOTES:

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**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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