# PL138-48

## 2.5V to 3.3V, Low-Skew, 1:4 Differential PECL Fanout Buffer

### Features

- Four Differential 2.5V/3.3V LVPECL Output Pairs
- Output Frequency: ≤800 MHz
- Two Selectable Differential Input Pairs
- Translates Any Standard Single-Ended or Differential Input Format to LVPECL Output. It Can Accept the Following Standard Input Formats and More:
  - LVPECL, LVCMOS, LVDS, HCSL, SSTL, LVHSTL, CML
- Output Skew: 25 ps (typ.)
- Part-to-Part Skew: 140 ps (typ.)
- Propagation Delay: 1.5 ns (typ.)
- Additive Jitter: <100 fs (max.)
- Operating Supply Voltage: 2.375V ~ 3.63V
- Operating Temperature Range from –40˚C to +85˚C
- Package Availability: 16-Pin QFN and 20-Pin TSSOP

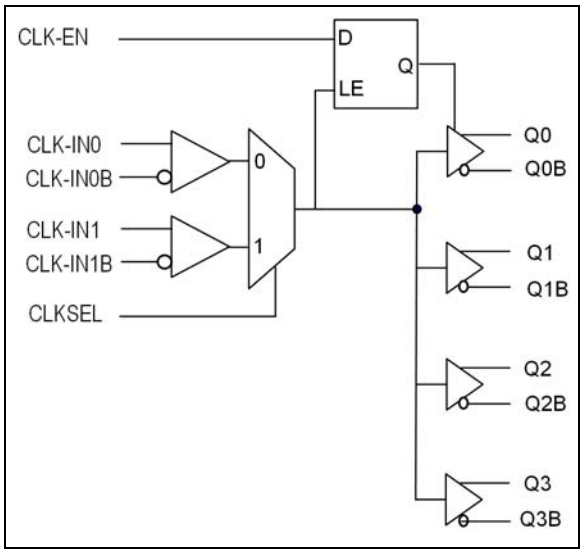
### General Description

The PL138-48 is a high performance low-cost 1:4 outputs differential LVPECL fanout buffer.

Microchip's family of differential LVPECL buffers are designed to operate from a single power supply of 2.5V ±5% or 3.3V ±10%. The differential input pairs are designed to accept most standard input signal levels, using an appropriate resistor bias network, and produce a high quality set of outputs with the lowest possible skew on the outputs, which is guaranteed for part-to-part or lot-to-lot skew.

Designed to fit in a small form-factor package, the PL138-48 offers up to 800 MHz of output operation with very low-power consumption and lowest additive jitter of any comparable device.

### Block Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Supply Voltage ($V_{DD}$) .....+4.6V
Input Voltage, DC ($V_I$).....–0.5V to $V_{DD}$+0.5V
Output Voltage, DC ($V_O$) .....–0.5V to $V_{DD}$+0.5V
ESD Protection (HBM) .....2 kV

**† Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

Specifications: $V_{CC}$ = 3.3V; $V_{EE}$ = 0V. Input and output parameters vary 1:1 with $V_{CC}$ when $V_{CC}$ varies ±10%.

| Parameters | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Output High Voltage, (Note 1) | $V_{OH}$ | 2.215 | 2.320 | 2.420 | V | At –40°C |
| | | 2.275 | 2.350 | 2.420 | | At +25°C |
| | | 2.275 | 2.350 | 2.420 | | At +85°C |
| Output Voltage Low, (Note 1) | $V_{OL}$ | 1.470 | 1.610 | 1.745 | V | At –40°C |
| | | 1.490 | 1.585 | 1.680 | | At +25°C |
| | | 1.490 | 1.585 | 1.680 | | At +85°C |
| Input High Voltage | $V_{IH}$ | 2.075 | — | 2.420 | V | At –40°C |
| | | 2.135 | — | 2.420 | | At +25°C |
| | | 2.135 | — | 2.420 | | At +85°C |
| Input Low Voltage | $V_{IL}$ | 1.470 | — | 1.890 | V | At –40°C |
| | | 1.490 | — | 1.825 | | At +25°C |
| | | 1.490 | — | 1.825 | | At +85°C |
| Output Voltage Reference, (Note 2) | $V_{BB}$ | 1.86 | — | 1.98 | V | At –40°C |
| | | 1.92 | — | 2.04 | | At +25°C |
| | | 1.92 | — | 2.04 | | At +85°C |
| Input High Voltage Common Mode Range, (Note 3, Note 4) | $V_{CMR}$ | 1.2 | — | 3.3 | V | At –40°C |
| | | 1.2 | — | 3.3 | | At +25°C |
| | | 1.2 | — | 3.3 | | At +85°C |
| Input High Current, (Note 5) | $I_{IH}$ | — | — | 75 | µA | At –40°C |
| | | — | — | 75 | | At +25°C |
| | | — | — | 75 | | At +85°C |
| Input Low Current, (Note 5) | $I_{IL}$ | –75 | — | — | µA | At –40°C |
| | | –75 | — | — | | At +25°C |
| | | –75 | — | — | | At +85°C |

**Note 1:** Outputs terminated with 50Ω to $V_{CCO}$–2V.
**2:** Single-ended input operation is limited to VCC ≥ 3V in LVPECL mode.
**3:** Common mode voltage is defined as $V_{IH}$.
**4:** For single-ended applications, the maximum input voltage for CLK-INx, CLK-INxB is $V_{CC}$+0.3V.
**5:** CLK-IN0, CLK-IN1; CLK-IN0B, CLK-IN1B.

## DC ELECTRICAL CHARACTERISTICS

Specifications: $V_{CC}$ = 2.5V; $V_{EE}$ = 0V. Input and output parameters vary 1:1 with $V_{CC}$ when $V_{CC}$ varies ±5%.

| Parameters | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Output High Voltage, (Note 1) | $V_{OH}$ | 1.415 | 1.520 | 1.620 | V | At –40°C |
| | | 1.475 | 1.550 | 1.620 | | At +25°C |
| | | 1.475 | 1.550 | 1.620 | | At +85°C |
| Output Voltage Low, (Note 1) | $V_{OL}$ | 0.670 | 0.810 | 0.945 | V | At –40°C |
| | | 0.690 | 0.785 | 0.880 | | At +25°C |
| | | 0.690 | 0.785 | 0.880 | | At +85°C |
| Input High Voltage | $V_{IH}$ | 1.275 | — | 1.620 | V | At –40°C |
| | | 1.335 | — | 1.620 | | At +25°C |
| | | 1.335 | — | 1.620 | | At +85°C |
| Input Low Voltage | $V_{IL}$ | 0.670 | — | 1.090 | V | At –40°C |
| | | 0.690 | — | 1.025 | | At +25°C |
| | | 0.690 | — | 1.025 | | At +85°C |
| Input High Voltage Common Mode Range, (Note 2, Note 3) | $V_{CMR}$ | 1.2 | — | 2.5 | V | At –40°C |
| | | 1.2 | — | 2.5 | | At +25°C |
| | | 1.2 | — | 2.5 | | At +85°C |
| Input High Current, (Note 4) | $I_{IH}$ | — | — | 60 | µA | At –40°C |
| | | — | — | 60 | | At +25°C |
| | | — | — | 60 | | At +85°C |
| Input Low Current, (Note 4) | $I_{IL}$ | –60 | — | — | µA | At –40°C |
| | | –60 | — | — | | At +25°C |
| | | –60 | — | — | | At +85°C |

**Note 1:** Outputs terminated with 50Ω to $V_{CCO}$–2V.

**2:** Common mode voltage is defined as $V_{IH}$.

**3:** For single-ended applications, the maximum input voltage for CLK-INx, CLK-INxB is $V_{CC}$+0.3V.

**4:** CLK-IN0, CLK-IN1; CLK-IN0B, CLK-IN1B.

## AC ELECTRICAL CHARACTERISTICS

$V_{CC}$ = –3.8V to –2.375 or $V_{CC}$ = 2.375V to 3.8V; $V_{EE}$ = 0V; $T_A$ = –40°C to +85°C. All parameters are measured at f ≤ 800 MHz unless otherwise noted.

| Parameters | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Output Frequency | $f_{MAX}$ | — | — | 800 | MHz | At all temperatures |
| Propagation Delay, (Note 1) | $t_{PD}$ | 600 | 680 | 750 | ps | At –40°C |
| | | 650 | 725 | 790 | | At +25°C |
| | | 690 | 790 | 890 | | At +85°C |
| Output Skew, (Note 2, Note 4) | $t_{SK(O)}$ | — | 25 | 37 | ps | At all temperatures |
| Part-to-Part Skew, (Note 3, Note 4) | $t_{SK(PP)}$ | — | 85 | 225 | ps | At all temperatures |
| Buffer Additive Phase Jitter, RMS | $t_{APJ}$ | — | — | 0.10 | ps | At all temperatures; refer to Noise Characteristics section |
| Peak-to-Peak Input Voltage (Differential Configuration) | $V_{PP}$ | 150 | 800 | 1200 | mV | At all temperatures |
| Peak-to-Peak Output Voltage | $V_{SWING}$ | 470 | 800 | 950 | mV | At –40°C |
| | | 600 | 800 | 930 | | At +25°C |
| | | 600 | 800 | 930 | | At +85°C |
| Output Rise/Fall Time | $t_R/t_F$ | 200 | — | 550 | ps | At all temperatures; 20% to 80% at full output swing. |

**Note 1:** Measured from the differential input crossing point to the differential output crossing point.

**2:** Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

**3:** Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

**4:** This parameter is defined in accordance with JEDEC Standard 65.

## TEMPERATURE SPECIFICATIONS (Note 1)

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Temperature Ranges** | | | | | | |
| Ambient Operating Temperature | $T_A$ | –40 | — | +85 | °C | Note 2 |
| Junction Temperature | $T_J$ | — | — | +110 | °C | — |
| Storage Temperature Range | $T_S$ | –65 | — | +150 | °C | — |
| Soldering Temperature | — | — | — | +260 | °C | 10 sec. |

**Note 1:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature, and the thermal resistance from junction to air (i.e., $T_A$, $T_J$, $\theta_{JA}$). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

**2:** Operating temperature is guaranteed by design for all parts (commercial and industrial), but tested for commercial grade only.

## 2.0 PIN DESCRIPTIONS

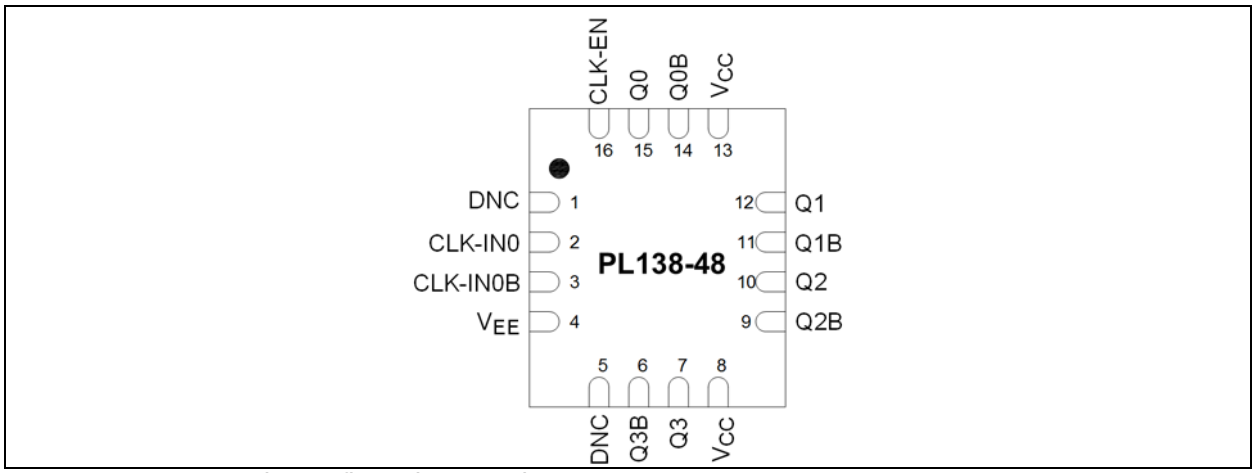



***FIGURE 2-1:*** *Pin Configuration, 16-Pin QFN.*

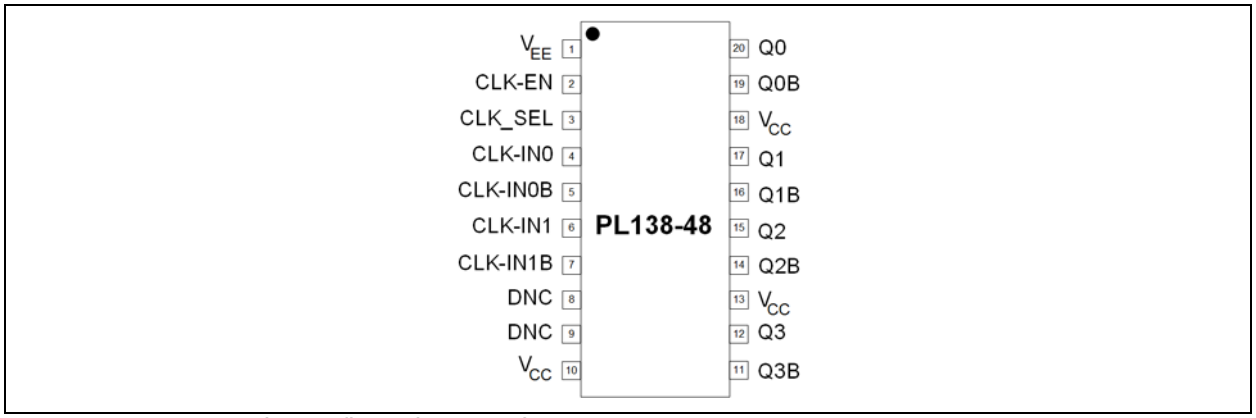



***FIGURE 2-2:*** *Pin Configuration, 20-Pin TSSOP.*

The descriptions of the pins are listed in Table 2-1.

**TABLE 2-1: PIN FUNCTION TABLE**

| Pin Number QFN-16 | Pin Number TSSOP-20 | Pin Name | Type | Description |
|---|---|---|---|---|
| 4 | 1 | $V_{EE}$ | P | Power supply pin connection. |
| 16 | 2 | CLK-EN | I | Synchronizing clock enable.<br>When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced low, QB outputs are forced high.<br>LVTTL/LVCMOS interface levels.<br>50 kΩ internal pull-up resistor. |
| — | 3 | CLK-SEL | I | Clock select input. When HIGH, selects CLK1 input. When LOW, selects CLK0 input.<br>LVTTL/LVCMOS interface levels.<br>50 kΩ internal pull-down resistor. |
| 2 | 4 | CLK-IN0 | I | True part of differential clock input signal. 75 kΩ internal pull-down resistor. |
| 3 | 5 | CLK-IN0B | I | Complementary part of differential clock input signal.<br>100 kΩ internal pull-up and pull-down resistors. |

**TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)**

| Pin Number QFN-16 | Pin Number TSSOP-20 | Pin Name | Type | Description |
|---|---|---|---|---|
| — | 6 | CLK-IN1 | I | True part of differential clock input signal. 75 kΩ internal pull-down resistor. |
| — | 7 | CLK-IN1B | I | Complementary part of differential clock input signal. 100 kΩ internal pull-up and pull-down resistors. |
| 1, 5 | 8, 9 | DNC | — | Do Not Connect. |
| 8, 13 | 10, 13, 18 | $V_{CC}$ | P | Power supply pin connection. |
| 6, 9, 11 ,14 | 11, 14, 16, 19 | QB0 ~ QB3 | O | LVPECL Complementary output. |
| 7, 10, 12, 15 | 12, 15, 17, 20 | Q0 ~ Q3 | O | LVPECL True output. |

## 3.0 NOISE CHARACTERISTICS

When a buffer is used to pass a signal, the buffer adds a little bit of its own noise. The phase noise on the output of the buffer will be a little bit more than the phase noise of the input signal. To quantify the noise addition in the buffer we compare the Phase Jitter numbers from the input and the output. The difference is called "Additive Phase Jitter". The formula for the Additive Phase Jitter is as follows:

**EQUATION 3-1:**

$$AdditivePhaseJitter = \sqrt{OutputPhaseJitter^2 - InputPhaseJitter^2}$$

**TABLE 3-1: PL138-48 NOISE CHARACTERISTICS**

| Parameters | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Additive Phase Jitter | $t_{APJ}$ | — | 20 | 40 | fs | $V_{DD}$ = 3.3V, Frequency = 622.08 MHz Offset = 12 kHz ~ 20 MHz |
| | | — | 50 | 100 | | $V_{DD}$ = 3.3V, Frequency = 156.25 MHz Offset = 12 kHz ~ 20 MHz |
| | | — | 50 | 100 | | $V_{DD}$ = 3.3V, Frequency = 50 MHz Offset = 1 kHz ~ 1 MHz |
| | | — | 50 | 100 | | $V_{DD}$ = 3.3V, Frequency = 25 MHz Offset = 1 kHz ~ 1 MHz |

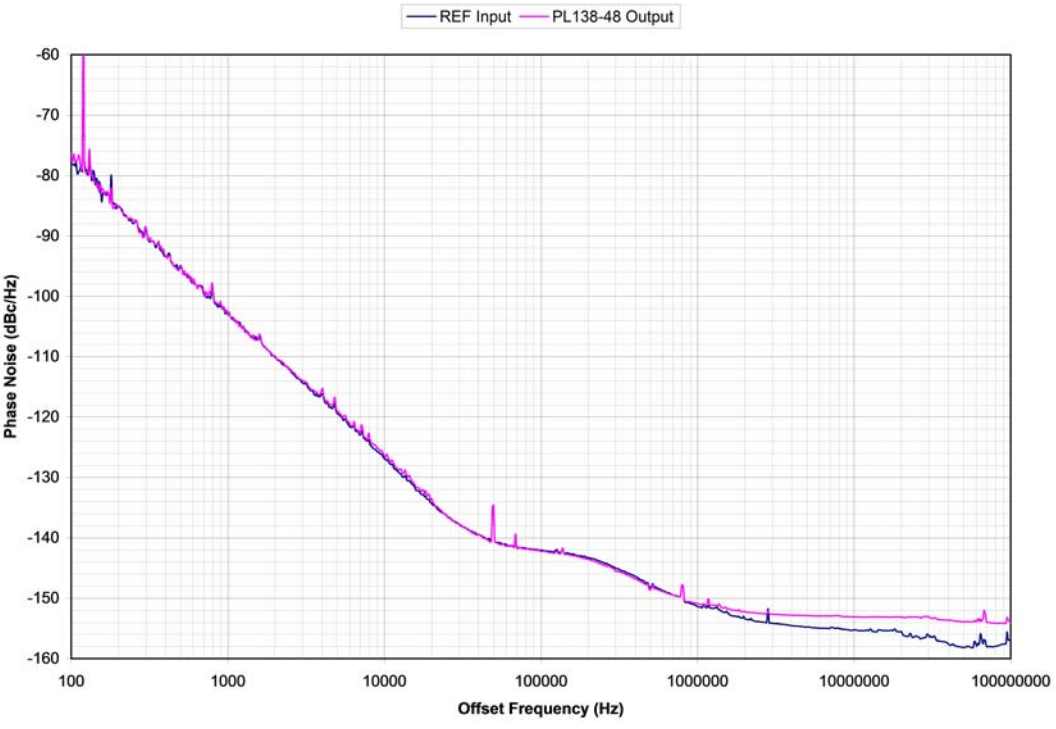



***FIGURE 3-1:*** *PL138-48 Additive Phase Jitter Plot, 622 MHz.*

## 4.0 PARAMETER MEASUREMENT INFORMATION

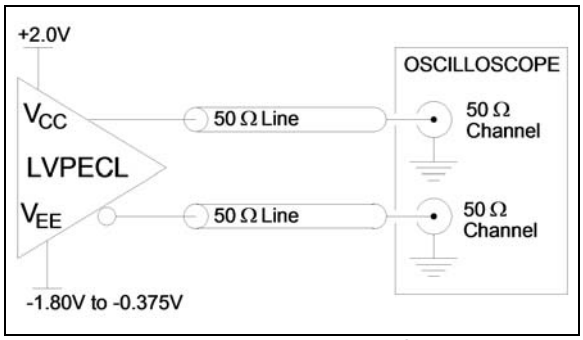



***FIGURE 4-1:*** *Output Waveform Test Circuit.*

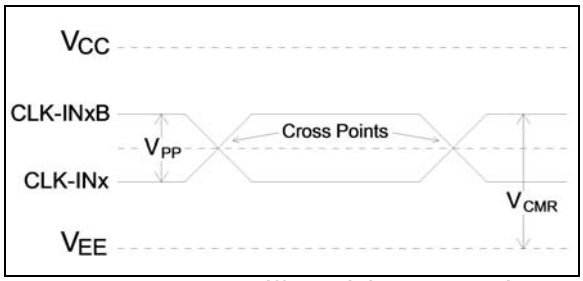



***FIGURE 4-4:*** *Differential Input Level.*

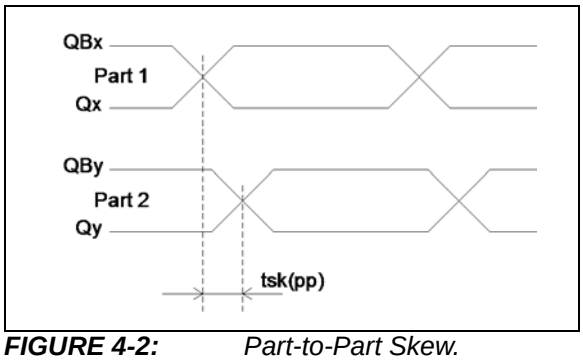



***FIGURE 4-2:*** *Part-to-Part Skew.*

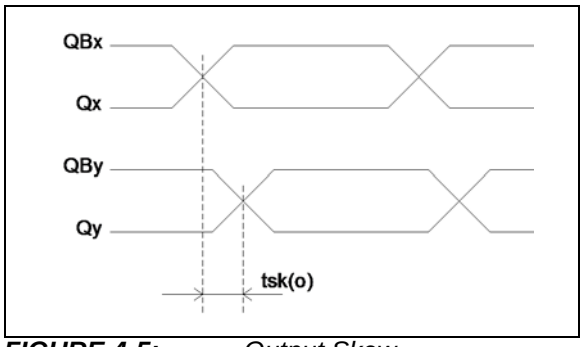



***FIGURE 4-5:*** *Output Skew.*

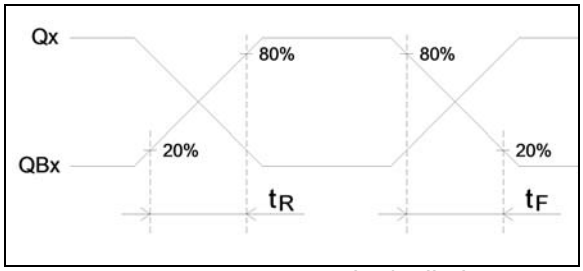



***FIGURE 4-3:*** *Output Rise/Fall Time.*

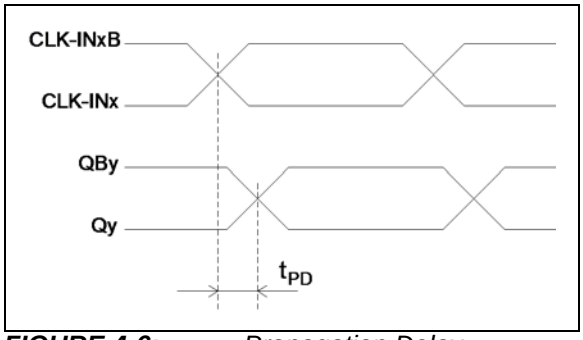



***FIGURE 4-6:*** *Propagation Delay.*

## 5.0 APPLICATION INFORMATION

### 5.1 Input Logic Configurations

The following circuits show different configurations for different input logic type signals. For good signal integrity at the PL138 input, the signals need to be properly terminated according to the logic type requirements. The signals need to be presented at the PL138 input according to $V_{CMR}$, $V_{PP}$, and other input requirements.

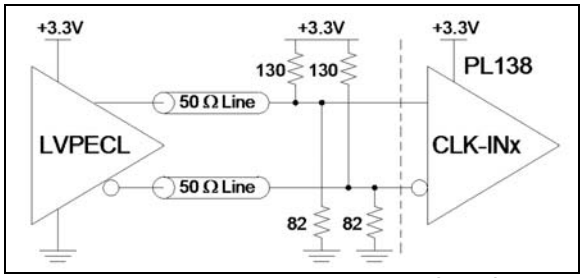



***FIGURE 5-1:*** *CLK-IN Input Driven by a 3.3V LVPECL Driver.*

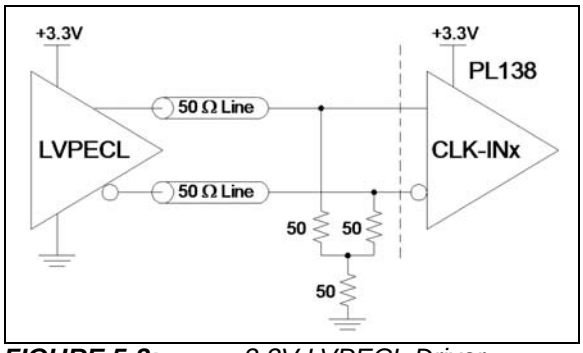



***FIGURE 5-2:*** *3.3V LVPECL Driver, Alternative Termination.*

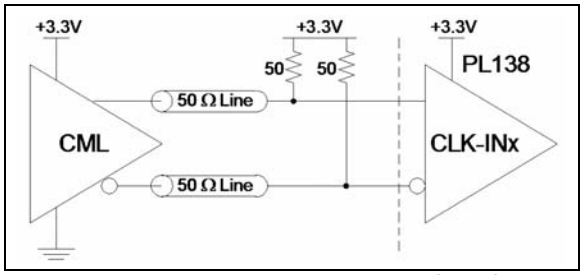



***FIGURE 5-3:*** *CLK-IN Input Driven by a CML Driver.*

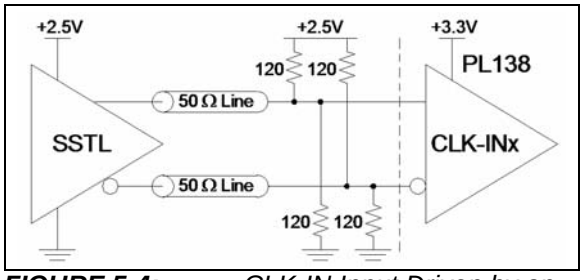



***FIGURE 5-4:*** *CLK-IN Input Driven by an SSTL Driver.*

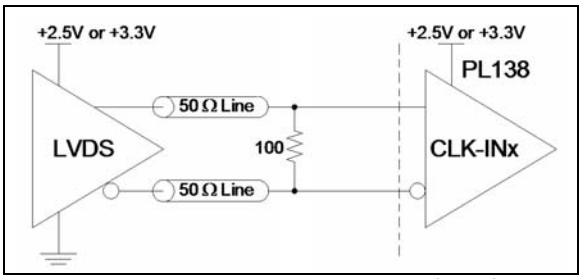



***FIGURE 5-5:*** *CLK-IN Input Driven by an LVDS Driver.*

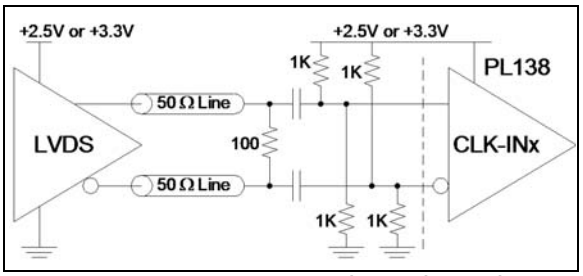



***FIGURE 5-6:*** *LVDS Driver, Alternative AC-Coupling.*

This circuit is for compatibility only. AC-coupling is not really required for LVDS. The $V_{CMR}$ range of the PL138 reaches low enough that LVDS signals can be connected directly to the PL138 input like in the circuit in Figure 5-5.

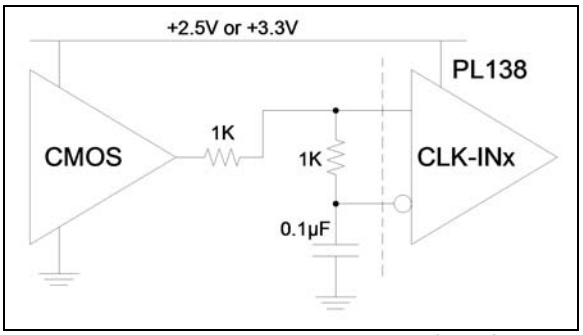



***FIGURE 5-7:*** *CLK-IN Input Driven by a CMOS Driver.*

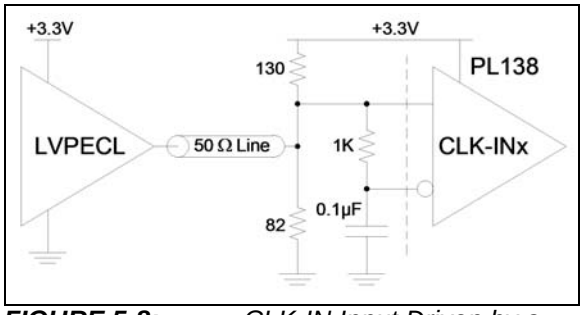



***FIGURE 5-8:*** *CLK-IN Input Driven by a Single-Ended LVPECL.*

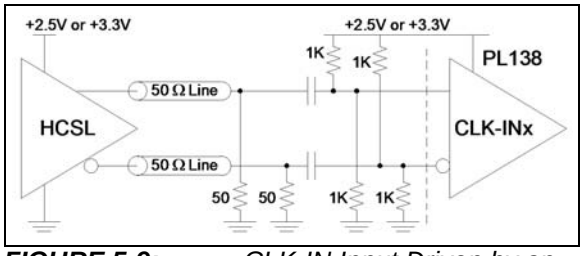



***FIGURE 5-9:*** *CLK-IN Input Driven by an HCSL Driver.*

HCSL presents its signals very close to the ground rail, below the $V_{CMR}$ range, so the HCSL signals cannot be connected to the PL138 input directly. AC-coupling is required for HCSL signals on the PL138 input.

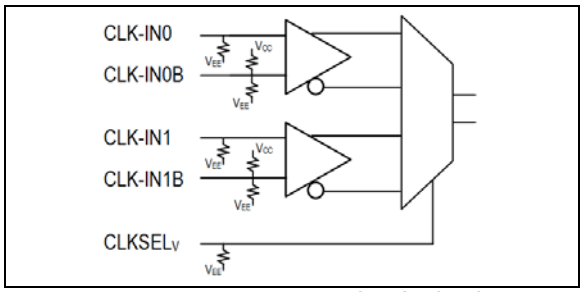



***FIGURE 5-10:*** *Input Logic Block Diagram.*

**TABLE 5-1: INPUT PIN CHARACTERISTICS**

| Input | Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| CLK-IN0, CLK-IN1 | Pull-Down Resistor | — | 75 | — | kΩ |
| CLK-IN0B, CLK_IN1B | Pull-Up & Pull-Down Resistors | — | 100 | — | |
| CLK-EN | Pull-Up Resistor | — | 50 | — | |
| CLKSEL | Pull-Down Resistor | — | 50 | — | |

**TABLE 5-2: INPUT CLOCK CONTROL SELECTION**

| CLK_SEL | Selected Source |
|---|---|
| 0 | CLK-IN0 |
| 1 | CLK-IN1 |

**TABLE 5-3: INPUT CLOCK FUNCTION**

| Inputs | | | Outputs | |
|---|---|---|---|---|
| CLK-EN | CLKSEL | Source | Q0:Q3 | Q0B:Q3B |
| 0 | 0 | CLK-IN0 | Disabled Low | Disabled High |
| 0 | 1 | CLK-IN1 | Disabled Low | Disabled High |
| 1 | 0 | CLK-IN0 | Enabled | Enabled |
| 1 | 1 | CLK-IN1 | Enabled | Enabled |

## 5.2 Termination for LVPECL Outputs

The required termination for LVPECL is 50Ω to a $V_{CC}$-2V DC voltage level. Below are two schematics to implement this termination.

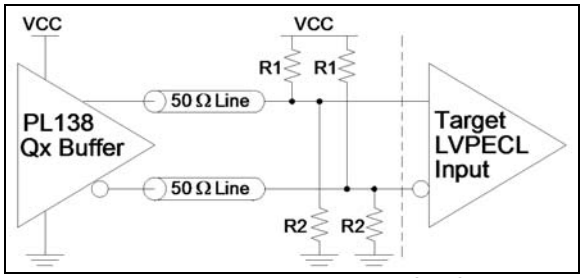



***FIGURE 5-11:*** *LVPECL Termination Schematic #1.*

- $V_{CC}$ = 3.3V
  - Ideal values: R1 = 127Ω, R2 = 82.5Ω
  - Commercial values (E24): R1 = 130Ω, R2 = 82Ω
- $V_{CC}$ = 2.5V
  - Ideal values: R1 = 250Ω, R2 = 62.5Ω
  - Commercial values (E24): R1 = 240Ω, R2 = 62Ω

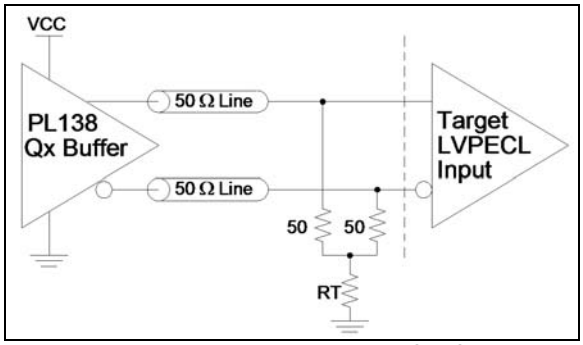



***FIGURE 5-12:*** *LVPECL Termination Schematic #2.*

Schematic #2 is an alternative simplified termination.

- $V_{CC}$ = 3.3V
  - Ideal value: RT = 48.7Ω
  - Commercial value: RT = 50Ω (E24: 51Ω)
- $V_{CC}$ = 2.5V
  - Ideal value: RT = 18.7Ω
  - Commercial value: RT = 18Ω

## 5.3 Power Considerations

Driving LVPECL outputs requires an amount of power that can warm up the chip significantly.

The general requirement for the chip is that the junction temperature should not exceed +110°C.

The power consumption can be divided into two parts:

1. Core power dissipation
2. Output buffer power dissipation

### 5.3.1 CORE POWER DISSIPATION

The chip core power is equal to $V_{CC} \times I_{EE}$. With a worst case $V_{CC}$ and $I_{EE}$, the power dissipation in the core is 3.63V × 45 mA = 163 mW.

### 5.3.2 OUTPUT BUFFER POWER DISSIPATION

The output buffers are not exposed to the full $V_{CC} - V_{EE}$ voltage. On the differential output, one line is at logic 1 with a small voltage across the buffer and a large output current. The other line is at logic 0 with a larger voltage across the buffer and a smaller output current. The power dissipation per output buffer is 32 mW. Only buffers that are loaded will have power dissipation. With all 4 buffers loaded the worst case output buffer power dissipation will be 128 mW.

Total chip power dissipation, worst case, is 163 mW + 128 mW = 291 mW.

### 5.3.3 JUNCTION TEMPERATURE

How much the chip is warmed up from the power dissipation depends upon the thermal resistance from the chip to the environment, also known as “junction to ambient”. The thermal resistance depends upon the type of package, how the package is assembled to the PCB and if there is additional air flow for improved cooling.

**TABLE 5-4: 20-PIN TSSOP THERMAL RESISTANCE**

| Air Flow Velocity in Linear Feet/Minute | $\theta_{JA}$ Value for JEDEC Standard Multi-Layer PCB |
|---|---|
| 0 | 73°C/W |
| 200 | 67°C/W |
| 500 | 64°C/W |

The temperature of the chip (junction) will be higher than the environment (ambient) with an amount equal to $\theta_{JA} \times$ Power. For an ambient temperature of +85°C, all outputs loaded and no air flow, the junction temperature $T_J$ = 85°C + 73 × 0.291 = 106°C.

**TABLE 5-5: 16-PIN QFN THERMAL RESISTANCE**

| Air Flow Velocity in Linear Feet/Minute | $\theta_{JA}$ Value for JEDEC Standard Multi-Layer PCB |
|---|---|
| 0 | 60°C/W |
| 200 | 53°C/W |
| 500 | 46°C/W |

The temperature of the chip (junction) will be higher than the environment (ambient) with an amount equal to $\theta_{JA} \times$ Power. For an ambient temperature of +85°C, all outputs loaded and no air flow, the junction temperature $T_J$ = 85°C + 60 × 0.291 = 102°C.

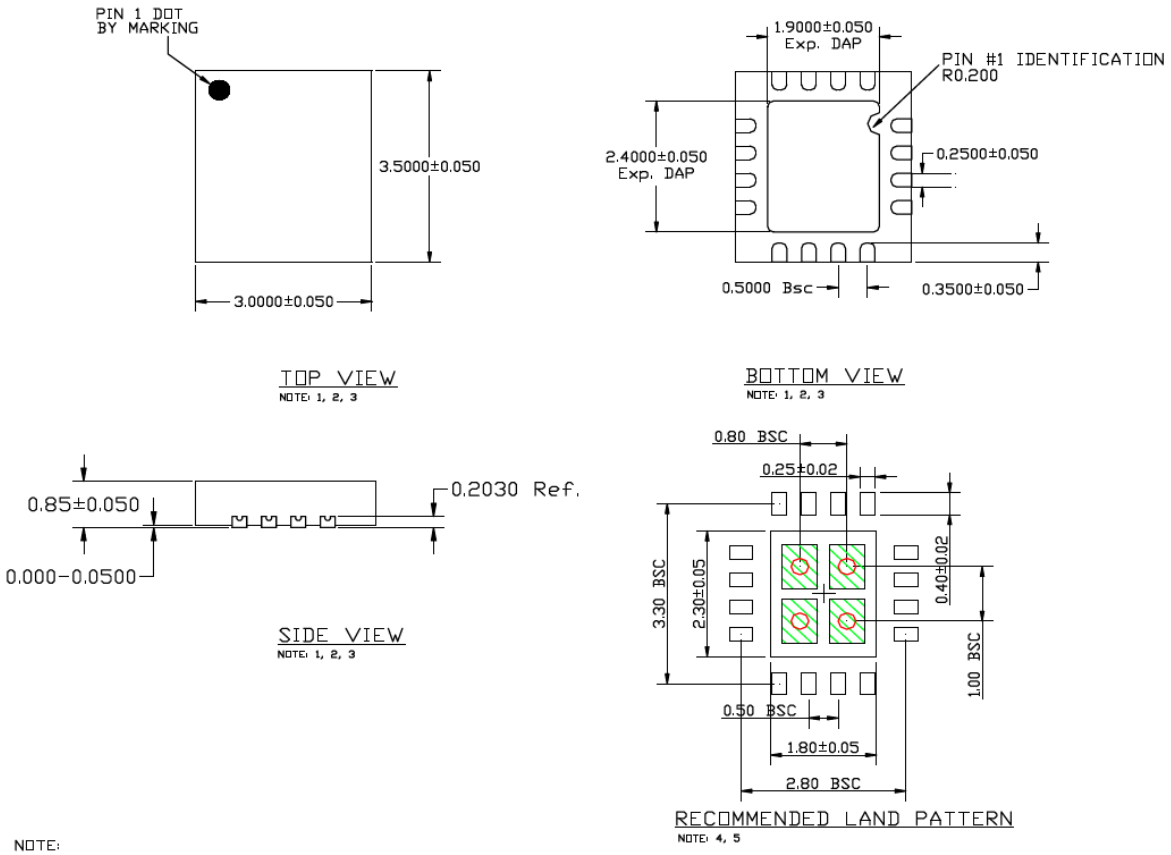
## 6.0 PACKAGE MARKING INFORMATION

### 16-Lead QFN 3.0 mm x 3.5 mm Package Outline and Recommended Land Pattern

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

**TITLE**
16 LEAD QFN 3.0x3.5mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

| DRAWING # | QFN3035-16LD-PL-1 | UNIT | MM |
|---|---|---|---|



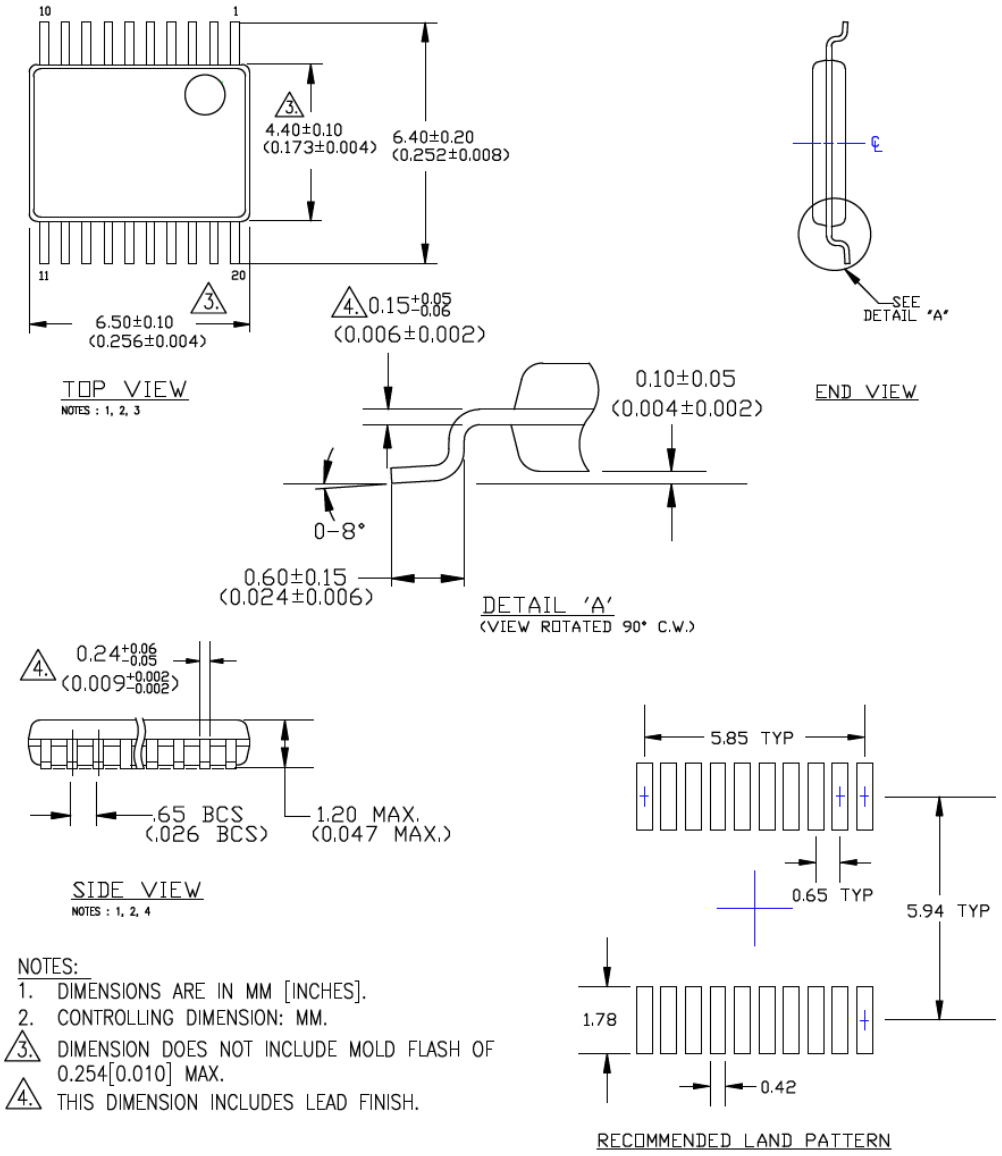

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN REPRESENT THERMAL VIA. RECOMMENDED DIAMETER IS 0.30 - 0.35 MM AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.80x0.60 MM, 0.20 MM SPACING.

## 20-Lead TSSOP Package Outline and Recommended Land Pattern

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

**TITLE**
20 LEAD TSSOP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

| DRAWING # | TSSOP-20LD-PL-1 | UNIT | MM [INCH] |
|---|---|---|---|




NOTES:
1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
4. THIS DIMENSION INCLUDES LEAD FINISH.

## APPENDIX A: REVISION HISTORY

### Revision A (May 2016)

- Converted Micrel data sheet PL138-48 to Microchip DS20005543A.
- Minor text changes throughout.

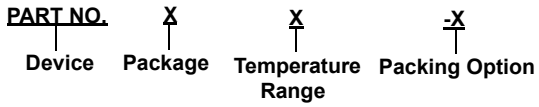
### Revision B (June 2016)

- Updated output frequency tolerances to 800 MHz.

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.




| | | | |
|---|---|---|---|
| **Device:** | PL138-48: | 2.5V - 3.3V, Low-Skew, 1:4 Differential PECL Fanout Buffer | |
| **Package:** | O | = | 20-Pin TSSOP |
| | Q | = | 16-Pin QFN |
| **Temperature Range:** | C | = | 0°C to +70°C (Commercial) |
| | I | = | –40°C to +85°C (Industrial) |
| **Packing Option:** | Blank | = | Tube |
| | R | = | Tape & Reel |

**Examples:**

a) PL138-48OC-R: 2.5V - 3.3V, Low-Skew, 1:4 Differential PECL Fanout Buffer, 20-Pin TSSOP, Commercial Temperature Range, Tape & Reel

b) PL138-48QI: 2.5V - 3.3V, Low-Skew, 1:4 Differential PECL Fanout Buffer, 16-Pin QFN, Industrial Temperature Range, Tube

c) PL138-48OI-R: 2.5V - 3.3V, Low-Skew, 1:4 Differential PECL Fanout Buffer, 20-Pin TSSOP, Industrial Temperature Range, Tape & Reel

d) PL138-48QC: 2.5V - 3.3V, Low-Skew, 1:4 Differential PECL Fanout Buffer, 16-Pin QFN, Commercial Temperature Range, Tube

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