PL586-55/-58

Low Phase Noise, LVPECL VCXO (for 150MHz to 160MHz Fundamental Crystals)

FEATURES

- Advanced non multiplier VCXO Design for High Performance Crystal Oscillators
- Input/Output Range: 150MHz to 160MHz
- Phase Noise Optimized for 155.52MHz: -68dBc @10Hz, -152dBc @100kHz
- Very low Phase Jitter: <100fs RMS
- High Pull Range: ±100ppm
- Linearity: <5%
- Integrated Variable Capacitors
- Complementary LVPECL Outputs
- Power Supply: 3.3V ±10%
- Available in Die or Wafer Form

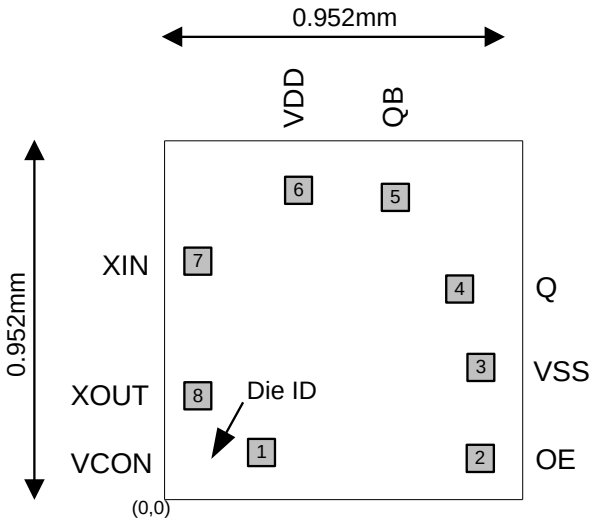
DESCRIPTION

The PL586-55/-58 is a non-multiplier VCXO IC specifically designed to pull fundamental mode crystals from 150MHz to 160MHz. This IC achieves a typical pull range of ±100ppm with <5% linearity. The phase noise performance is optimized for close-in performance and with <100fs phase jitter, makes this an ideal solution for all high end clocking applications such as SONET, WiMax, CPRI, OBSAI, Fiber Channel, and any application where performance and quality are required.

DIE SPECIFICATIONS

Name	Value
Size	952 micron x 952 micron
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	8 mil

DIE CONFIGURATION



OUTPUT ENABLE LOGIC PL586-55

OE State (Pad 4)	Output Buffers State
0	Outputs Tri-Stated
1 (Default)	Outputs Enabled

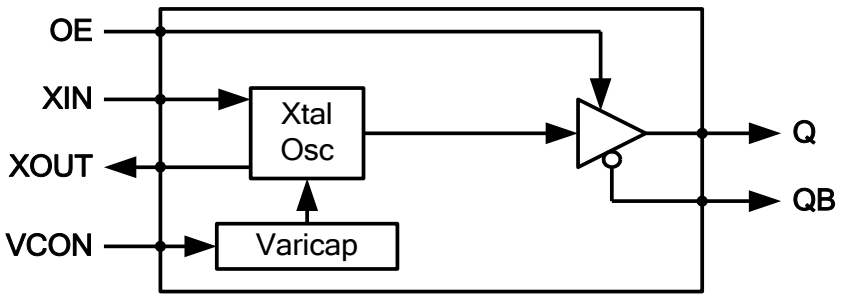
* Internal 60KΩ pull-up resistor

OUTPUT ENABLE LOGIC PL586-58

OE State (Pad 4)	Output Buffers State
0 (Default)	Outputs Enabled
1	Outputs Tri-Stated

* Internal 60KΩ pull-down resistor

BLOCK DIAGRAM



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PAD ASSIGNMENT

Pad #	Name	X (µm)*	Y (µm)*	Description
1	VCON	-194	-365	Voltage Control input
2	XOUT	-372	-190	Crystal output connection
3	XIN	-372	158	Crystal input connection
4	VDD	-117	329	V_{DD} connection
5	QB	140	315	Complementary LVPECL output
6	Q	315	75	LVPECL output
7	VSS	373	-127	GND connection
8	OE	373	-373	Output enable pin. Internal pull up (-55) or pull down (-58).

* **Note:** Referenced to center of the die.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, DC	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, DC	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature	T_A	-40	85	°C
HBM ESD Protection		2,000		V

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

2. Voltage Control Crystal Oscillator

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time *	$T_{VCXOSTB}$	From power valid			10	ms
VCXO Pullability *		XTAL C_1 = 6.8, C_0/C_1 = 270 0V ≤ VCON ≤ V_{DD} (at 25°C)		± 120		ppm
		XTAL C_1 = 3.7, C_0/C_1 = 480 0V ≤ VCON ≤ V_{DD} (at 25°C)		± 70		ppm
Varicap Control Range *		VCON = 0 to V_{DD}	0		3.3	V
Linearity *		0.0V ≤ VCON ≤ 3.3V		7		%
		0.3V ≤ VCON ≤ 3.0V		2.5		%
VCON Input Impedance *		DC Input resistance	10			MΩ
VCON Modulation BW *		0V ≤ VCON ≤ V_{DD}, -3dB		30		kHz

Note: Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits.

3. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}	Fundamental Mode, AT cut	150		160	MHz
Crystal Loading Rating	$C_{L\ (xtal)}$	VCON = 1.65V		5		pF
Shunt Capacitance	C_0				2.0	pF
Motional Capacitance	C_1	Recommended for at least ±100ppm Frequency Pulling	5.5			fF
Recommended ESR	R_E	C_0 ≤ 2.0pF			10	Ω
		C_0 ≤ 1.5pF			12	Ω

4. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	I_{DD}	Standard LVPECL Loading (See LVPECL Levels Test Circuit, page 4)			50	mA
Operating Voltage	V_{DD}		2.97	3.3	3.63	V
Output Clock Duty Cycle		@ V_{DD} – 1.3V (See LVPECL Transition Time Waveform, page 4)	45	50	55	%
Short Circuit Current				±50		mA

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5. Jitter Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period Jitter RMS	At 155.52MHz, with capacitive decoupling between V_{DD} and GND. Over 10,000 cycles		2.5		ps
Period Jitter pk-to-pk			20		
Integrated Jitter RMS at 155.52MHz	Integrated 12 kHz to 20 MHz		90		fs

6. Phase Noise Specifications

PARAMETERS	FREQUENCY	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	@1MHz	@10MHz	UNITS
Phase Noise, relative to carrier	155.52MHz	-68	98	124	144	152	156	158	dBc/Hz

Note: Phase Noise measured at VCON = 0.3V to 3.0V.

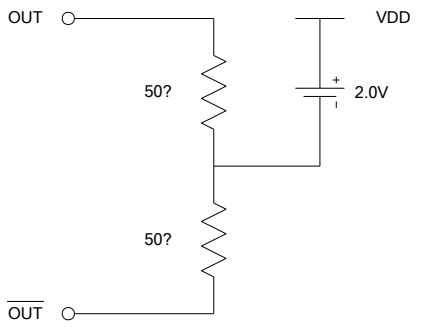
7. LVPECL Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output High Voltage	V_{OH}	R_L = 50 Ω to (V_{DD} – 2V) (see figure)	V_{DD} – 1.025	V_{DD} – 0.950	V_{DD} – 0.880	V
Output Low Voltage	V_{OL}		V_{DD} – 1.810	V_{DD} – 1.700	V_{DD} – 1.620	V

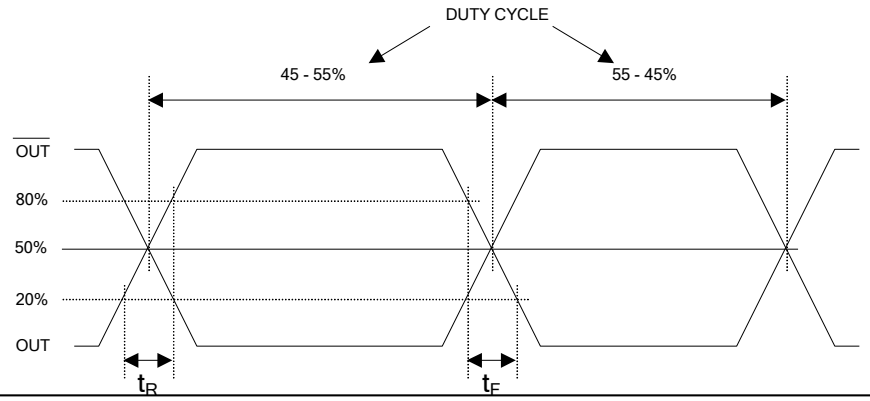
8. LVPECL Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	t_r	@20/80% of output waveform		400	600	ps
Clock Fall Time	t_f	@80/20% of output waveform		400	600	ps

LVPECL Levels Test Circuit



LVPECL Transistion Time Waveform



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ORDERING INFORMATION

For part ordering, please contact our Sales Department:

2180 Fortune Drive, San Jose, CA 95131, USA
Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER

The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range

PL586-5X XX

Part Number

Packaging Option
D = Die
W = Wafer

Temperature Range
C=Commercial (0°C to 70°C)

Order Number	Packaging
PL586-55DC PL586-58DC	Die – Waffle Pack
PL586-55WC PL586-58WC	Wafer