

NB6L56

2.5V / 3.3V Dual 2:1 Differential Clock / Data Multiplexer with LVPECL Outputs

Multi-Level Inputs w/ Internal Termination

The NB6L56 is a high performance Dual 2-to-1 Differential Clock or Data multiplexer. The differential inputs incorporate internal 50 Ω termination resistors that are accessed through the VT pin. This feature allows the NB6L56 to accept various Differential logic level standards, such as LVPECL, CML or LVDS. Outputs are 800 mV LVPECL signals. For interface options see Figures 12 – 15.

The NB6L56 produces minimal Clock or Data jitter operating up to 2.5 GHz or 2.5 Gbps, respectively. As such, the NB6L56 is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock/Data distribution applications.

The NB6L56 is offered in a low profile 5 mm x 5 mm 32-pin QFN package and is a member of the ECLinPS MAX™ family of high performance Clock / Data products. Application notes, models, and support documentation are available at www.onsemi.com.

Features

- Maximum Input Data Rate > 2.5 Gbps
- Maximum Input Clock Frequency > 2.5 GHz
- Jitter
 - < 1 ps RMS RJ (Data)
 - < 10 ps PP DJ (Data)
 - < 0.7 ps RMS Crosstalk induced jitter (CLOCK)
- 360 ps Max Propagation Delay
- 180 ps Max Rise and Fall Times
- Operating Range:
 - $V_{CC} = 2.5 \pm 5\%$ (2.375 V to 2.625 V)
 - $V_{CC} = 3.3 \pm 10\%$ (3.0 V to 3.6 V)
- Internal 50 Ω Input Termination Resistors
- Industrial Temp. Range (-40°C to 85°C)
- QFN-32 Package
- These are Pb-Free Devices

Applications

- Clock and Data Distribution
- Networking and Communications
- High End Computing
- Wireless and Wired Infrastructure

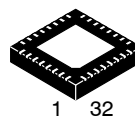
End Products

- Servers
- Ethernet Switch/Routers
- ATE
- Test and Measurement



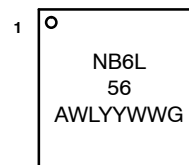
ON Semiconductor®

<http://onsemi.com>



QFN32
MN SUFFIX
CASE 488AM

MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

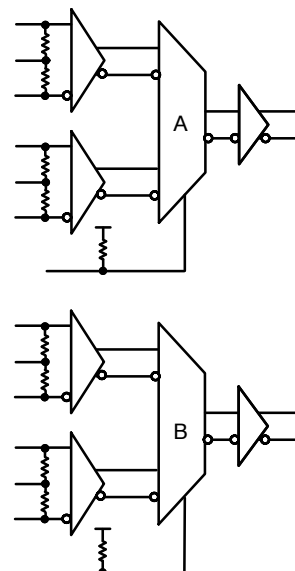


Figure 1. Simplified Logic Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

NB6L56

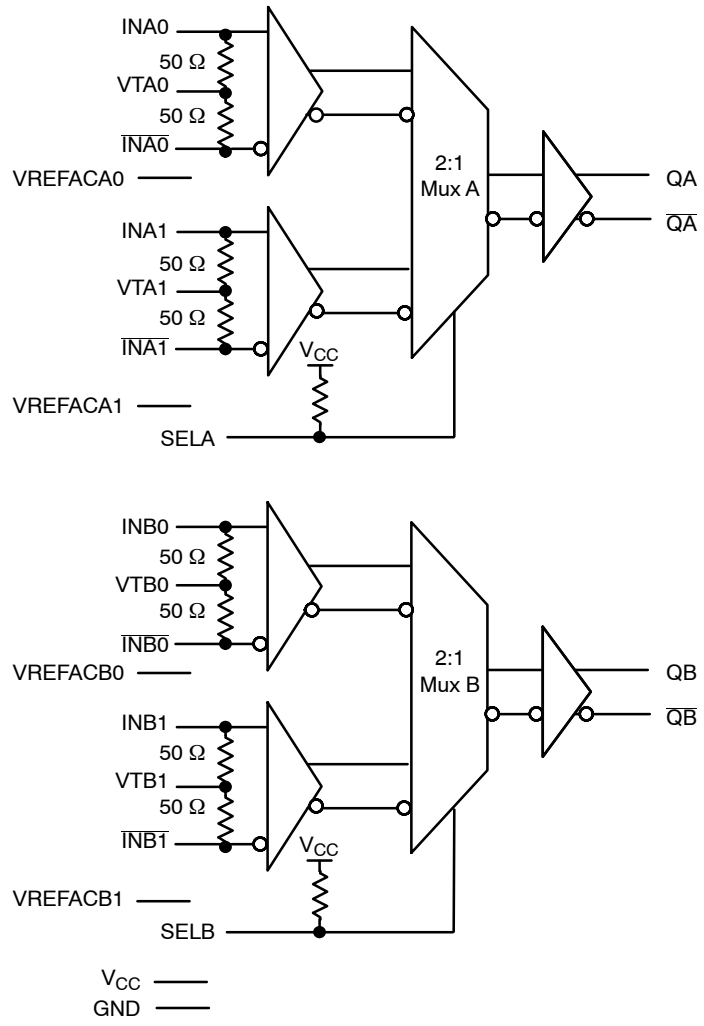


Figure 2. Pin Configuration (Top View)

NB6L56

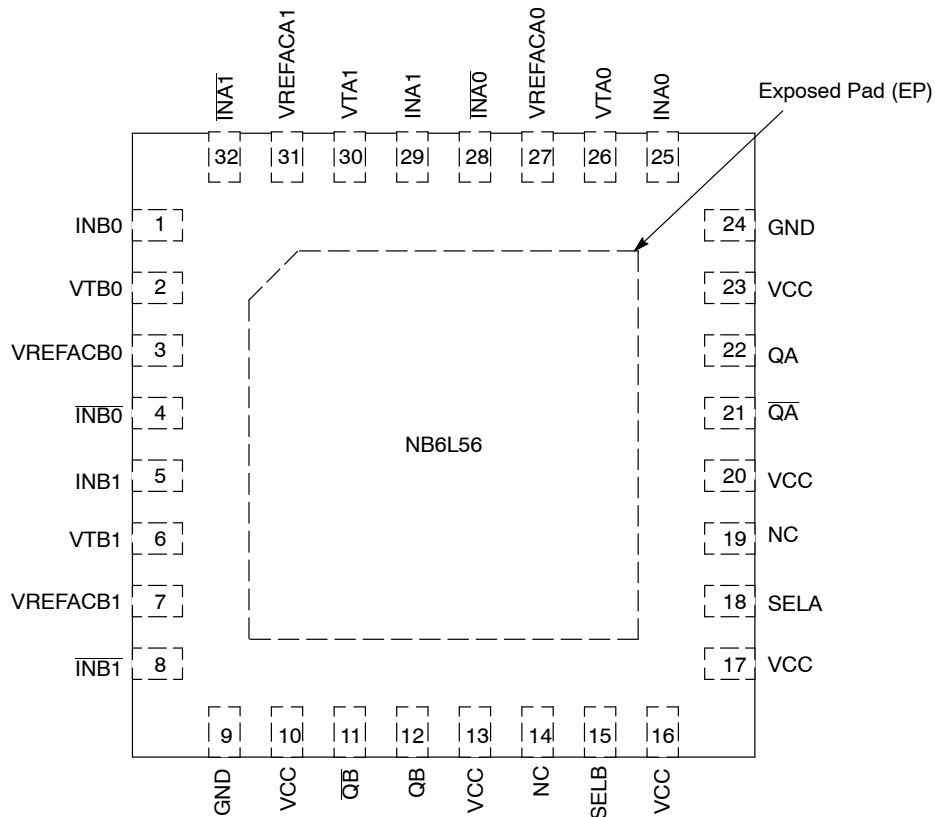


Figure 3. NB6L56 Pinout: QFN-32 (Top View)

Table 1. PIN DESCRIPTION

| Pin | Name | I/O | Pin Description |
|----------------------------------|--|----------------------------|---|
| 1, 4 5, 8 25, 28 29, 32 | INB0, $\overline{\text{INB0}}$ INB1, $\overline{\text{INB1}}$ INA0, $\overline{\text{INA0}}$ INA1, $\overline{\text{INA1}}$ | LVPECL, CML, LVDS Input | Noninverted, Inverted Differential Input pairs (Note 1). Default state is indeterminate if left floating open. Do not connect unused input pairs with one input connected to VCC and the complementary input to GND. For differential and single ended interface, see "Interface Applications". |
| 2, 6 26, 30 | VTB0, VTB1 VTA0, VTA1 | | Internal 100 Ω Center-tapped Termination Pin for Differential Input pairs (Figure 4) |
| 3 7 27 31 | VREFACB0 VREFACB1 VREFACA0 VREFACA1 | - | Output Voltage Reference for Capacitor-Coupled Inputs or Single Ended Interface (see "Interface Applications") |
| 15 18 | SELB SELA | LVTTTL / LVCMOS Input | Input Select pin; LOW for IN0 Inputs, HIGH for IN1 Inputs; defaults HIGH when left open |
| 14, 19 | NC | - | No Connect |
| 10, 13, 16, 17 20, 23 | VCC | Power | Positive Supply Voltage. All VCC pins must be connected to the positive power supply for correct DC and AC operation. |
| 11, 12 21, 22 | $\overline{\text{QB}}$, QB QA, QA | LVPECL Output | Inverted, Non-inverted Differential Outputs Note 1. |
| 9, 24 | GND | Ground | Negative Supply Voltage, connected to Ground |
| - | EP | - | The Exposed Pad (EP) on the package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is connected to the die and must only be connected electrically to GND on the PC board. |

1. If no signal is applied on any IN_{xn} input pair, the device will be susceptible to self-oscillation.
2. All V_{CC} and GND pins must be externally connected to a power supply for proper operation.

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Table 2. INPUT SELECT FUNCTION TABLE

| SELA/SELB | Q | \bar{Q} |
|-----------|------|--------------|
| L | INx0 | $\bar{INx0}$ |
| H | INx1 | $\bar{INx1}$ |

Table 3. ATTRIBUTES

| Characteristic | | Value |
|--|-----------------------------------|----------------------|
| ESD Protection | Human Body Model Machine Model | >2 kV 200 V |
| Input Pullup resistor (R _{PU}) | | 75 kΩ |
| Moisture Sensitivity (Note 3) | QFN32 | Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| Transistor Count | | 1023 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | |

3. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 4)

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---------------------|--|---------------------|----------------------|-------------|------|
| V _{CC} | Positive Power Supply | GND = 0 V | | 4.0 | V |
| V _{INPP} | Differential Input Voltage INx – \bar{INx} | | | 1.89 | V |
| I _{IN} | Input Current Through RT (50 Ω Resistor) | | | ±40 | mA |
| I _{OUT} | Output Current | Continuous Surge | | ±50 ±100 | mA |
| I _{VREFAC} | VREFAC Sink/Source Current | | | ±1.5 | mA |
| T _A | Operating Temperature Range | | | –40 to +85 | °C |
| T _{stg} | Storage Temperature Range | | | –65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction–to–Ambient) (Note 4) | 0 lfpm 500 lfpm | QFN – 32 QFN – 32 | 31 27 | °C/W |
| θ _{JC} | Thermal Resistance (Junction–to–Case) (Note 4) | Standard Board | QFN – 32 | 12 | °C/W |
| ψ _{JC} | Thermal Resistance (Junction–to–Board) | | | 16 | °C/W |
| T _{sol} | Wave Solder Pb–Free | | | 265 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. JEDEC standard 51–6, multilayer board – 2S2P (2 signal, 2 power) with eight filled thermal vias under exposed pad.

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Table 5. DC CHARACTERISTICS $V_{CC} = 2.5 \pm 5\%$ (2.375 V to 2.625 V); $V_{CC} = 3.3 \pm 10\%$ (3.0 V to 3.6 V) (Note 5)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|----------|--|-----|-----|-----|------|
| I_{CC} | Power Supply Current (Inputs and Outputs Open) | | 65 | 85 | mA |

LVPECL OUTPUTS

| | | | | | |
|-----------|--|------------------|-------------|------------------|----|
| V_{OH} | Output HIGH Voltage | $V_{CC} - 1.145$ | | $V_{CC} - 0.895$ | mV |
| V_{OL} | Output LOW Voltage | $V_{CC} - 2.000$ | | $V_{CC} - 1.695$ | mV |
| V_{OUT} | Output Swing (Single Ended) Output Swing (Differential) | 400 800 | 800 1600 | | mV |

DIFFERENTIAL INPUT DRIVEN SINGLE-ENDED (Note 6) (Figures 5 and 6)

| | | | | | |
|-----------|---|---------------|--|---------------|----|
| V_{th} | Input Threshold Reference Voltage Range | 1125 | | $V_{CC} - 75$ | mV |
| V_{IH} | Single-ended Input HIGH Voltage | $V_{th} + 75$ | | V_{CC} | mV |
| V_{IL} | Single-ended Input LOW Voltage | GND | | $V_{th} - 75$ | mV |
| V_{ISE} | Single-ended Input Voltage ($V_{IH} - V_{IL}$) (Note 6) | 150 | | 3015 | mV |

DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Note 7) (Figures 7 and 8)

| | | | | | |
|-----------|---|------|--|-----------------|---------|
| V_{IHD} | Differential Input HIGH Voltage | 1200 | | V_{CC} | mV |
| V_{ILD} | Differential Input LOW Voltage | GND | | $V_{IHD} - 100$ | mV |
| V_{ID} | Differential Input Voltage ($V_{IHD} - V_{ILD}$) | 100 | | 1890 | mV |
| V_{CMR} | Input Common Mode Range (Differential Configuration) (Figure 9) | 1150 | | $V_{CC} - 50$ | mV |
| I_{IH} | Input HIGH Current (V_{Tnx} Open) | -150 | | 150 | μA |
| I_{IL} | Input LOW Current (V_{Tnx} Open) | -150 | | 150 | μA |

LVTTTL / LVCMOS INPUTS (SELA/SELB)

| | | | | | |
|----------|---------------------------------------|------|--|-----|---------|
| V_{IH} | Input HIGH Voltage | 2.0 | | | V |
| V_{IL} | Input LOW Voltage | | | 0.8 | V |
| I_{IL} | Input LOW Current ($V_{IN} = 0.5$ V) | -300 | | | μA |
| I_{IH} | Input HIGH Current (V_{CC}) | | | 75 | μA |

TERMINATION RESISTORS

| | | | | | |
|-----------|--|----|----|----|----------|
| R_{TIN} | Internal Input Termination Resistor INx_n/INx_n to VTx_n | 45 | 50 | 55 | Ω |
|-----------|--|----|----|----|----------|

REFERENCE VOLTAGE

| | | | | | |
|--------------|--------------------------|-----------------|----------------|----------------|---|
| V_{REF-AC} | Output Reference Voltage | $V_{CC} - 1.35$ | $V_{CC} - 1.2$ | $V_{CC} - 1.1$ | V |
|--------------|--------------------------|-----------------|----------------|----------------|---|

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Outputs evaluated with 50 Ω resistors to $V_{TT} = V_{CC} - 2.0$ V for proper operation (See Figure 16).

6. V_{TH} is applied to the complementary input when operating in single-ended mode. V_{IH} , V_{IL} and V_{TH} parameters must be complied with simultaneously.

7. V_{IHD} , V_{ILD} and V_{CMR} parameters must be complied with simultaneously. V_{CMR} max varies 1:1 with V_{CC} .

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Table 6. AC CHARACTERISTICS $V_{CC} = 2.5 \pm 5\%$ (2.375 V to 2.625 V); $V_{CC} = 3.3 \pm 10\%$ (3.0 V to 3.6 V) (Note 8)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|--------------------------|--|------------|------------|--------------------|----------------|
| f_{MAX} | Maximum Input Clock Frequency Maximum Operating Data Rate (NRZ) $V_{outpp} \geq 400$ mV $V_{outpp} \geq 400$ mV | 2.5 2.5 | | | Ghz Gbps |
| f_{SEL} | Maximum Toggle Frequency, SELA/SELB | 25 | 50 | | MHz |
| V_{OUTPP} | Output Voltage Amplitude (Differential Interconnect) $f_{in} \leq 2.5$ GHz | 400 | | | mVpp |
| t_{PLH} , t_{PHL} | Propagation Delay to Differential Outputs, @ 1 GHz, INxn/INxn̄ to Qx, Qx̄ SELx to Qx, Qx̄ | 160 100 | 250 260 | 360 400 | ps |
| t_{PLH} Tempco | Differential Propagation Delay Temperature Coefficient | | 143 | | Δ fs/°C |
| tskew | Input to Input per Bank Within Device Output Bank to Output Bank Within Device | | 10 12 | 20 25 | ps |
| t_{JITTER} | DATA JITTER R_J for K28.7 at 2.5 GHz (RMS) D_J for NRZ PRBS23 / K28.5 at 2.5 Gbps CLOCK JITTER Cycle to Cycle (1K WFMS; RMS) Total Jitter TJ (PP) | | | 1 10 1 10 | ps |
| tjit(ϕ) | Integrated Phase Jitter $f_{in} = 155.52$ MHz and 1GHz 12 kHz – 20 MHz Offset (RMS) | | 35 | | fs |
| t_{JITTER} | Crosstalk Induced Jitter Input to Input per Output Bank Within Device (Note 9) | | | 0.7 | psRMS |
| V_{INPP} | Input Voltage Swing (Differential Configuration) (Note 10) | 100 | | 1200 | mV |
| t_r , t_f | Output Rise/Fall Times @ 1 GHz (20% – 80%), Qx, Qx̄ | 50 | 100 | 180 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

8. Differential 50% duty cycle at $V_{INPPmin}$ clock source. Outputs evaluated with 50 Ω resistors to $V_{TT} = V_{CC} - 2.0$ V (See Figure 16). Input crosspoint to output crosspoint for INxn/INxn̄ to Qx, Qx̄; 50% input to output crosspoint for SELx to Qx, Qx̄. See Figures 5, 10 and 11.
9. Crosstalk is measured at the output while applying two similar clock frequencies that are asynchronous with respect to each other at the inputs.
10. Input voltage swing is a single-ended measurement operating in differential mode.

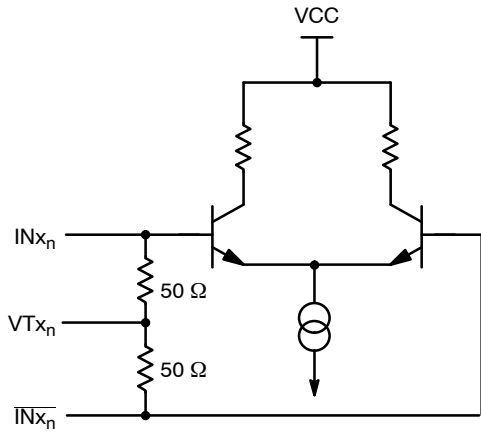


Figure 4. Simplified Input Structure

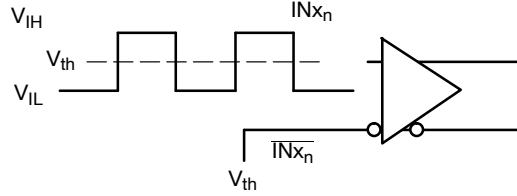


Figure 5. Differential Input Driven Single-Ended

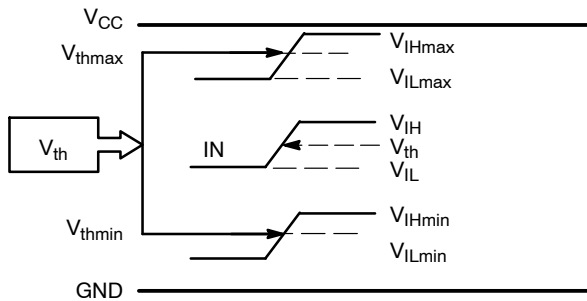


Figure 6. V_{th} Diagram

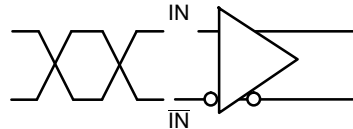


Figure 7. Differential Inputs Driven Differentially

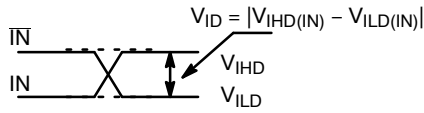


Figure 8. Differential Inputs Driven Differentially

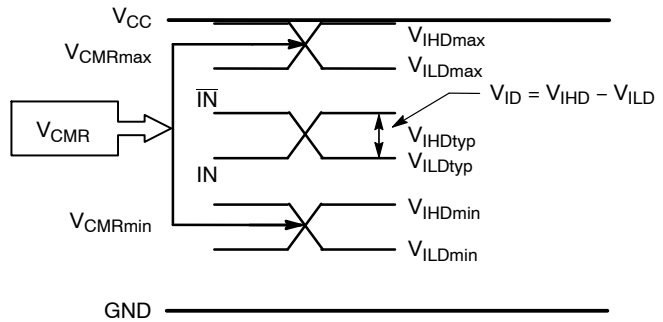


Figure 9. V_{CMR} Diagram

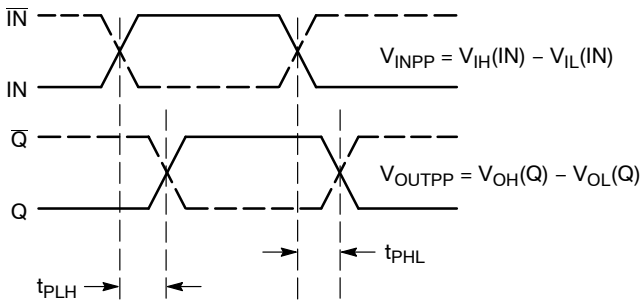


Figure 10. AC Reference Measurement

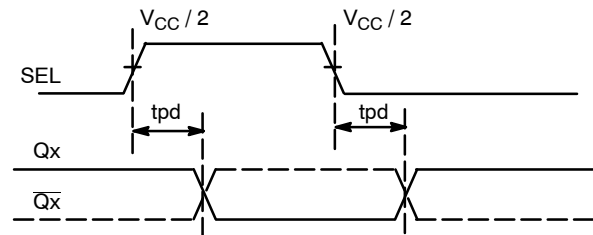


Figure 11. SEL to Qx Timing Diagram

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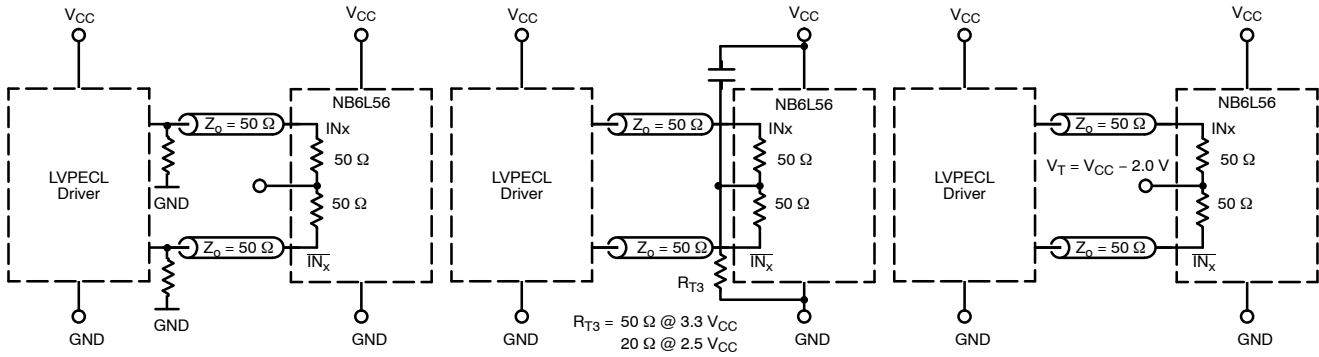


Figure 12. Typical LVPECL Interface (see AND8020)

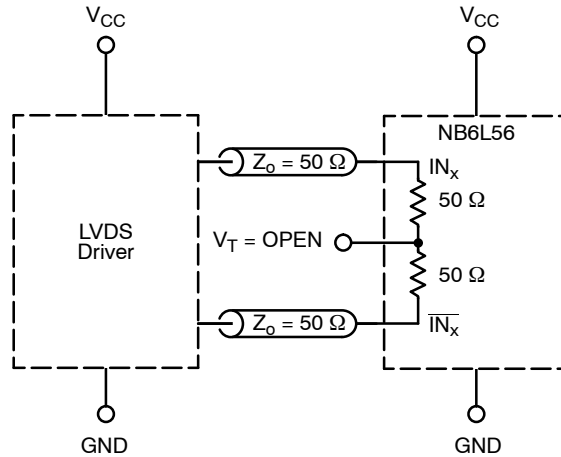


Figure 13. Typical LVDS Interface

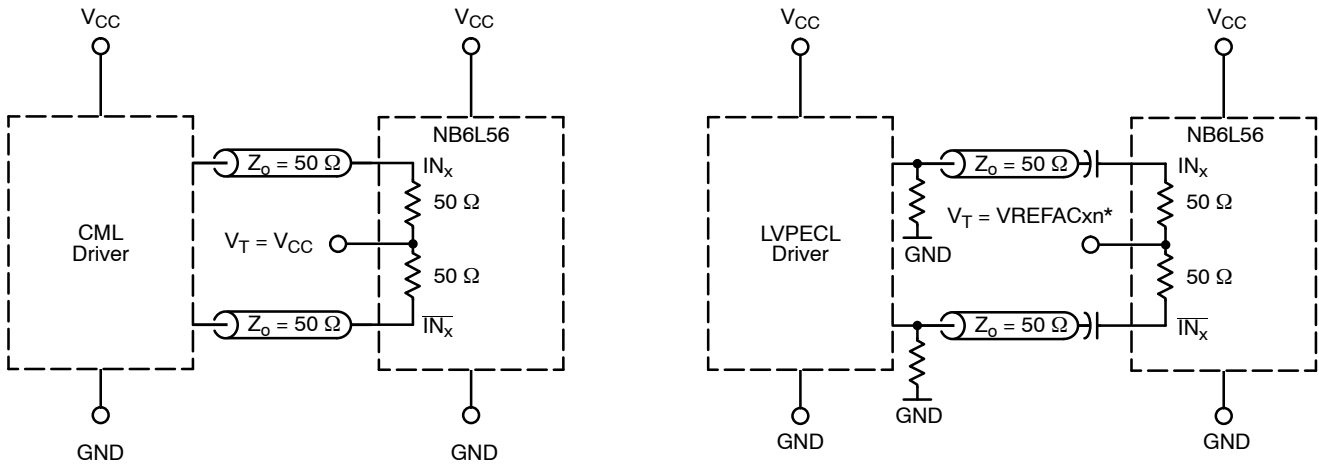


Figure 14. Typical Standard 50 Ω Load CML Interface

Figure 15. Typical LVPECL Capacitor-Coupled Differential Interface (V_T Connected to V_{REFAC})
* V_{REFAC} bypassed to ground with a 0.01 μF capacitor.

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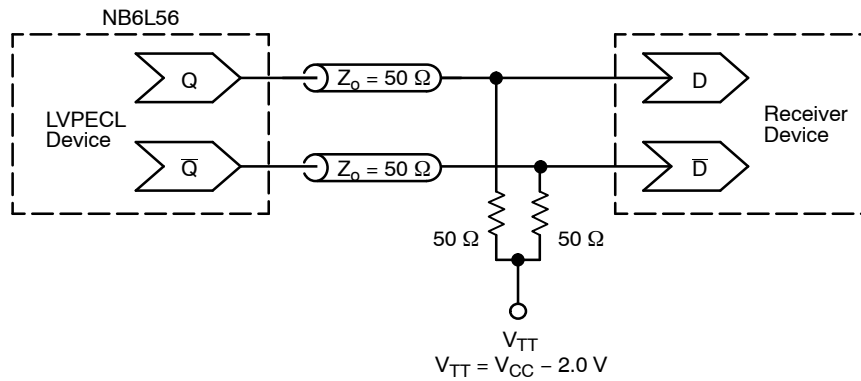


Figure 16. Typical Termination for LVPECL Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|-------------|--------------------|-----------------------|
| NB6L56MNG | QFN32 (Pb-Free) | 74 Units / Rail |
| NB6L56MNTXG | QFN32 (Pb-Free) | 1000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



1 32

SCALE 2:1

QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

DATE 23 OCT 2013



TOP VIEW

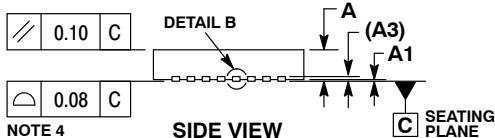


DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS

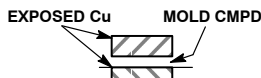
NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS | | |
|-------------|------|------|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | --- | 0.05 |
| A3 | 0.20 | REF |
| b | 0.18 | 0.30 |
| D | 5.00 | BSC |
| D2 | 2.95 | 3.25 |
| E | 5.00 | BSC |
| E2 | 2.95 | 3.25 |
| e | 0.50 | BSC |
| K | 0.20 | --- |
| L | 0.30 | 0.50 |
| L1 | --- | 0.15 |

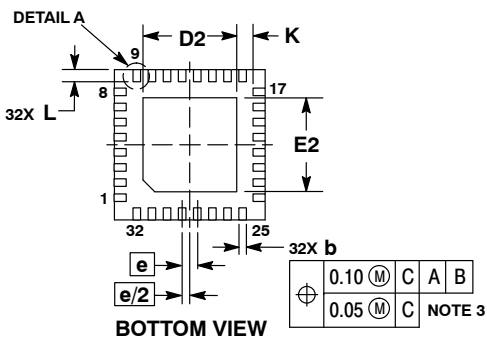


SIDE VIEW

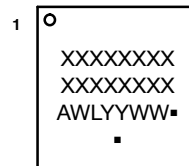


DETAIL B
ALTERNATE
CONSTRUCTION

GENERIC
MARKING DIAGRAM*



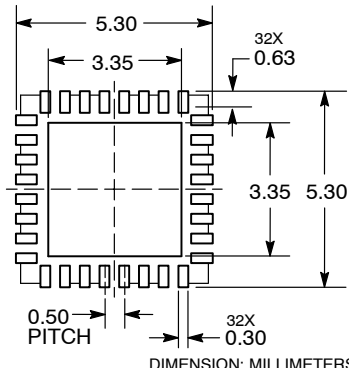
BOTTOM VIEW



- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)
*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

RECOMMENDED
SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|------------------|----------------|--|
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| DESCRIPTION: | QFN32 5x5 0.5P | PAGE 1 OF 1 |

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