DUAL 2:1 AND 1:2, DIFFERENTIAL-TO-LVPECL/ECL MULTIPLEXER

ICS85354

General Description

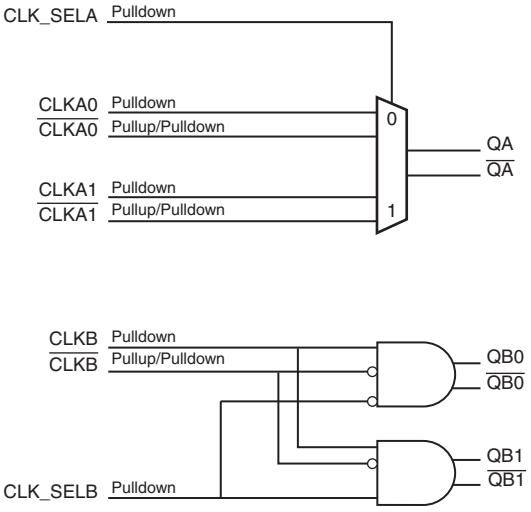
The ICS85354 is a dual 2:1 and 1:2 Multiplexer and a member of the HiPerClockS™ family of high performance clock solutions from IDT. The 2:1 Multiplexer allows one of 2 inputs to be selected onto one output pin and the 1:2 MUX switches one input to one of two outputs. This device is useful for multiplexing multi-rate Ethernet PHYs which have 100 M bit and 1000 bit transmit/receive pairs onto an optical SFP module which has a single transmit/receive pair. See Application Section for further information.

The ICS85354 is optimized for applications requiring very high performance and has a maximum operating frequency of 3GHz. The device is packaged in a small, 3mm x 3mm VFQFN package, making it ideal for use on space-constrained boards.

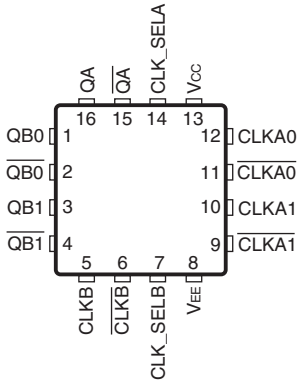
Features

- Three LVPECL outputs
- Three differential clock inputs
- CLKx/$\overline{\text{CLKx}}$ pairs can accept the following differential input levels: LVPECL, LVDS, CML
- Maximum output frequency: 3.2GHz
- Part-to-part skew: 200ps (maximum)
- Propagation delay: QA/$\overline{\text{QA}}$: 450ps (maximum)
  QBx/$\overline{\text{QBx}}$: 430ps (maximum)
- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 3.465V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3.465V to -2.375V-40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS85354

16-Lead VFQFN
3mm x 3mm x 0.95mm
package body
K Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	QB0/$\overline{QB0}$	Output		Differential output pair. LVPECL/ECL interface levels.
3, 4	QB1/$\overline{QB1}$	Output		Differential output pair. LVPECL/ECL interface levels.
5	CLKB	Input	Pulldown	Non-inverting LVPECL/ECL differential clock input.
6	$\overline{CLKB}$	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{CC}/2 default when left floating.
7	CLK_SELB	Input	Pulldown	Clock select pin for QBx outputs. When HIGH, selects QB1/$\overline{QB1}$ outputs. When LOW, selects QB0/$\overline{QB0}$ outputs. LVCMOS/LVTTL interface levels.
8	V_{EE}	Power		Negative supply pin.
9	$\overline{CLKA1}$	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{CC}/2 default when left floating.
10	CLKA1	Input	Pulldown	Non-inverting LVPECL/ECL differential clock input.
11	$\overline{CLKA0}$	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. V_{CC}/2 default when left floating.
12	CLKA0	Input	Pulldown	Non-inverting LVPECL/ECL differential clock input.
13	V_{CC}	Power		Positive supply pin.
14	CLK_SELA	Input	Pulldown	Clock select pin for QA output. When HIGH, selects QA output. When LOW, selects $\overline{QA}$ output. LVCMOS/LVTTL interface levels.
15, 16	$\overline{QA}$/QA	Output		Differential output pair. LVPECL/ECL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			37.5		kΩ
$R_{VCC/2}$	Pullup/Pulldown Resistor			37.5		kΩ

Function Tables

Table 3A. Control Input Function Table, (Bank A)

Bank A	
Control Input	**Outputs**
CLK_SELA	**QA/$\overline{QA}$**
0	Selects CLKA0/$\overline{CLKA0}$
1	Selects CLKA1/$\overline{CLKA1}$

Table 3B. Control Input Function Table, (Bank B)

Bank B		
Control Input	**Outputs**	
CLK_SELB	**QB0/$\overline{QB0}$**	**QB1/$\overline{QB1}$**
0	Follows CLKB input	Low
1	Low	Follows CLKB input

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V (LVPECL mode, V_{EE} = 0V)
Negative Supply Voltage, V_{EE}	-4.6V (ECL mode, V_{CC} = 0V)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5V
Inputs, V_I (ECL mode)	0.5V to V_{EE} – 0.5V
Outputs, I_O Continuos Current Surge Current	 50mA 100mA
Operating Termperature Range, T_A	-40°C to 85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA}	51.5°C/W (0 lfpm)

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 2.375V to 3.465V, V_{EE} = 0V or V_{CC} = 0V, V_{EE} = -3.465V to -2.375V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{EE}	Power Supply Current				50	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{CC} = 2.375V to 3.465V, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			$0.7V_{CC}$		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		$0.3V_{CC}$	V
I_{IH}	Input High Current	CLK_SELA, CLK_SELB	$V_{CC} = V_{IN}$			150	µA
I_{IL}	Input Low Current	CLK_SELA, CLK_SELB	$V_{CC} = V_{IN}$	-150			µA

Table 4C. LVCMOS/LVTTL DC Characteristics, V_{CC} = 0V, V_{EE} = -3.465V to -2.375V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			$0.3V_{EE}$		0.3	V
V_{IL}	Input Low Voltage			V_{EE} – 0.3		$0.7V_{EE}$	V
I_{IH}	Input High Current	CLK_SELA, CLK_SELB	$V_{CC} = V_{IN}$			150	µA
I_{IL}	Input Low Current	CLK_SELA, CLK_SELB	$V_{CC} = V_{IN}$	-150			µA

Table 4D. LVPECL DC Characteristics, V_{CC} = 2.375V to 3.465V, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLKA[0:1], CLKB	$V_{CC} = V_{IN}$			200	µA
		$\overline{CLKA[0:1]}$, $\overline{CLKB}$	$V_{CC} = V_{IN}$			200	µA
I_{IL}	Input Low Current	CLKA[0:1], CLKB	V_{CC} = 3.465V, V_{IN} = 0V	-200			µA
		$\overline{CLKA[0:1]}$, $\overline{CLKB}$	V_{CC} = 3.465V, V_{IN} = 0V	-200			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.2	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			1.2		V_{CC}	V
V_{OH}	Output High Current; NOTE 3			V_{CC} – 1.125	V_{CC} – 1.005	V_{CC} – 0.92	V
V_{OL}	Output Low Current; NOTE 3			V_{CC} – 1.895	V_{CC} – 1.78	V_{CC} – 1.62	V
V_{SWING}	Peak-to-Peak Output Voltage Swing			0.6		1.0	V

NOTE 1: Common mode input voltage is defined as V_{IH}.
NOTE 2: For single-ended applications, the maximum input voltage for CLKx, $\overline{CLKx}$ is V_{CC} + 0.3V.
NOTE 3: Outputs terminated with 50Ω to V_{CC} – 2V.

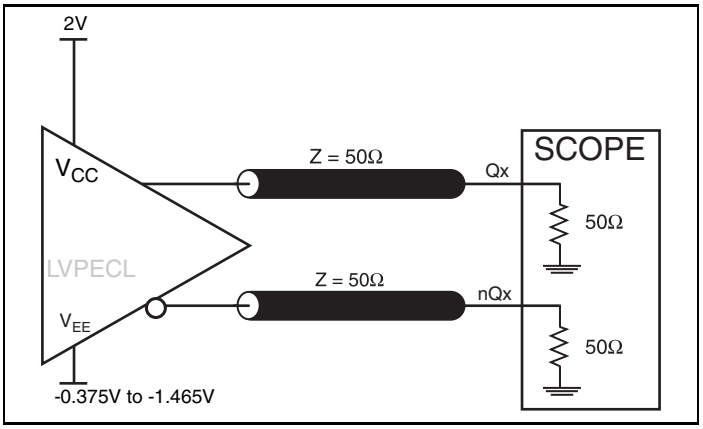
AC Electrical Characteristics

Table 5. AC Characteristics, V_{CC} = 2.375V to 3.465V, V_{EE} = 0V or V_{CC} = 0V, V_{EE} = -3.465V to -2.375V, T_A = -40°C to 85°C

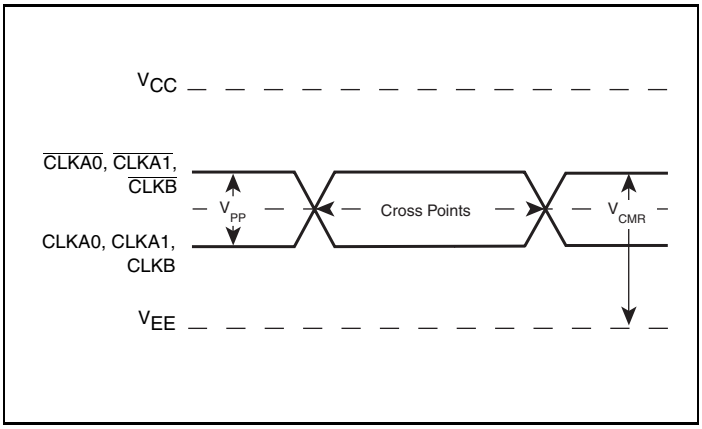
Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency					3.2	GHz
t_{PD}	Propagation Delay; NOTE 1	QA/$\overline{QA}$		225	335	445	ps
		QBx/$\overline{QBx}$		195	305	420	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3					200	ps
$MUX_{\_ISOLATION}$	MUX Isolation; NOTE 4				55		dB
t_R / t_F	Output Rise/Fall Time		20% to 80%	75	155	245	ps

All parameters are measured ≤ 1GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Measured using standard LVPECL input at 622MHz.

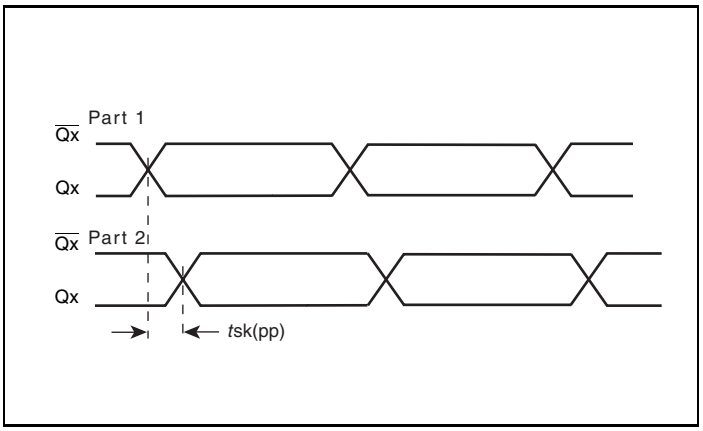
Parameter Measurement Information



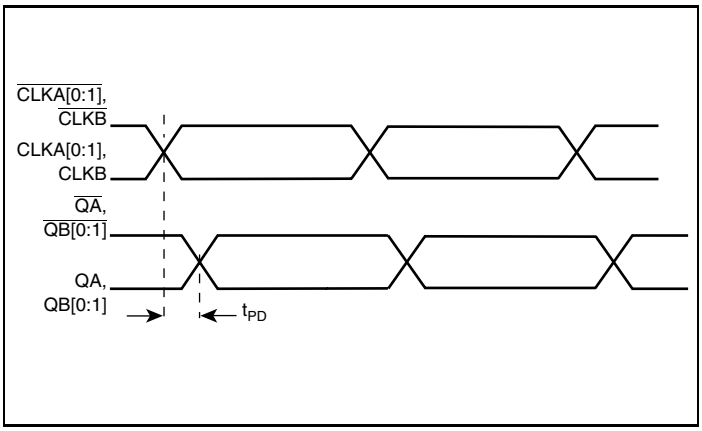
LVPECL Output Load AC Test Circuit



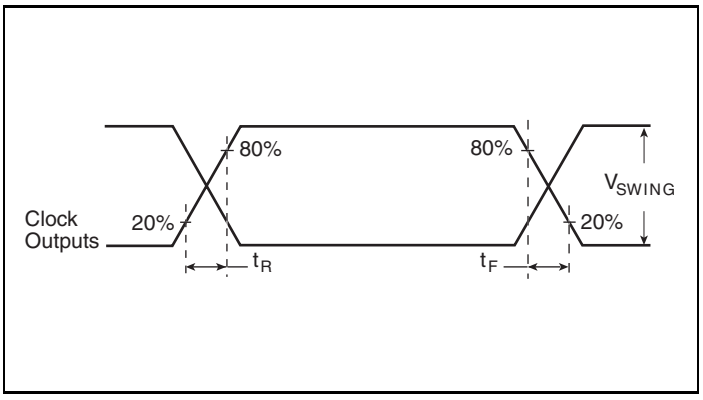
Differential Input Level



Part-to-Part Skew



Propagation Delay



Output Rise/Fall Time

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

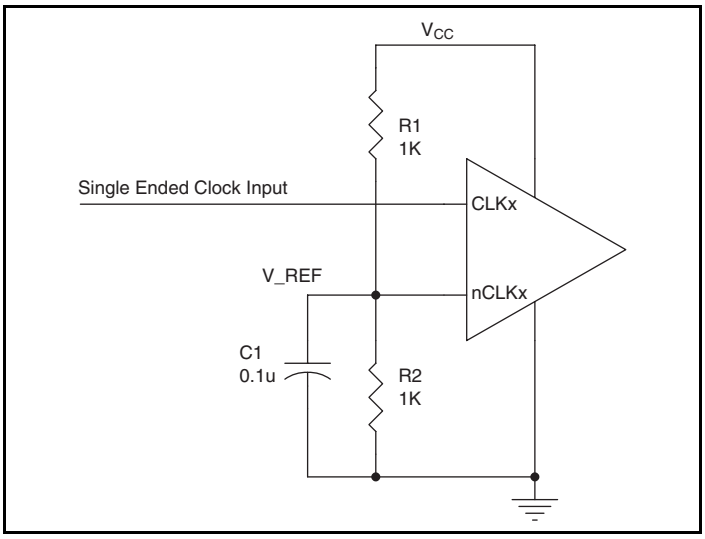


Figure 1. Single-Ended Signal Driving Differential Input

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

CLK/$\overline{CLK}$ Inputs

For applications not requiring the use of the differential input, both CLK and $\overline{CLK}$ can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Differential Clock Input Interface

The CLK /$\overline{CLK}$ accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2F* show interface examples for the HiPerClockS CLK/$\overline{CLK}$ input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

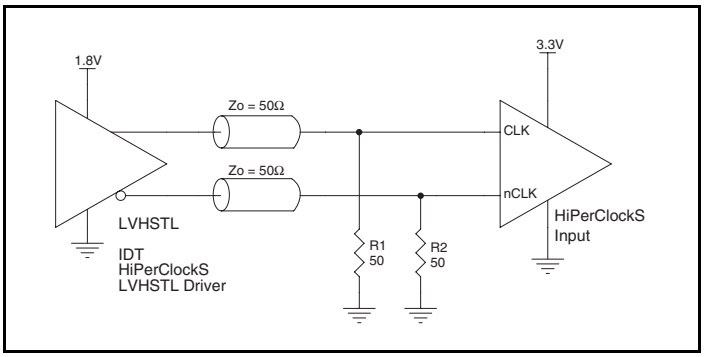


Figure 2A. HiPerClockS CLK/$\overline{CLK}$ Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

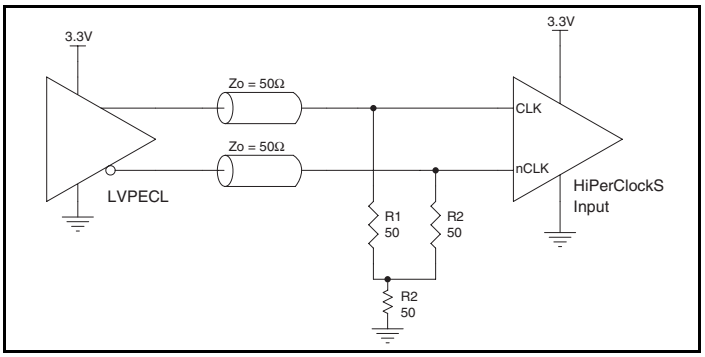


Figure 2B. HiPerClockS CLK/$\overline{CLK}$ Input Driven by a 3.3V LVPECL Driver

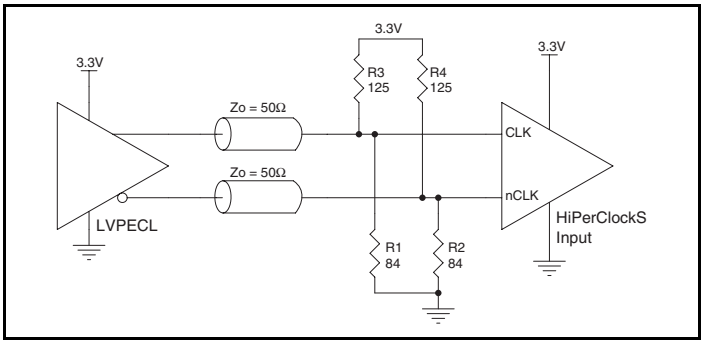


Figure 2C. HiPerClockS CLK/$\overline{CLK}$ Input Driven by a 3.3V LVPECL Driver

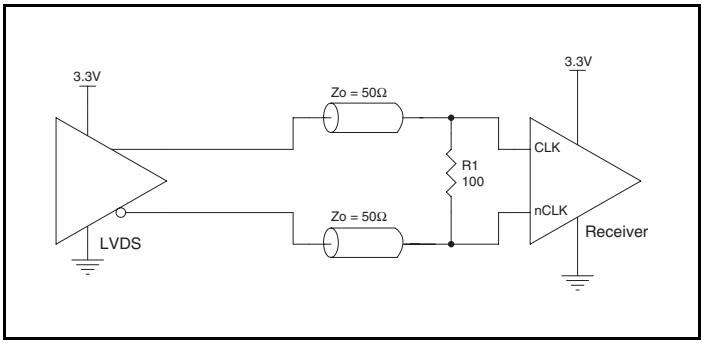


Figure 2D. HiPerClockS CLK/$\overline{CLK}$ Input Driven by a 3.3V LVDS Driver

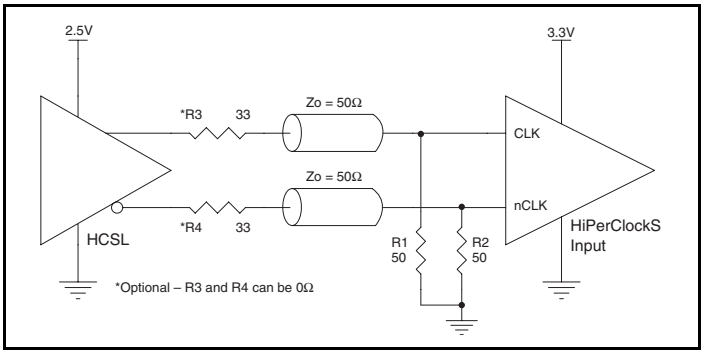


Figure 2E. HiPerClockS CLK/$\overline{CLK}$ Input Driven by a 3.3V HCSL Driver

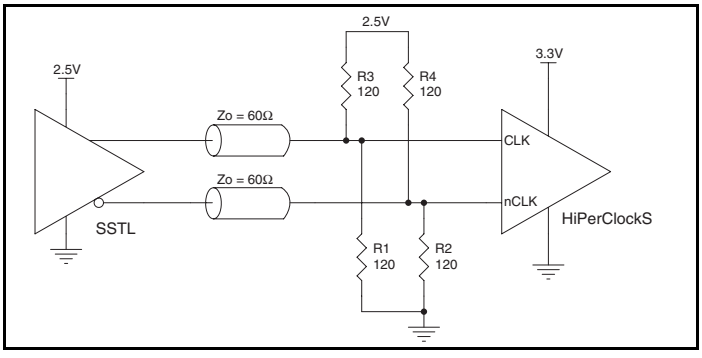


Figure 2F. HiPerClockS CLK/$\overline{CLK}$ Input Driven by a 2.5V SSTL Driver

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

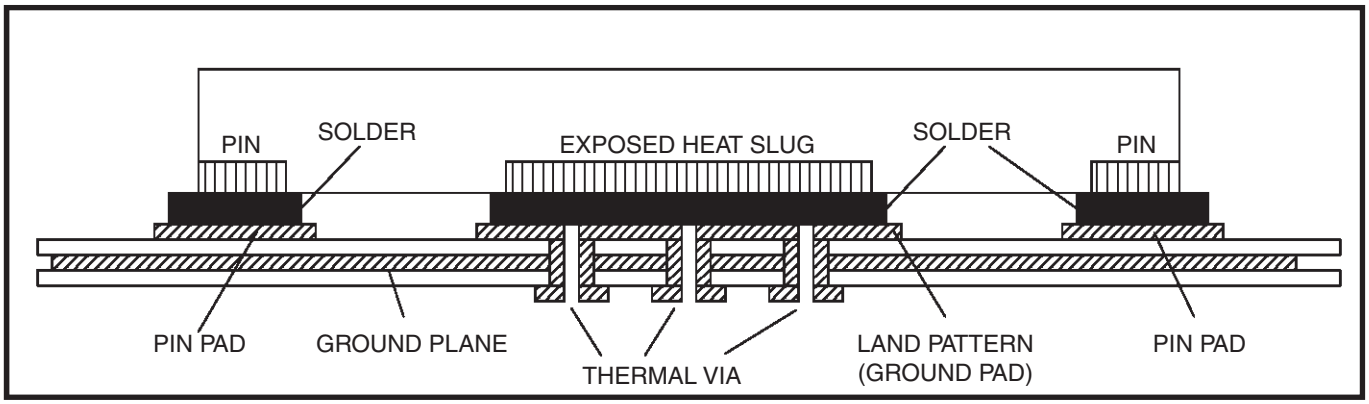


Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and $\overline{FOUT}$ are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

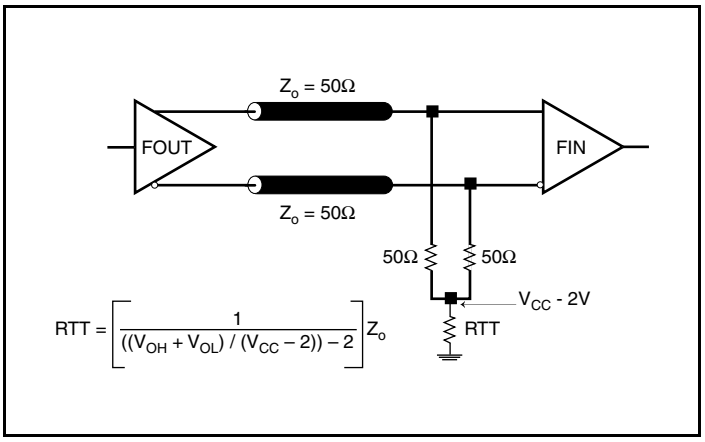


Figure 4A. 3.3V LVPECL Output Termination

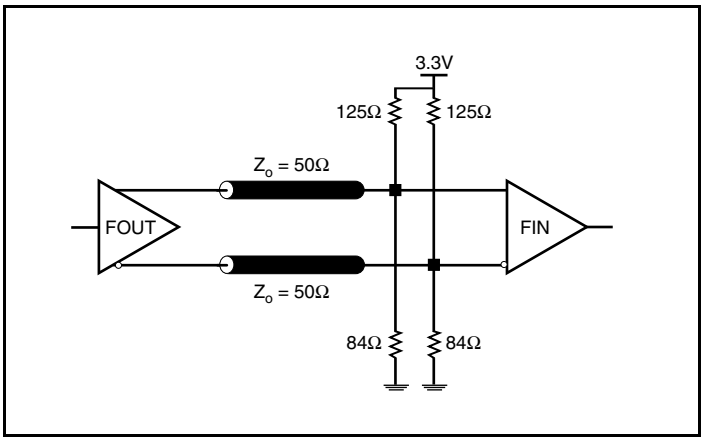


Figure 4B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

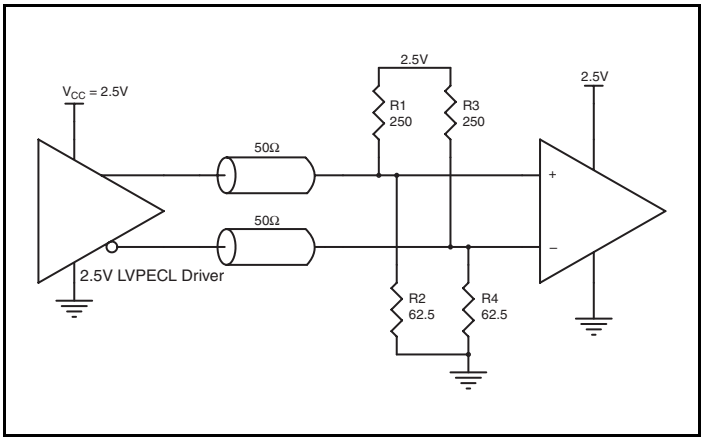


Figure 5A. 2.5V LVPECL Driver Termination Example

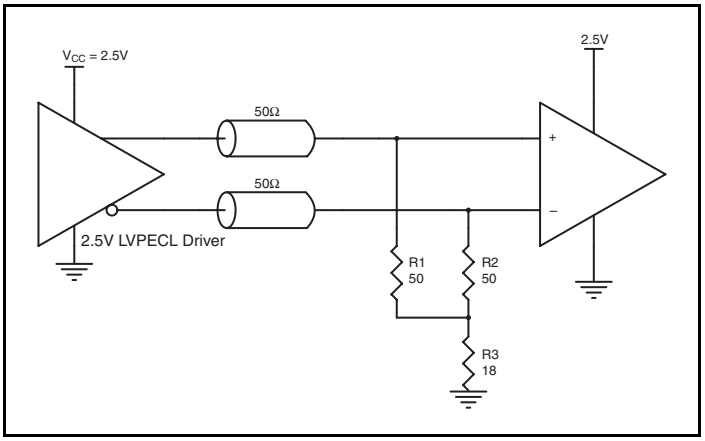


Figure 5B. 2.5V LVPECL Driver Termination Example

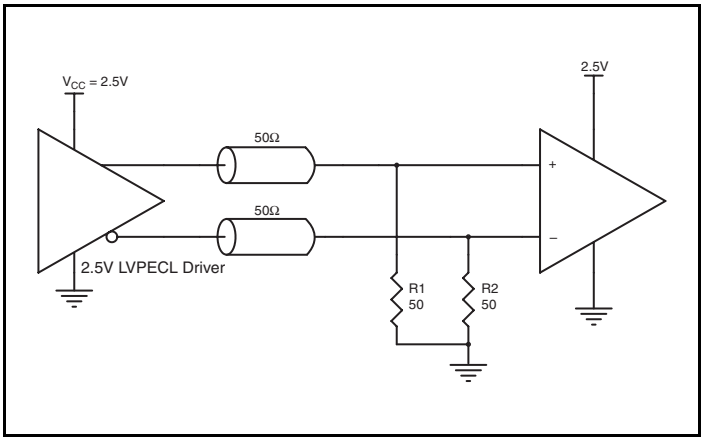
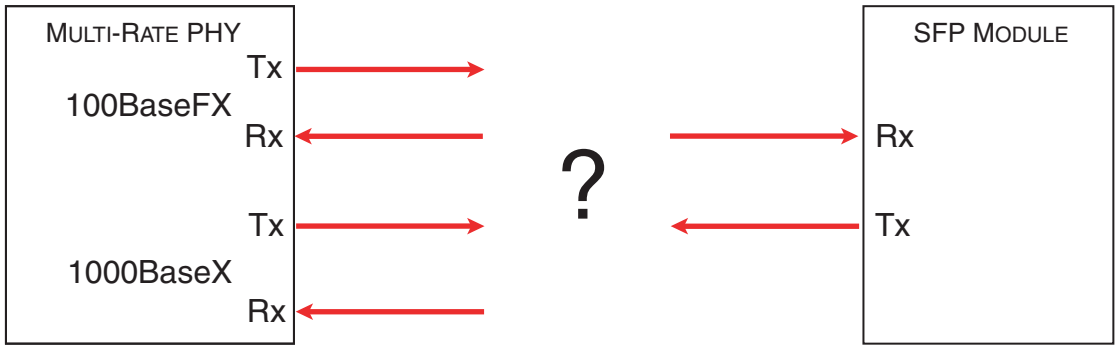


Figure 5C. 2.5V LVPECL Driver Termination Example

A Typical Application for the ICS85354

Used to connect a multi-rate PHY with the Tx/Rx pins of an SFP Module.

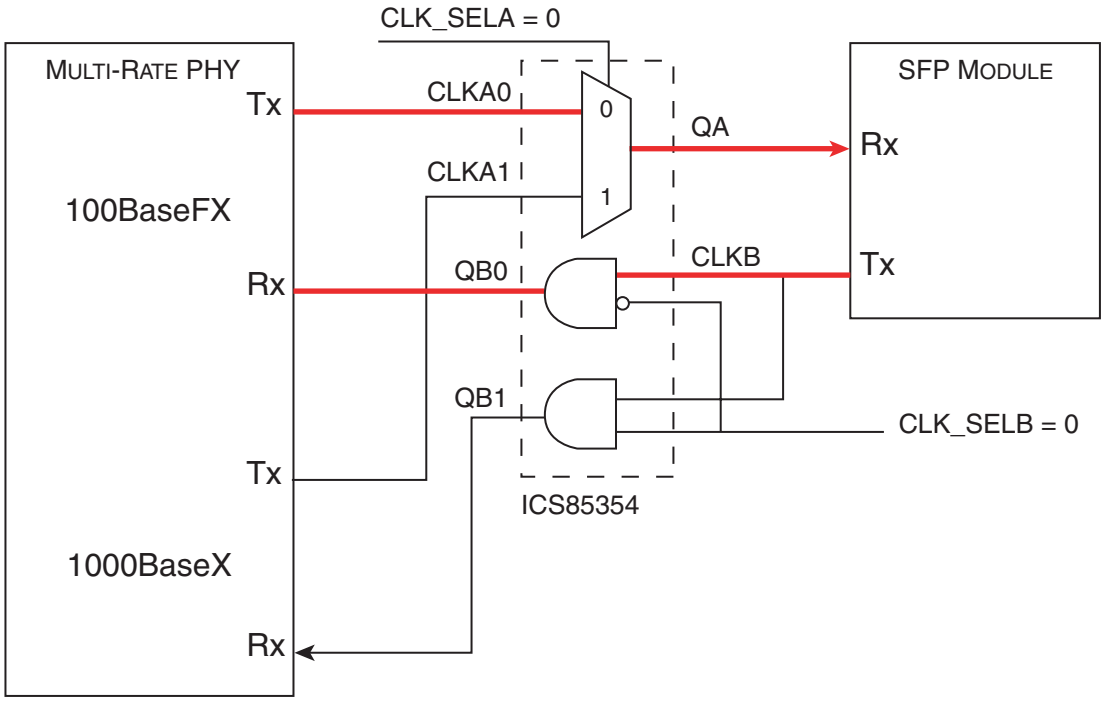
Problem Addressed: How to map the 2 Tx/Rx pairs of the multi-rate PHY to the single Tx/Rx pair on the SFP Module.



Mode 1, 100BaseX Connected to SFP

All lines are differential pairs, but drawn as single-ended to simplify the drawing.

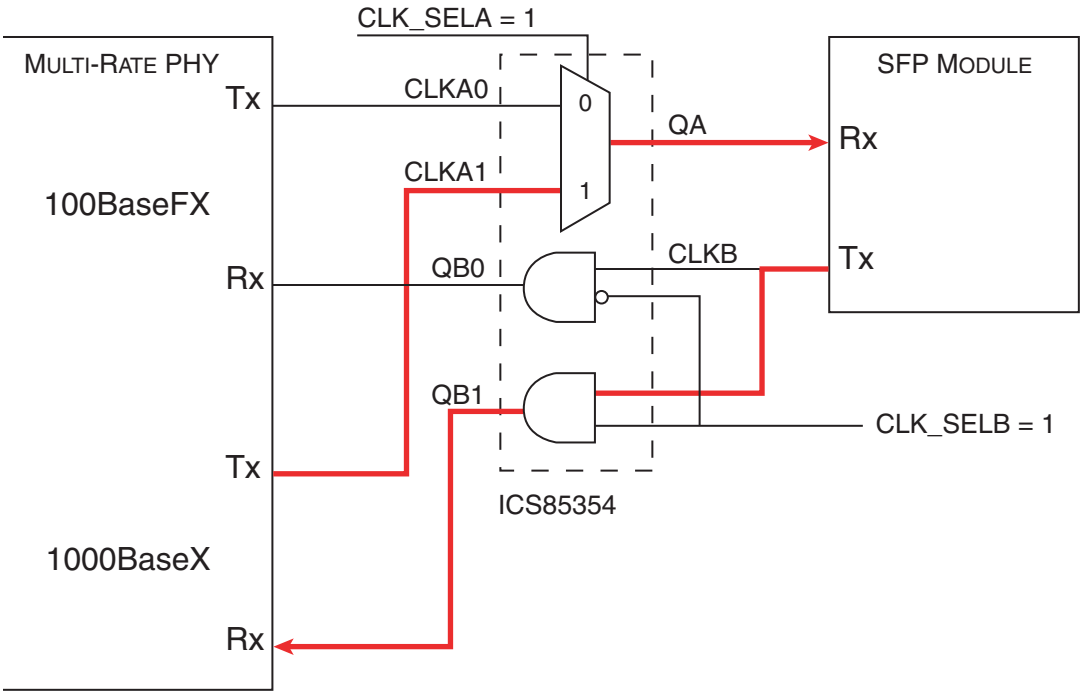
Bold red lines ——— are active connections highlighting the signal path.



Mode 2, 100BaseX Connected to SFP

All lines are differential pairs, but drawn as single-ended to simplify the drawing.

Bold red lines ——— are active connections highlighting the signal path.



Power Considerations

This section provides information on power dissipation and junction temperature for the ICS85354.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS85354 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 50mA = **173.25mW**
- Power $(outputs)_{MAX}$ = **27.83mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 27.83mW = **111.3mW**

Total Power$_{\_MAX}$ (3.3V, with all outputs switching) =173.25mW + 111.3mW = **284.55mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 65°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.285W * 51.5°C/W = 99.7°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6. Thermal Resitance θ_{JA} for 24 Lead TSSOP, Forced Convection

θ_{JA} **vs. Air Flow**			
Linear Feet per Minute	**0**		
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W		

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5.*

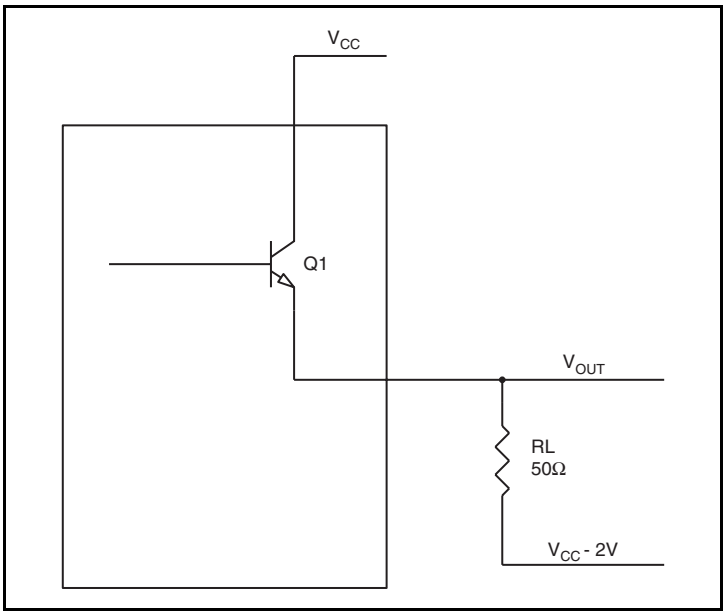


Figure 5. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} =$ **V_{CC_MAX} – 0.9V**
  ($V_{CC\_MAX} – V_{OH\_MAX}$) = **1.009V**
- For logic low, $V_{OUT} = V_{OL\_MAX} =$ **V_{CC_MAX} – 1.78V**
  ($V_{CC\_MAX} – V_{OL\_MAX}$) = **1.78V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 1.005V)/50Ω] * 1.005V =$ **20mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.78V)/50Ω] * 1.78V =$ **7.83mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **27.83mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFN

θ_{JA} by Velocity			
Linear Feet per Minute	**0**		
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W		

Transistor Count

The transistor count for ICS85354 is: 210

Package Outline and Package Dimension

Package Outline - K Suffix for 16 Lead VFQFN

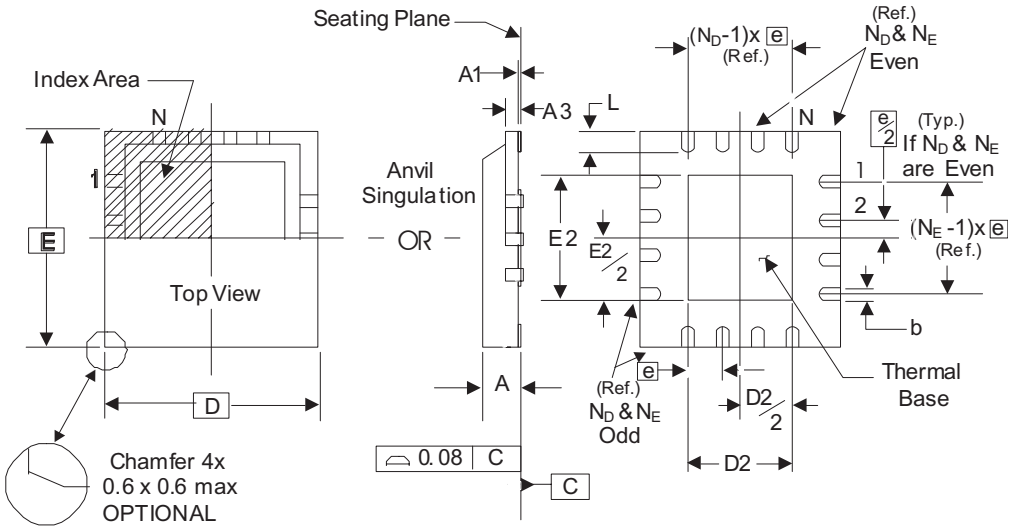


Table 8. Package Dimensions

JEDEC Variation: VEED-2/-4 All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A	0.80	1.00
A1	0	0.05
A3	0.25 Ref.	
b	0.18	0.30
N_D & N_E	4	
D & E	3.00 Basic	
D2 & E2	1.00	1.80
e	0.50 Basic	
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
85354AK	354A	16 Lead VFQFN	Tube	-40°C to 85°C
85354AKT	354A	16 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C
85354AKLF	54AL	“Lead-Free” 16 Lead VFQFN	Tube	-40°C to 85°C
85354AKLFT	54AL	“Lead-Free” 16 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T4D	4	LVPECL Characteristics Table - added min. & max. values to VOH and VOL.	5/6/05
C	T4D	4 6 7	LVPECL Characteristics Table - deleted VBB row. Added Recommendations for Unused Input and Output Pins. Corrected Differential Clock Input Interface section.	10/5/05
C	T9	16	Ordering Information Table - corrected Shipping Packaging from Tray to Tube.	3/14/06
C	T8	9 15	Added *Thermal Release Path Application Note.* Package Dimensions Table - corrected D2/E2 dimensions from 0.25min/1.25max. to 1.0min/1.8max. Updated format throughout the datasheet.	5/3/07
C		8 9 16	Updated *Differential Clock Input Interface* section. Updated *Thermal Release Path* section. Updated *Package Outline.*	2/19/08

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