



SKYWORKS®

# Si53314

## 1:6 LOW JITTER UNIVERSAL BUFFER/LEVEL TRANSLATOR WITH 2:1 INPUT MUX AND INDIVIDUAL OE (<1.25 GHz)

### Features

- 6 differential or 12 LVCMOS outputs
- Ultra-low additive jitter: 45 fs rms
- Wide frequency range: dc to 1.25 GHz
- Universal input with pin selectable output formats
- LVPECL, Low Power LVPECL, LVDS, CML, HCSL, LVCMOS
- 2:1 mux with hot-swappable inputs
- Individual output enable
- Independent  $V_{DD}$  and  $V_{DDO}$ : 1.8/2.5/3.3 V
- 1.2/1.5 V LVCMOS output support
- Excellent power supply noise rejection (PSRR)
- Selectable LVCMOS drive strength to tailor jitter and EMI performance
- Small size: 32-QFN (5x5 mm)
- RoHS compliant, Pb-free
- Industrial temperature range: -40 to +85 °C

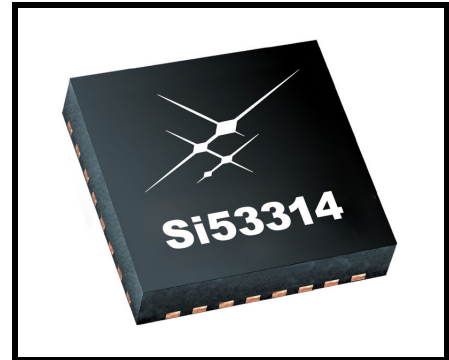
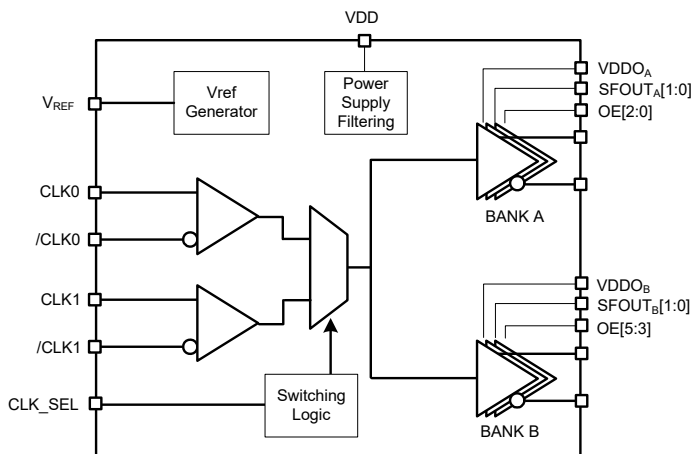
### Applications

- High-speed clock distribution
- Ethernet switch/router
- Optical Transport Network (OTN)
- SONET/SDH
- PCI Express Gen 1/2/3
- Storage
- Telecom
- Industrial
- Servers
- Backplane clock distribution

### Description

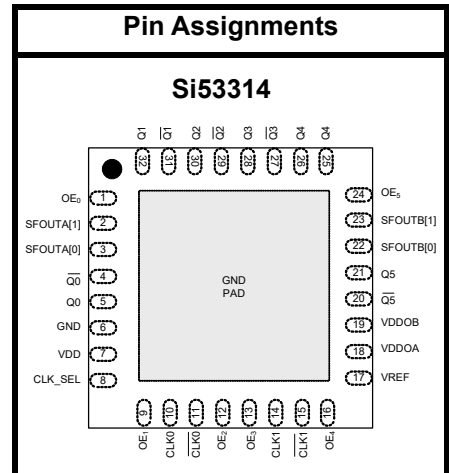
The Si53314 is an ultra low jitter six output differential buffer with pin-selectable output clock signal format and individual OE. The Si53314 features a 2:1 mux making it ideal for redundant clocking applications. The Si53314 utilizes Skyworks Solutions' advanced CMOS technology to fanout clocks from dc to 1.25 GHz with guaranteed low additive jitter, low skew, and low propagation delay variability. The Si53314 features minimal cross-talk and provides superior supply noise rejection, simplifying low jitter clock distribution in noisy environments. Independent core and output bank supply pins provide integrated level translation without the need for external circuitry.

### Functional Block Diagram



### Ordering Information:

See page 27.



Patents pending

## TABLE OF CONTENTS

---

Section	Page
<b>1. Electrical Specifications</b>	<b>3</b>
<b>2. Functional Description</b>	<b>11</b>
2.1. Universal, Any-Format Input	11
2.2. Input Bias Resistors	13
2.3. Input Clock Voltage Reference (VREF)	13
2.4. Universal, Any-Format Output Buffer	14
2.5. Input Mux and Output Enable Logic	15
2.6. Power Supply ( $V_{DD}$ and $V_{DDOX}$ )	15
2.7. Output Clock Termination Options	16
2.8. AC Timing Waveforms	19
2.9. Typical Phase Noise Performance	20
2.10. Input Mux Noise Isolation	23
2.11. Power Supply Noise Rejection	23
<b>3. Pin Descriptions</b>	<b>24</b>
<b>4. Ordering Guide</b>	<b>27</b>
<b>5. Package Outline</b>	<b>28</b>
5.1. 5x5 mm 32-QFN Package Diagram	28
<b>6. PCB Land Pattern</b>	<b>29</b>
6.1. 5x5 mm 32-QFN Package Land Pattern	29
<b>7. Top Marking</b>	<b>30</b>
7.1. Si53314 Top Marking	30
7.2. Top Marking Explanation	30
<b>Document Change List</b>	<b>31</b>
<b>Contact Information</b>	<b>32</b>

## 1. Electrical Specifications

**Table 1. Recommended Operating Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Operating Temperature	$T_A$		-40	—	85	°C
Supply Voltage Range*	$V_{DD}$	LVDS, CML	1.71	1.8	1.89	V
			2.38	2.5	2.63	V
			2.97	3.3	3.63	V
		LVPECL, low power LVPECL, LVCMOS	2.38	2.5	2.63	V
			2.97	3.3	3.63	V
		HCSL	2.97	3.3	3.63	V
Output Buffer Supply Voltage*	$V_{DDOX}$	LVDS, CML, LVCMOS	1.71	1.8	1.89	V
			2.38	2.5	2.63	V
			2.97	3.3	3.63	V
		LVPECL, low power LVPECL	2.38	2.5	2.63	V
			2.97	3.3	3.63	V
		HCSL	2.97	3.3	3.63	V

**\*Note:** Core supply  $V_{DD}$  and output buffer supplies  $V_{DDOX}$  are independent. LVCMOS clock input is not supported for  $V_{DD} = 1.8V$  but is supported for LVCMOS clock output for  $V_{DDOX} = 1.8V$ . LVCMOS outputs at 1.5V and 1.2V can be supported via a simple resistor divider network. See “2.7.1. LVCMOS Output Termination To Support 1.5 and 1.2 V”

**Table 2. Input Clock Specifications**

( $V_{DD} = 1.8V \pm 5\%$ ,  $2.5V \pm 5\%$ , or  $3.3V \pm 10\%$ ,  $T_A = -40$  to  $85$  °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Input Common Mode Voltage	$V_{CM}$	$V_{DD} = 2.5V \pm 5\%$ , $3.3V \pm 10\%$	0.05	—	—	V
Differential Input Swing (peak-to-peak)	$V_{IN}$		0.2	—	2.2	V
LVCMOS Input High Voltage	$V_{IH}$	$V_{DD} = 2.5V \pm 5\%$ , $3.3V \pm 10\%$	$V_{DD} \times 0.7$	—	—	V
LVCMOS Input Low Voltage	$V_{IL}$	$V_{DD} = 2.5V \pm 5\%$ , $3.3V \pm 10\%$	—	—	$V_{DD} \times 0.3$	V
Input Capacitance	$C_{IN}$	CLK0 and CLK1 pins with respect to GND	—	5	—	pF

**Table 3. DC Common Characteristics**

( $V_{DD} = 1.8\text{ V} \pm 5\%$ ,  $2.5\text{ V} \pm 5\%$ , or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40\text{ to }85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	$I_{DD}$		—	65	100	mA
Output Buffer Supply Current (Per Clock Output) @100 MHz (diff) @200 MHz (CMOS)	$I_{DDOX}$	LVPECL (3.3 V)	—	35	—	mA
		Low Power LVPECL (3.3 V)*	—	35	—	mA
		LVDS (3.3 V)	—	20	—	mA
		CML (3.3 V)	—	35	—	mA
		HCSL, 100 MHz, 2 pF load (3.3 V)	—	35	—	mA
		CMOS (1.8 V, SFOUT = Open/0), per output, $C_L = 5\text{ pF}$ , 200 MHz	—	5	—	mA
		CMOS (2.5 V, SFOUT = Open/0), per output, $C_L = 5\text{ pF}$ , 200 MHz	—	8	—	mA
CMOS (3.3 V, SFOUT = 0/1), per output, $C_L = 5\text{ pF}$ , 200 MHz	—	15	—	mA		
Input Clock Voltage Reference	$V_{REF}$	$V_{REF}$ pin $I_{REF} = \pm 500\text{ }\mu\text{A}$	—	$V_{DD}/2$	—	V
Input High Voltage	$V_{IH}$	SFOUTx, CLK_SEL, OEx	$0.8 \times V_{DD}$	—	—	V
Input Mid Voltage	$V_{IM}$	SFOUTx, 3-level input pins	$0.45 \times V_{DD}$	$0.5 \times V_{DD}$	$0.55 \times V_{DD}$	V
Input Low Voltage	$V_{IL}$	SFOUTx, CLK_SEL, OEx	—	—	$0.2 \times V_{DD}$	V
Internal Pull-down Resistor	$R_{DOWN}$	CLK_SEL, SFOUTx	—	25	—	$k\Omega$
Internal Pull-up Resistor	$R_{UP}$	OEx, SFOUTx	—	25	—	$k\Omega$

**\*Note:** Low-power LVPECL mode supports an output termination scheme that will reduce overall system power.

**Table 4. Output Characteristics (LVPECL)** $(V_{DDOX} = 2.5\text{ V} \pm 5\%$ , or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output DC Common Mode Voltage	$V_{COM}$		$V_{DDOX} - 1.595$	—	$V_{DDOX} - 1.245$	V
Single-Ended Output Swing*	$V_{SE}$		0.40	0.80	1.050	V

\*Note: Unused outputs can be left floating. Do not short unused outputs to ground.

**Table 5. Output Characteristics (Low Power LVPECL)** $(V_{DDOX} = 2.5\text{ V} \pm 5\%$ , or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output DC Common Mode Voltage	$V_{COM}$	$R_L = 100\ \Omega$ across $Q_n$ and $\overline{Q_n}$	$V_{DDOX} - 1.895$		$V_{DDOX} - 1.275$	V
Single-Ended Output Swing	$V_{SE}$	$R_L = 100\ \Omega$ across $Q_n$ and $\overline{Q_n}$	0.20	0.60	0.85	V

**Table 6. Output Characteristics—CML** $(V_{DDOX} = 1.8\text{ V} \pm 5\%$ ,  $2.5\text{ V} \pm 5\%$ , or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single-Ended Output Swing	$V_{SE}$	Terminated as shown in Figure 8 (CML termination).	200	400	550	mV

**Table 7. Output Characteristics—LVDS** $(V_{DDOX} = 1.8\text{ V} \pm 5\%$ ,  $2.5\text{ V} \pm 5\%$ , or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single-Ended Output Swing	$V_{SE}$	$R_L = 100\ \Omega$ across $Q_N$ and $\overline{Q_N}$	200	—	490	mV
Output Common Mode Voltage ( $V_{DDO} = 2.5\text{ V}$ or $3.3\text{ V}$ )	$V_{COM1}$	$V_{DDOX} = 2.38$ to $2.63\text{ V}$ , $2.97$ to $3.63\text{ V}$ , $R_L = 100\ \Omega$ across $Q_N$ and $\overline{Q_N}$	1.10	1.25	1.35	V
Output Common Mode Voltage ( $V_{DDO} = 1.8\text{ V}$ )	$V_{COM2}$	$V_{DDOX} = 1.71$ to $1.89\text{ V}$ , $R_L = 100\ \Omega$ across $Q_N$ and $\overline{Q_N}$	0.85	0.97	1.25	V

# Si53314

**Table 8. Output Characteristics—LVCMOS**

( $V_{DDOX} = 1.8\text{ V} \pm 5\%$ ,  $2.5\text{ V} \pm 5\%$ , or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage High*	$V_{OH}$		$0.75 \times V_{DDOX}$	—	—	V
Output Voltage Low*	$V_{OL}$		—	—	$0.25 \times V_{DDOX}$	V

\*Note:  $I_{OH}$  and  $I_{OL}$  per the Output Signal Format Table for specific  $V_{DDOX}$  and SFOUTX settings.

**Table 9. Output Characteristics—HCSL**

( $V_{DDOX} = 3.3\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage High	$V_{OH}$	$R_L = 50\ \Omega$ to GND	550	700	900	mV
Output Voltage Low	$V_{OL}$	$R_L = 50\ \Omega$ to GND	-150	0	150	mV
Single-Ended Output Swing	$V_{SE}$	$R_L = 50\ \Omega$ to GND	450	700	850	mV
Crossing Voltage	$V_C$	$R_L = 50\ \Omega$ to GND	250	350	550	mV

**Table 10. AC Characteristics**

( $V_{DD} = V_{DDOX} = 1.8\text{ V} \pm 5\%$ ,  $2.5\text{ V} \pm 5\%$ , or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency	F	LVPECL, low power LVPECL, LVDS, CML, HCSL	DC	—	1250	GHz
		LVCMOS	DC	—	200	MHz
Duty Cycle Note: 50% input duty cycle.	$D_C$	200 MHz, 20/80% $T_R/T_F < 10\%$ of period (LVCMOS) (12 mA drive)	40	50	60	%
		20/80% $T_R/T_F < 10\%$ of period (Differential)	47	50	53	%
Minimum Input Clock Slew Rate	SR	Required to meet prop delay and additive jitter specifications (20–80%)	0.75	—	—	V/ns

**Notes:**

1. HCSL measurements were made with receiver termination. See Figure 8 on page 17.
2. Output to Output skew specified for outputs with an identical configuration.
3. Defined as skew between any output on different devices operating at the same supply voltage, temperature, and equal load condition. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
4. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to  $V_{DDOX}$  ( $3.3\text{ V} = 100\text{ mV}_{PP}$ ) and noise spur amplitude measured. See "AN491: Power Supply Rejection for Low-Jitter Clocks" for further details.

**Table 10. AC Characteristics (Continued)** $(V_{DD} = V_{DDOX} = 1.8\text{ V} \pm 5\%, 2.5\text{ V} \pm 5\%, \text{ or } 3.3\text{ V} \pm 10\%, T_A = -40\text{ to } 85\text{ }^\circ\text{C})$ 

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Rise/Fall Time	$T_R/T_F$	LVDS, 20/80%	—	—	325	ps
		LVPECL, 20/80%	—	—	350	ps
		HCSL <sup>1</sup> , 20/80%	—	—	280	ps
		CML, 20/80%	—	—	350	ps
		Low-Power LVPECL, 20/80%	—	—	325	ps
		LVC MOS 200 MHz, 20/80%, 2 pF load	—	—	750	ps
Minimum Input Pulse Width	$T_W$		360	—	—	ps
Propagation Delay	$T_{PLH}, T_{PHL}$	LVC MOS (12mA drive with no load)	1250	2000	2750	ps
		LVPECL	600	800	1000	ps
		LVDS	600	800	1000	ps
Output Enable Time	$T_{EN}$	F = 1 MHz	—	2500	—	ns
		F = 100 MHz	—	30	—	ns
		F = 725 MHz	—	5	—	ns
Output Disable Time	$T_{DIS}$	F = 1 MHz	—	2000	—	ns
		F = 100 MHz	—	30	—	ns
		F = 725 MHz	—	5	—	ns
Output to Output Skew <sup>2</sup>	$T_{SK}$	LVC MOS (12 mA drive to no load)	—	50	120	ps
		LVPECL	—	35	70	ps
		LVDS	—	35	70	ps
Part to Part Skew <sup>3</sup>	$T_{PS}$	Differential	—	—	150	ps
Power Supply Noise Rejection <sup>4</sup>	PSRR	10 kHz sinusoidal noise	—	-65	—	dBc
		100 kHz sinusoidal noise	—	-63	—	dBc
		500 kHz sinusoidal noise	—	-60	—	dBc
		1 MHz sinusoidal noise	—	-55	—	dBc

**Notes:**

1. HCSL measurements were made with receiver termination. See Figure 8 on page 17.
2. Output to Output skew specified for outputs with an identical configuration.
3. Defined as skew between any output on different devices operating at the same supply voltage, temperature, and equal load condition. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
4. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to  $V_{DDOX}$  ( $3.3\text{ V} = 100\text{ mV}_{PP}$ ) and noise spur amplitude measured. See "AN491: Power Supply Rejection for Low-Jitter Clocks" for further details.

**Table 11. Additive Jitter, Differential Clock Input**

V <sub>DD</sub>	Input <sup>1,2</sup>				Output	Additive Jitter (fs rms, 12 kHz to 20 MHz) <sup>3</sup>	
	Freq (MHz)	Clock Format	Amplitude V <sub>IN</sub> (Single-Ended, Peak-to-Peak)	Differential 20%-80% Slew Rate (V/ns)	Clock Format	Typ	Max
3.3	725	Differential	0.15	0.637	LVPECL	45	65
3.3	725	Differential	0.15	0.637	LVDS	50	65
3.3	156.25	Differential	0.5	0.458	LVPECL	160	185
3.3	156.25	Differential	0.5	0.458	LVDS	150	200
2.5	725	Differential	0.15	0.637	LVPECL	45	65
2.5	725	Differential	0.15	0.637	LVDS	50	65
2.5	156.25	Differential	0.5	0.458	LVPECL	145	185
2.5	156.25	Differential	0.5	0.458	LVDS	145	195

**Notes:**

1. For best additive jitter results, use the fastest slew rate possible. See “AN766: Understanding and Optimizing Clock Buffer’s Additive Jitter Performance” for more information.
2. AC-coupled differential inputs.
3. Measured differentially using a balun at the phase noise analyzer input. See Figure 1.



Table 12. Additive Jitter, Single-Ended Clock Input

V <sub>DD</sub>	Input <sup>1,2</sup>				Output	Additive Jitter (fs rms, 12 kHz to 20 MHz) <sup>3</sup>	
	Freq (MHz)	Clock Format	Amplitude V <sub>IN</sub> (single-ended, peak to peak)	SE 20%-80% Slew Rate (V/ns)		Clock Format	Typ
3.3	200	Single-ended	1.70	1	LVC MOS <sup>4</sup>	120	160
3.3	156.25	Single-ended	2.18	1	LVPECL	160	185
3.3	156.25	Single-ended	2.18	1	LVDS	150	200
3.3	156.25	Single-ended	2.18	1	LVC MOS <sup>4</sup>	130	180
2.5	200	Single-ended	1.70	1	LVC MOS <sup>5</sup>	120	160
2.5	156.25	Single-ended	2.18	1	LVPECL	145	185
2.5	156.25	Single-ended	2.18	1	LVDS	145	195
2.5	156.25	Single-ended	2.18	1	LVC MOS <sup>5</sup>	140	180

**Notes:**

1. For best additive jitter results, use the fastest slew rate possible. See “AN766: Understanding and Optimizing Clock Buffer’s Additive Jitter Performance” for more information.
2. DC-coupled single-ended inputs.
3. Measured differentially using a balun at the phase noise analyzer input. See Figure 1.
4. Drive Strength: 12 mA, 3.3 V (SFOUT = 11). LVC MOS jitter is measured single-ended.
5. Drive Strength: 9 mA, 2.5 V (SFOUT = 11). LVC MOS jitter is measured single-ended.

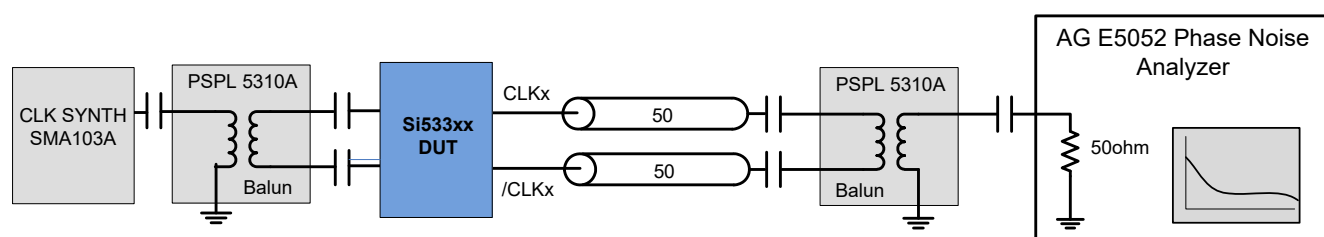


Figure 1. Differential Measurement Method Using a Balun

**Table 13. Thermal Conditions**

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance, Junction to Ambient	$\theta_{JA}$	Still air	49.6	°C/W
Thermal Resistance, Junction to Case	$\theta_{JC}$	Still air	32.3	°C/W

**Table 14. Absolute Maximum Ratings**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage Temperature	$T_S$		-55	—	150	°C
Supply Voltage	$V_{DD}$		-0.5	—	3.8	V
Input Voltage	$V_{IN}$		-0.5	—	$V_{DD} + 0.3$	V
Output Voltage	$V_{OUT}$		—	—	$V_{DD} + 0.3$	V
ESD Sensitivity	HBM	HBM, 100 pF, 1.5 k $\Omega$	—	—	2000	V
ESD Sensitivity	CDM		—	—	500	V
Peak Soldering Reflow Temperature	$T_{PEAK}$	Pb-Free; Solder reflow profile per JEDEC J-STD-020	—	—	260	°C
Maximum Junction Temperature	$T_J$		—	—	125	°C

**Note:** Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

## 2. Functional Description

The Si53314 is a low jitter, low skew 1:6 differential buffer with an integrated 2:1 input mux and individual OE control. The device has a universal input that accepts most common differential or LVCMOS input signals. A clock select pin control is used to select the active input clock. The selected clock input is routed to two independent banks of outputs. Each output bank features control pins to select signal format setting and LVCMOS drive strength. In addition, each clock output has an independent OE pin for individual clock enable/disable.

### 2.1. Universal, Any-Format Input

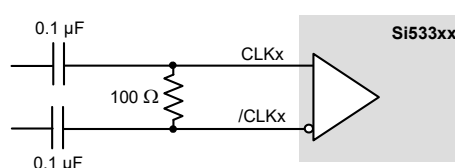
The universal input stage enables simple interfacing to a wide variety of clock formats, including LVPECL, low-power LVPECL, LVCMOS, LVDS, HCSL, and CML. Tables 15 and 16 summarize the various ac- and dc-coupling options supported by the device. For the best high-speed performance, the use of differential formats is recommended. For both single-ended and differential input clocks, the fastest possible slew rate is recommended as low slew rates can increase the noise floor and degrade jitter performance. Though not required, a minimum slew rate of 0.75 V/ns is recommended for differential formats and 1.0 V/ns for single-ended formats. See “AN766: Understanding and Optimizing Clock Buffer’s Additive Jitter Performance” for more information.

**Table 15. LVPECL, LVCMOS, and LVDS Input Clock Options**

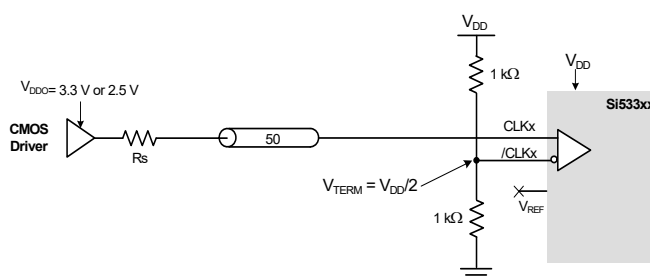
	LVPECL		LVCMOS		LVDS	
	AC-Couple	DC-Couple	AC-Couple	DC-Couple	AC-Couple	DC-Couple
1.8 V	N/A	N/A	No	No	Yes	No
2.5/3.3 V	Yes	Yes	No	Yes	Yes	Yes

**Table 16. HCSL and CML Input Clock Options**

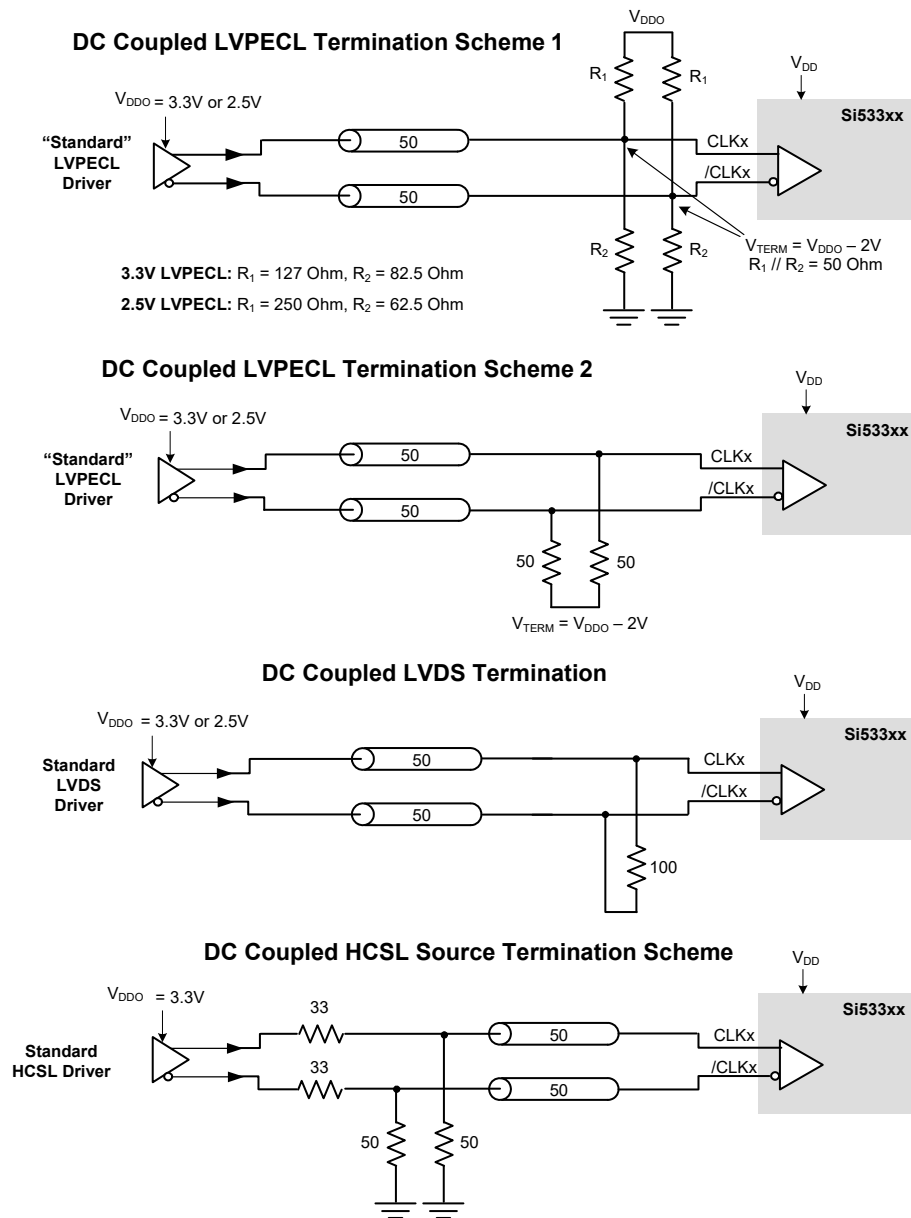
	HCSL		CML	
	AC-Couple	DC-Couple	AC-Couple	DC-Couple
1.8 V	No	No	Yes	No
2.5/3.3 V	Yes (3.3 V)	Yes (3.3 V)	Yes	No



**Figure 2. Differential HCSL, LVPECL, Low-Power LVPECL, LVDS, CML AC-Coupled Input Termination**



**Figure 3. LVCMOS DC-Coupled Input Termination**

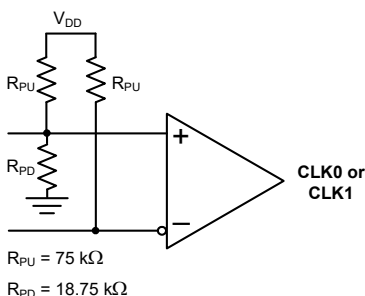


Note: 33 Ohm series termination is optional depending on the location of the receiver.

**Figure 4. Differential DC-Coupled Input Terminations**

## 2.2. Input Bias Resistors

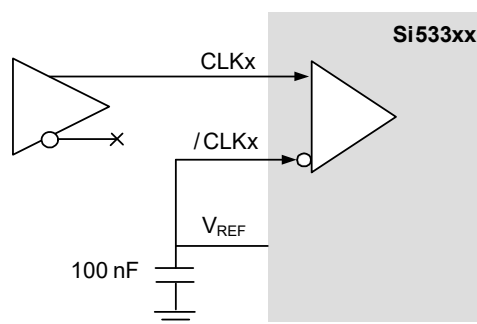
Internal bias resistors ensure a differential output low condition in the event that the clock inputs are not connected. The non-inverting input is biased with a 18.75 k $\Omega$  pull-down to GND and a 75 k $\Omega$  pull-up to V<sub>DD</sub>. The inverting input is biased with a 75 k $\Omega$  pull-up to V<sub>DD</sub>.



**Figure 5. Input Bias Resistors**

## 2.3. Input Clock Voltage Reference (V<sub>REF</sub>)

The V<sub>REF</sub> pin is used to bias the input receiver when a differential input clock is terminated as a single-ended reference clock to the device. Connect the single-ended input to either CLK0 or CLK1. Use the recommended input termination and bias circuit as shown in Figure 3. Note that the V<sub>REF</sub> pin should be left floating when LVCMOS or differential clocks are used.



**Figure 6. Using Voltage Reference with Single-Ended Input Clock**

## 2.4. Universal, Any-Format Output Buffer

The highly flexible output drivers support a wide range of clock signal formats, including LVPECL, low power LVPECL, LVDS, CML, HCSL, and LVCMOS. SFOUTx[1] and SFOUTx[0] are 3-level inputs that can be pin-strapped to select the Bank A and Bank B clock signal formats independently. This feature enables the device to be used for format translation in addition to clock distribution, minimizing the number of unique buffer part numbers required in a typical application and simplifying design reuse. For EMI reduction applications, four LVCMOS drive strength options are available for each  $V_{DDO}$  setting.

**Table 17. Output Signal Format Selection**

SFOUTX[1]	SFOUTX[0]	$V_{DDOX} = 3.3 \text{ V}$	$V_{DDOX} = 2.5 \text{ V}$	$V_{DDOX} = 1.8 \text{ V}$
Open*	Open*	LVPECL	LVPECL	N/A
0	0	LVDS	LVDS	LVDS
0	1	LVCMOS, 24 mA drive	LVCMOS, 18 mA drive	LVCMOS, 12 mA drive
1	0	LVCMOS, 18 mA drive	LVCMOS, 12 mA drive	LVCMOS, 9 mA drive
1	1	LVCMOS, 12 mA drive	LVCMOS, 9 mA drive	LVCMOS, 6 mA drive
Open*	0	LVCMOS, 6 mA drive	LVCMOS, 4 mA drive	LVCMOS, 2 mA drive
Open*	1	LVPECL low power	LVPECL low power	N/A
0	Open*	CML	CML	CML
1	Open*	HCSL	N/A	N/A

**\*Note:** SFOUTx are 3-level input pins. Tie low for "0" setting. Tie high for "1" setting. When left open, the pin floats to  $V_{DD}/2$ .

## 2.5. Input Mux and Output Enable Logic

Two clock inputs for applications that need to select between one of two clock sources. The CLK\_SEL pin selects the active clock input. The table below summarizes the input and output clock based on the input mux and output enable pin settings.

**Table 18. Input Mux and Output Enable Logic**

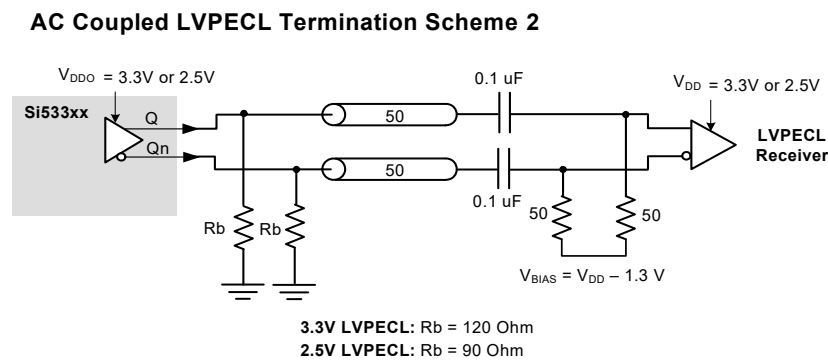
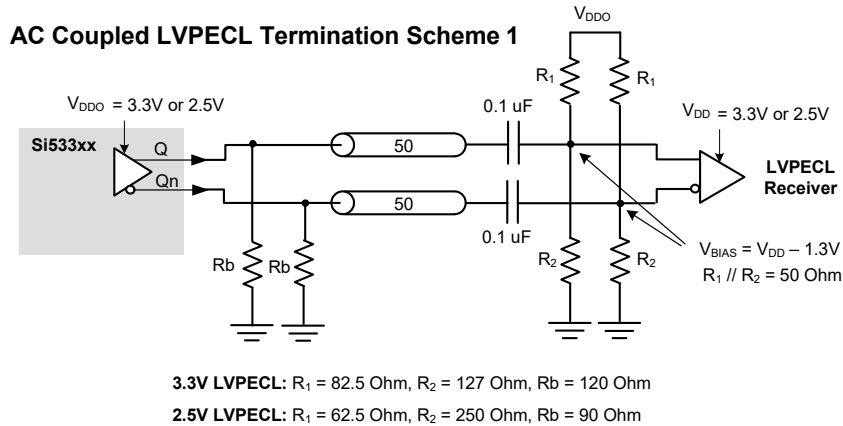
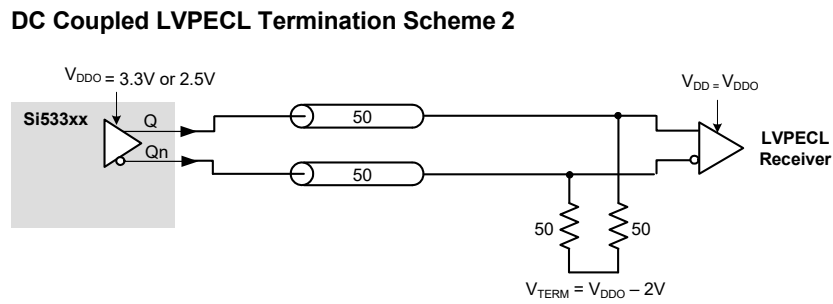
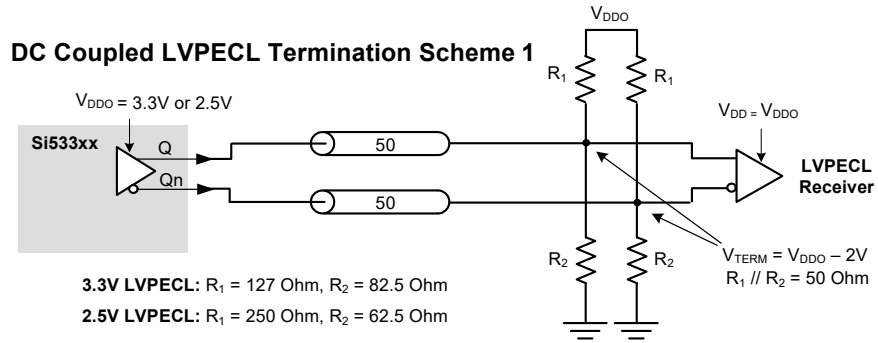
CLK_SEL	CLK0	CLK1	OE <sup>1</sup>	Q <sup>2</sup>
L	L	X	H	L
L	H	X	H	H
H	X	L	H	L
H	X	H	H	H
X	X	X	L	L <sup>3</sup>
<b>Notes:</b>				
1. Output enable active high				
2. On the next negative transition of CLK0 or CLK1.				
3. Single-end: Q = low, $\overline{Q}$ = low Differential: Q = low, $\overline{Q}$ = high				

## 2.6. Power Supply ( $V_{DD}$ and $V_{DDOX}$ )

The device includes separate core ( $V_{DD}$ ) and output driver supplies ( $V_{DDOX}$ ). This feature allows the core to operate at a lower voltage than  $V_{DDO}$ , reducing current consumption in mixed supply applications. The core  $V_{DD}$  supports 3.3 V, 2.5 V, or 1.8 V. Each output bank has its own  $V_{DDOX}$  supply, supporting 3.3 V, 2.5 V, or 1.8 V.

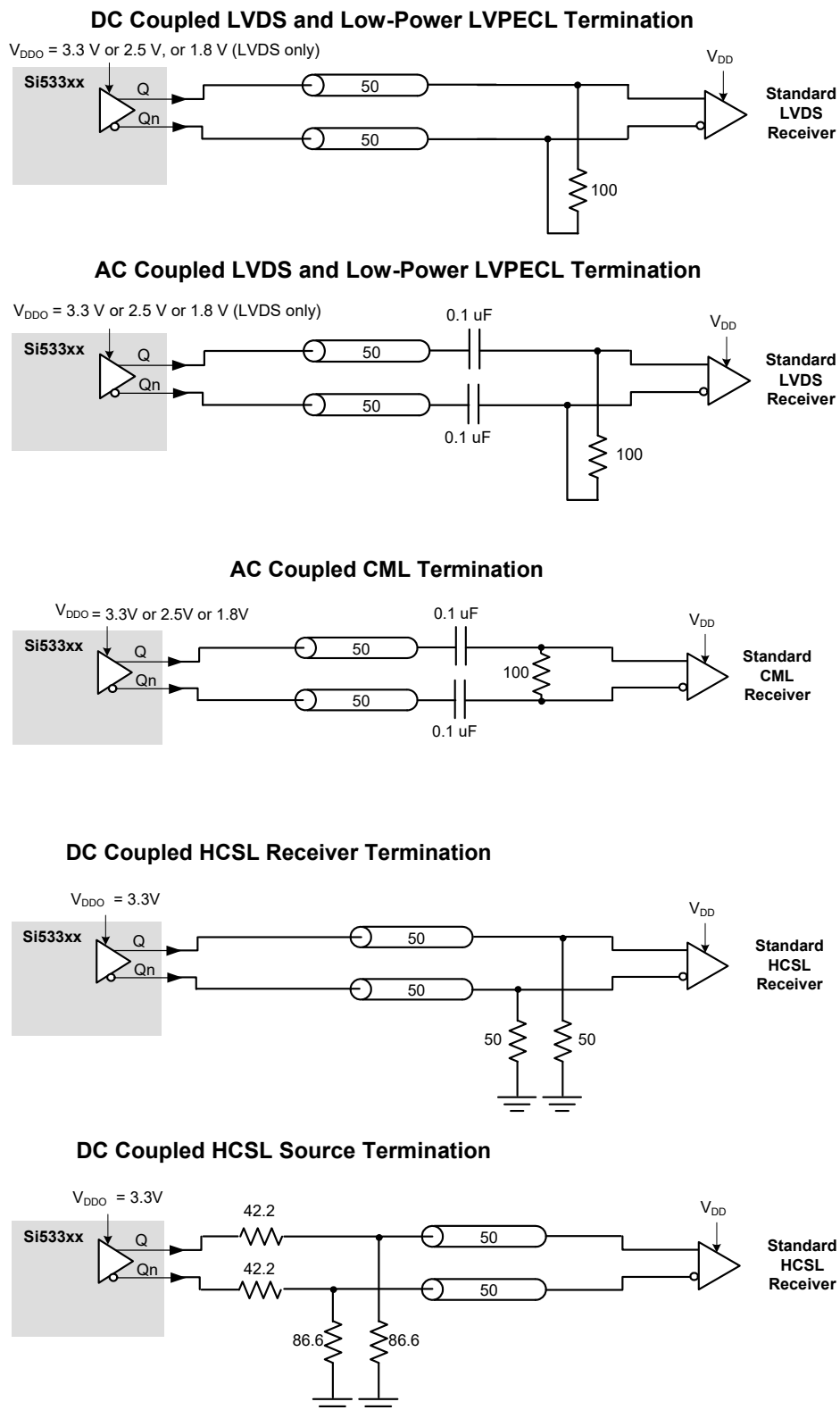
## 2.7. Output Clock Termination Options

The recommended output clock termination options are shown below.

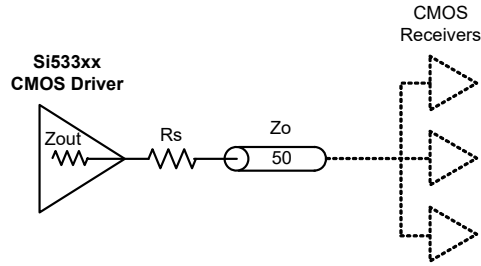


**Figure 7. LVPECL Output Termination**





**Figure 8. LVDS, CML, HCSL, and Low-Power LVPECL Output Termination**



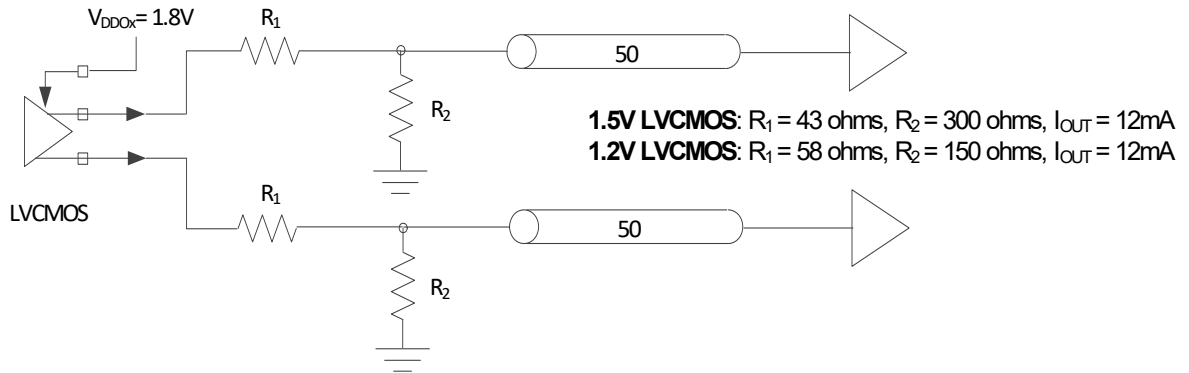
**Figure 9. LVC MOS Output Termination**

**Table 19. Recommended LVC MOS  $R_S$  Series Termination**

SFOUTX[1]	SFOUTX[0]	$R_S$ (ohms)		
		3.3 V	2.5 V	1.8 V
0	1	33	33	33
1	0	33	33	33
1	1	33	33	0
Open	0	0	0	0

### 2.7.1. LVC MOS Output Termination To Support 1.5 and 1.2 V

LVC MOS clock outputs are natively supported at 1.8, 2.5, and 3.3 V. However, 1.2 and 1.5V LVC MOS clock outputs can be supported via a simple resistor divider network that will translate the buffer’s 1.8V output to a lower voltage as shown in Figure 10.



**Figure 10. 1.5V and 1.2V LVC MOS Low-Voltage Output Termination**

## 2.8. AC Timing Waveforms

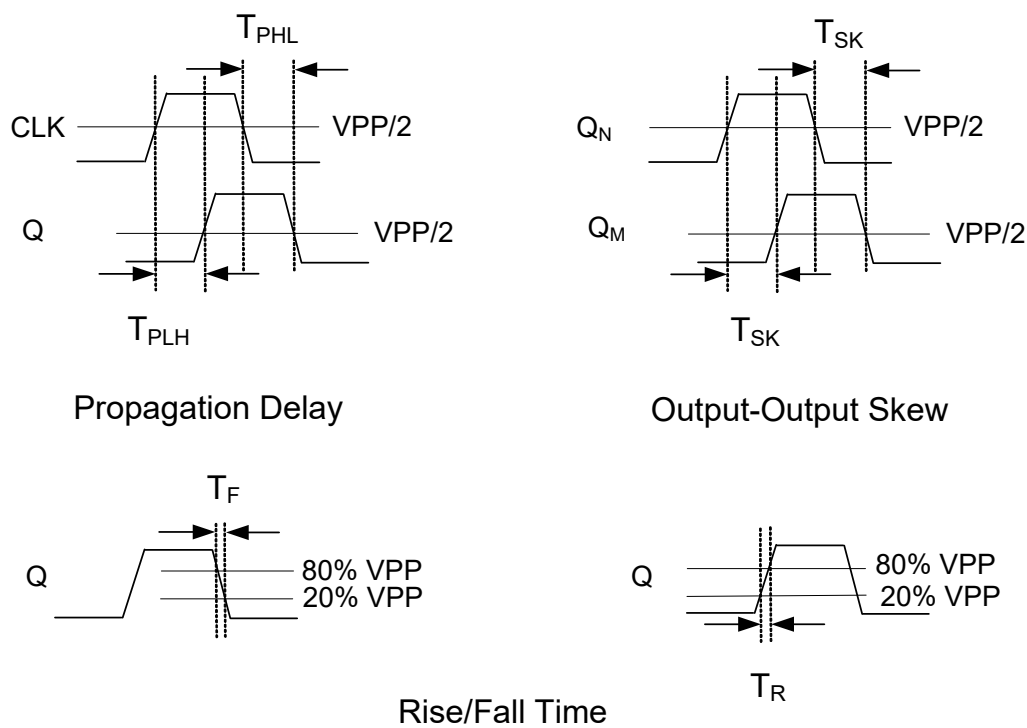


Figure 11. AC Waveforms

## 2.9. Typical Phase Noise Performance

Each of the following three figures shows three phase noise plots superimposed on the same diagram.

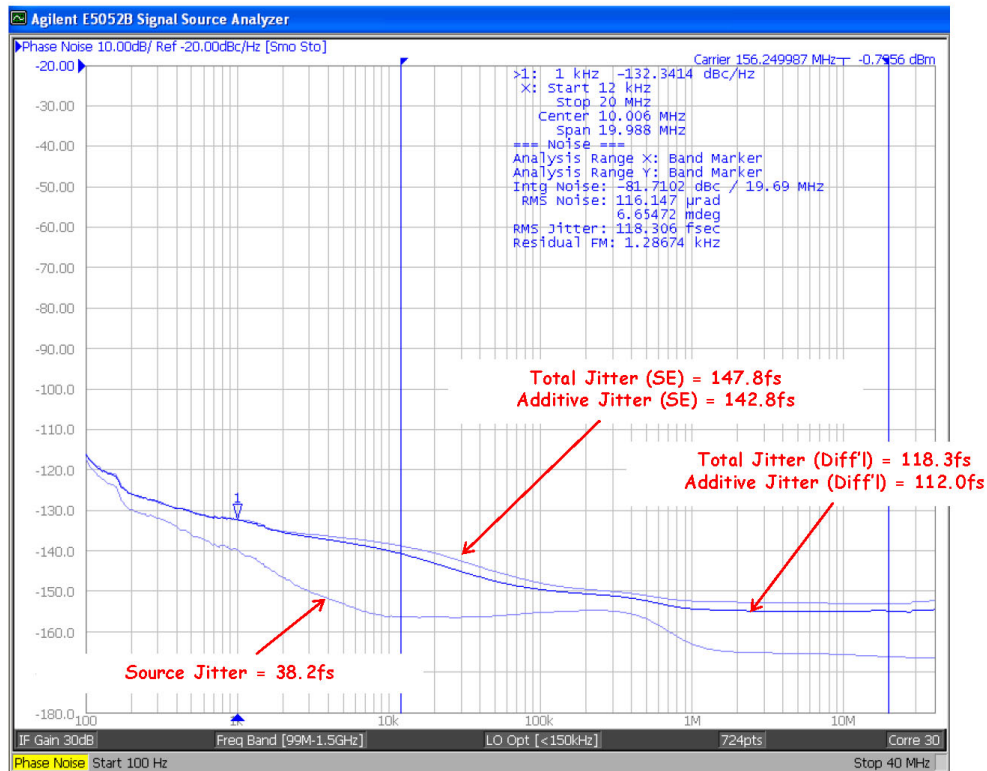
**Source Jitter:** Reference clock phase noise.

**Total Jitter (SE):** Combined source and clock buffer phase noise measured as a single-ended output to the phase noise analyzer and integrated from 12 kHz to 20 MHz.

**Total Jitter (Diff):** Combined source and clock buffer phase noise measured as a differential output to the phase noise analyzer and integrated from 12 kHz to 20 MHz. The differential measurement as shown in each figure is made using a balun. See Figure 1 on page 9.

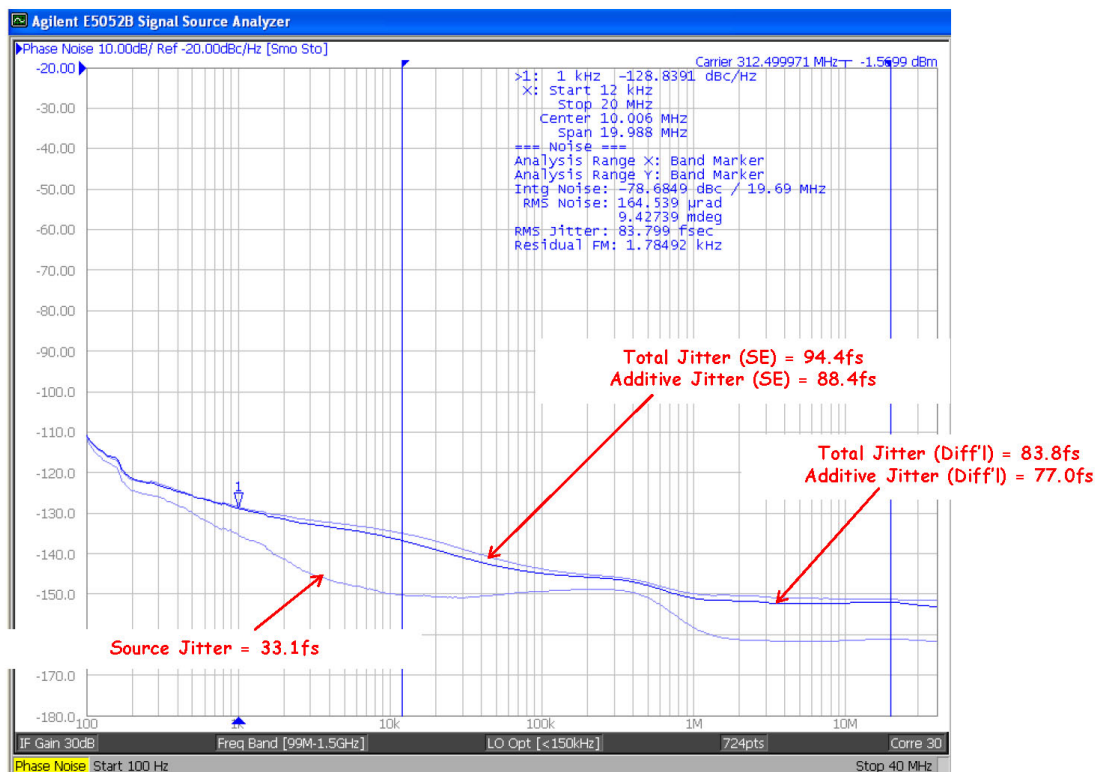
**Note:** To calculate the total RMS phase jitter when adding a buffer to your clock tree, use the root-sum-square (RSS).

The total jitter is a measure of the source plus the buffer's additive phase jitter. The additive jitter (rms) of the buffer can then be calculated (via root-sum-square addition).



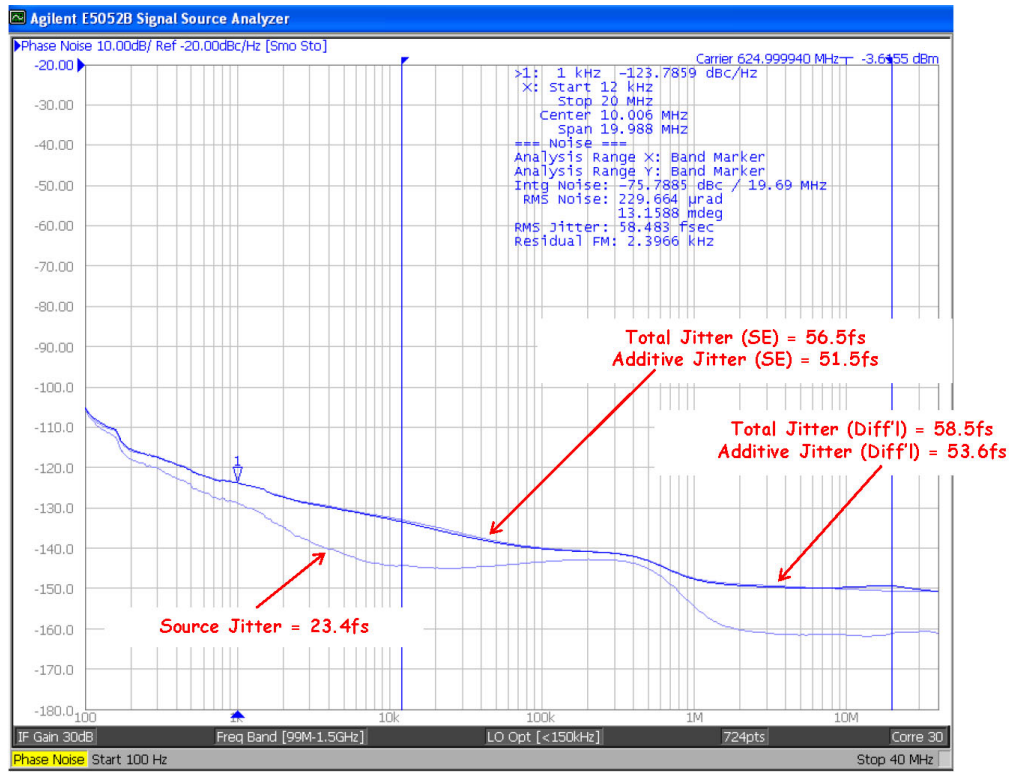
Frequency (MHz)	Diff'l Input Slew Rate (V/ns)	Source Jitter (fs)	Total Jitter (SE) (fs)	Additive Jitter (SE) (fs)	Total Jitter (Diff'l) (fs)	Additive Jitter (Diff'l) (fs)
156.25	1.0	38.2	147.8	142.8	118.3	112.0

Figure 12. Source Jitter (156.25 MHz)



Frequency (MHz)	Diff'l Input Slew Rate (V/ns)	Source Jitter (fs)	Total Jitter (SE) (fs)	Additive Jitter (SE) (fs)	Total Jitter (Diff'l) (fs)	Additive Jitter (Diff'l) (fs)
312.5	1.0	33.10	94.39	88.39	83.80	76.99

**Figure 13. Single-Ended Total Jitter (312.5 MHz)**



Frequency (MHz)	Diff'l Input Slew Rate (V/ns)	Source Jitter (fs)	Total Jitter (SE) (fs)	Additive Jitter (SE) (fs)	Total Jitter (Diff'l) (fs)	Additive Jitter (Diff'l) (fs)
625	1.0	23.4	56.5	51.5	58.5	53.6

Figure 14. Differential Total Jitter (625 MHz)

## 2.10. Input Mux Noise Isolation

The buffer's input clock mux is designed to minimize crosstalk between the CLK0 and CLK1. This improves phase jitter performance when clocks are present at both the CLK0 and CLK1 inputs. Figure 15 below is a measurement the input mux's noise isolation.

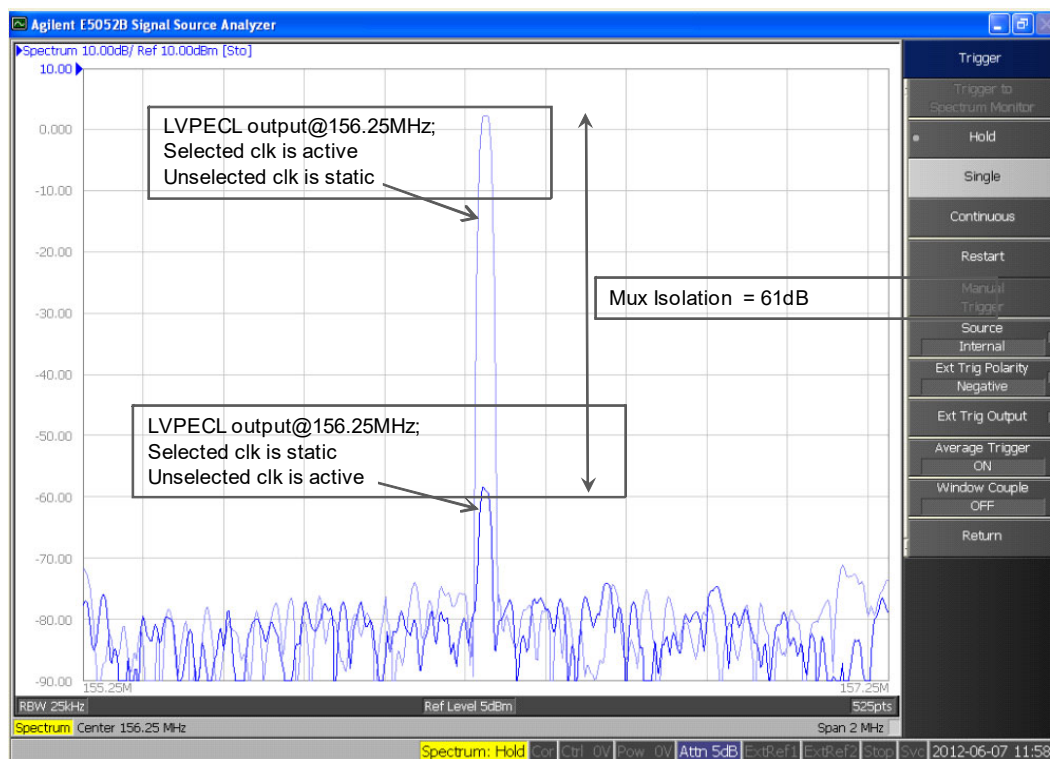
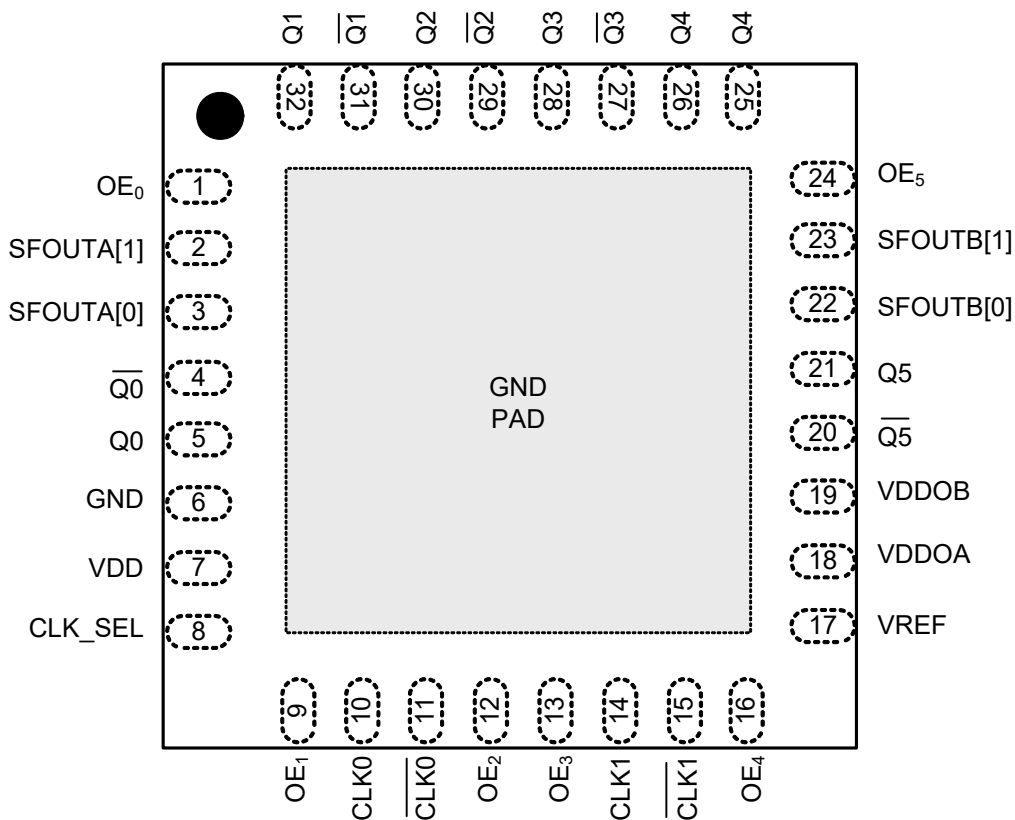


Figure 15. Input Mux Noise Isolation

## 2.11. Power Supply Noise Rejection

The device supports on-chip supply voltage regulation to reject noise present on the power supply, simplifying low jitter operation in real-world environments. This feature enables robust operation alongside FPGAs, ASICs and SoCs and may reduce board-level filtering requirements. For more information, see “AN491: Power Supply Rejection for Low Jitter Clocks”.

## 3. Pin Descriptions



**Table 20. Pin Description**

Pin	Name	Type*	Description
1	OE0	I	Output enable—Output 0 When OE = high, the Q0 is enabled. When OE = low, Q is held low and $\bar{Q}$ is held high for differential formats. For LVCMOS, both Q and $\bar{Q}$ are held low when OE is set low. This pin contains an internal pull-up resistor.
2	SFOUTA[1]	I	Output signal format control pin for Bank A Three level input control. Internally biased at $V_{DD}/2$ . Can be left floating or tied to ground or $V_{DD}$ .
3	SFOUTA[0]	I	Output signal format control pin for Bank A Three level input control. Internally biased at $V_{DD}/2$ . Can be left floating or tied to ground or $V_{DD}$ .
4	$\bar{Q}0$	O	Output clock 0 (complement)
5	Q0	O	Output clock 0
6	GND	O	Ground



Table 20. Pin Description (Continued)

Pin	Name	Type*	Description
7	V <sub>DD</sub>	P	Core voltage supply Bypass with 1.0 $\mu$ F capacitor and place as close to the V <sub>DD</sub> pin as possible.
8	CLK_SEL	I	Mux input select pin (LVCMOS) When CLK_SEL is high, CLK1 is selected. When CLK_SEL is low, CLK0 is selected. CLK_SEL contains an internal pull-down resistor.
9	OE1	I	Output enable—Output 1 When OE = high, the Q1 is enabled. When OE = low, Q is held low and $\bar{Q}$ is held high for differential formats. For LVCMOS, both Q and $\bar{Q}$ are held low when OE is set low. This pin contains an internal pull-up resistor.
10	CLK0	I	Input clock 0
11	$\overline{\text{CLK0}}$	I	Input clock 0 (complement) When the CLK0 is driven by a single-end input, connect $\overline{\text{CLK0}}$ to Vdd/2.
12	OE2	I	Output enable—Output 2 When OE = high, the Q2 is enabled. When OE = low, Q is held low and $\bar{Q}$ is held high for differential formats. For LVCMOS, both Q and $\bar{Q}$ are held low when OE is set low. OE2 contains an internal pull-up resistor.
13	OE3	I	Output enable—Output 3 When OE = high, the Q3 is enabled. When OE = low, Q is held low and $\bar{Q}$ is held high for differential formats. For LVCMOS, both Q and $\bar{Q}$ are held low when OE is set low. OE3 contains an internal pull-up resistor.
14	CLK1	I	Input clock 1
15	$\overline{\text{CLK1}}$	I	Input clock 1 (complement) When the CLK1 is driven by a single-end input, connect $\overline{\text{CLK1}}$ to Vdd/2.
16	OE4	I	Output enable—Output 4 When OE = high, the Q4 is enabled. When OE = low, Q is held low and $\bar{Q}$ is held high for differential formats. For LVCMOS, both Q and $\bar{Q}$ are held low when OE is set low. This pin contains an internal pull-up resistor.
17	V <sub>REF</sub>	O	Input clock reference voltage used to bias CLK0 or CLK1 clock input pins. V <sub>REF</sub> is required when a differential input clock is applied to the device and terminated as a single-ended reference. V <sub>REF</sub> may be left unconnected for LVCMOS or differential clock inputs. See “2.3. Input Clock Voltage Reference (VREF)” for details.
18	V <sub>DDOA</sub>	P	Output voltage supply—Bank A (Outputs: Q0 to Q2) Bypass with 1.0 $\mu$ F capacitor and place as close to the V <sub>DDOA</sub> pin as possible.

**Table 20. Pin Description (Continued)**

Pin	Name	Type*	Description
19	V <sub>DDOB</sub>	P	Output voltage supply—Bank B (Outputs: Q3 to Q5) Bypass with 1.0 $\mu$ F capacitor and place as close to the V <sub>DDOB</sub> pin as possible.
20	$\overline{Q5}$	O	Output clock 5 (complement)
21	Q5	O	Output clock 5
22	SFOUTB[0]	I	Output signal format control pin for Bank B Three level input control. Internally biased at V <sub>DD</sub> /2. Can be left floating or tied to ground or V <sub>DD</sub> .
23	SFOUTB[1]	I	Output signal format control pin for Bank B Three level input control. Internally biased at V <sub>DD</sub> /2. Can be left floating or tied to ground or V <sub>DD</sub> .
24	OE5	I	Output enable—Output 5 When OE = high, the Q5 is enabled. When OE = low, Q is held low and $\overline{Q}$ is held high for differential formats. For LVCMOS, both Q and $\overline{Q}$ are held low when OE is set low. This pin contains an internal pull-up resistor.
25	$\overline{Q4}$	O	Output clock 4 (complement)
26	Q4	O	Output clock 4
27	$\overline{Q3}$	O	Output clock 3 (complement)
28	Q3	O	Output clock 3
29	$\overline{Q2}$	O	Output clock 2 (complement)
30	Q2	O	Output clock 2
31	$\overline{Q1}$	O	Output clock 1 (complement)
32	Q1	O	Output clock 1
GND Pad	GND	GND	Ground Pad Power supply ground and thermal relief.

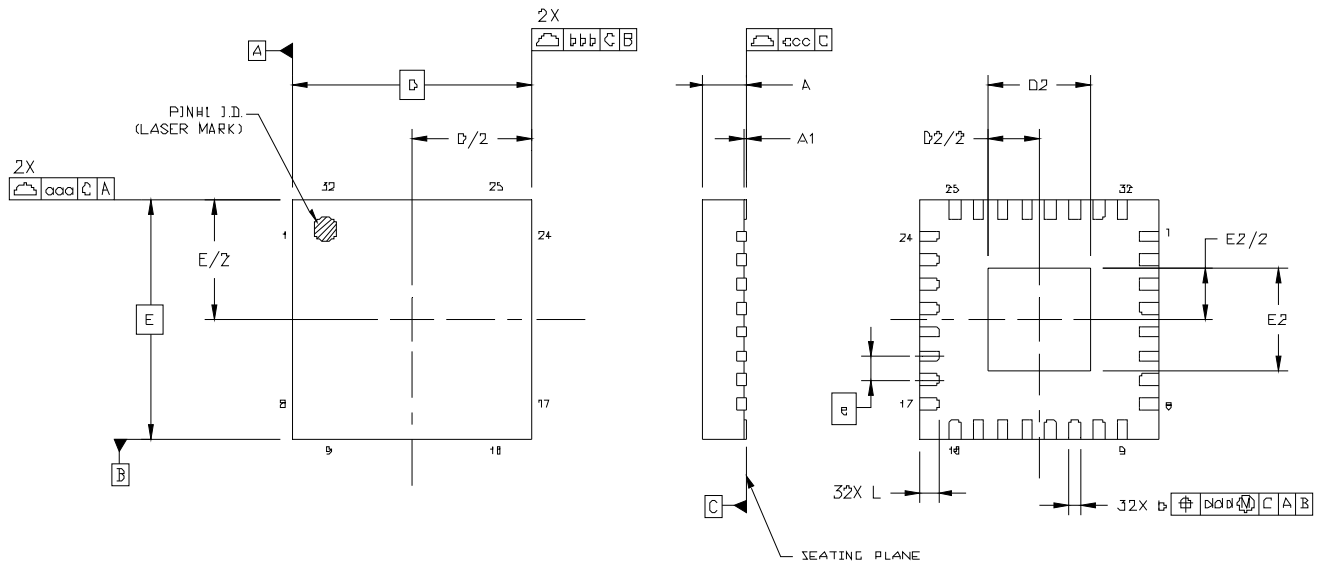
\*Pin types are: I = input, O = output, P = power, GND = ground.

## 4. Ordering Guide

<b>Part Number</b>	<b>Package</b>	<b>PB-Free, ROHS-6</b>	<b>Temperature</b>
Si53314-B-GM	32-QFN	Yes	-40 to 85 °C
Si53301/4-EVB	Evaluation Board	Yes	—

## 5. Package Outline

### 5.1. 5x5 mm 32-QFN Package Diagram



**Figure 16. Si53314 5x5 mm Package Diagram**

**Table 21. Package Dimensions**

Dimension	Min	Nom	Max
A	0.80	0.85	1.00
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c	0.20	0.25	0.30
D	5.00 BSC		
D2	2.00	2.15	2.30
e	0.50 BSC		
E	5.00 BSC		
E2	2.00	2.15	2.30
L	0.30	0.40	0.50
aaa	0.10		
bbb	0.10		
ccc	0.08		
ddd	0.10		
<b>Notes:</b>			
1. All dimensions shown are in millimeters (mm) unless otherwise noted.			
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.			
3. This drawing conforms to the JEDEC Solid State Outline MO-220.			

## 6. PCB Land Pattern

### 6.1. 5x5 mm 32-QFN Package Land Pattern

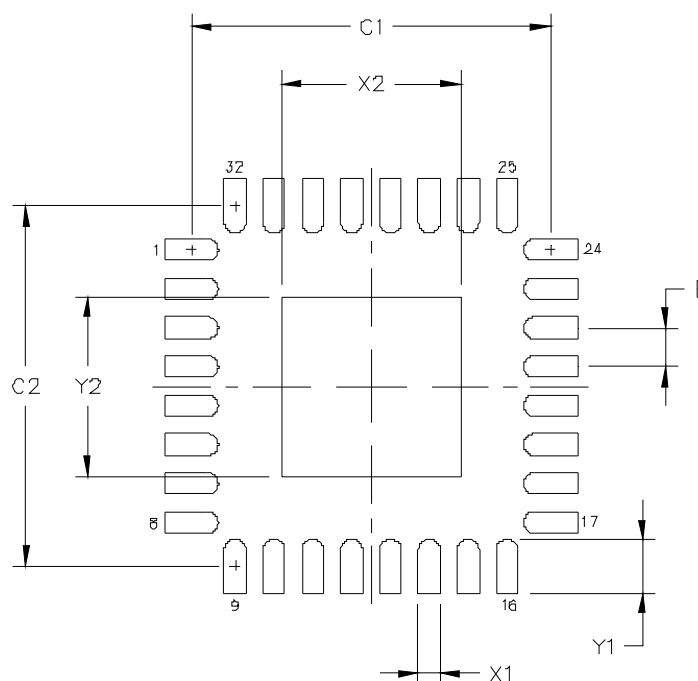


Figure 17. Si53314 5x5 mm Package Land Pattern

Table 22. PCB Land Pattern

Dimension	Min	Max	Dimension	Min	Max
C1	4.52	4.62	X2	2.20	2.30
C2	4.52	4.62	Y1	0.59	0.69
E	0.50 BSC		Y2	2.20	2.30
X1	0.20	0.30			

#### Notes:

##### General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

##### Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu\text{m}$  minimum, all the way around the pad.

##### Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 2x2 array of 0.75 mm square openings on 1.15 mm pitch should be used for the center ground pad.

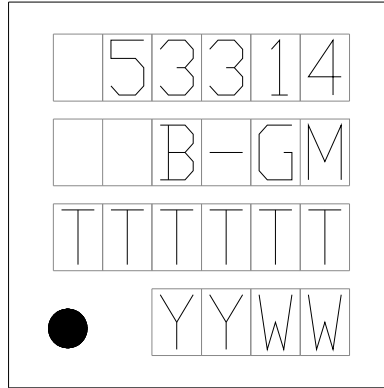
##### Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

# Si53314

## 7. Top Marking

### 7.1. Si53314 Top Marking



### 7.2. Top Marking Explanation

<b>Mark Method:</b>	Laser	
<b>Font Size:</b>	2.0 Point (28 mils) Center-Justified	
<b>Line 1 Marking:</b>	Device Part Number	<b>53314</b>
<b>Line 2 Marking:</b>	Device Revision/Type	<b>B-GM</b>
<b>Line 3 Marking:</b>	YY = Year WW = Work Week	Corresponds to the year and work week of the mold date.
	R = Die Rev F = Wafer Fab	First two characters of the Manufacturing Code.
<b>Line 4 Marking</b>	Circle = 0.5 mm Diameter Lower-Left Justified	Pin 1 Identifier
	A = Assembly Site I = Internal Code XX = Serial Lot Number	Last four characters of the Manufacturing Code.

## DOCUMENT CHANGE LIST

### Revision 0.4 to Revision 1.0

- Corrected front-page buffer block diagram.
- Improved performance specifications with greater detail.
- Added additional information to clarify the use of the voltage reference feature.
- Added pin type description to Table 20, “Pin Description,” on page 24.
- Added low-voltage termination options for 1.2 V and 1.5 V LVCMOS support.
- Clarified output clock bank A and bank B assignments.



# SKYWORKS®

## ClockBuilder Pro

Customize Skyworks clock generators, jitter attenuators and network synchronizers with a single tool. With CBPro you can control evaluation boards, access documentation, request a custom part number, export for in-system programming and more!

[www.skyworksinc.com/CBPro](http://www.skyworksinc.com/CBPro)



**Portfolio**

[www.skyworksinc.com/ia/timing](http://www.skyworksinc.com/ia/timing)



**SW/HW**

[www.skyworksinc.com/CBPro](http://www.skyworksinc.com/CBPro)



**Quality**

[www.skyworksinc.com/quality](http://www.skyworksinc.com/quality)



**Support & Resources**

[www.skyworksinc.com/support](http://www.skyworksinc.com/support)

### Copyright © 2021 Skyworks Solutions, Inc. All Rights Reserved.

Information in this document is provided in connection with Skyworks Solutions, Inc. ("Skyworks") products or services. These materials, including the information contained herein, are provided by Skyworks as a service to its customers and may be used for informational purposes only by the customer. Skyworks assumes no responsibility for errors or omissions in these materials or the information contained herein. Skyworks may change its documentation, products, services, specifications or product descriptions at any time, without notice. Skyworks makes no commitment to update the materials or information and shall have no responsibility whatsoever for conflicts, incompatibilities, or other difficulties arising from any future changes.

No license, whether express, implied, by estoppel or otherwise, is granted to any intellectual property rights by this document. Skyworks assumes no liability for any materials, products or information provided hereunder, including the sale, distribution, reproduction or use of Skyworks products, information or materials, except as may be provided in Skyworks' Terms and Conditions of Sale.

THE MATERIALS, PRODUCTS AND INFORMATION ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND, WHETHER EXPRESS, IMPLIED, STATUTORY, OR OTHERWISE, INCLUDING FITNESS FOR A PARTICULAR PURPOSE OR USE, MERCHANTABILITY, PERFORMANCE, QUALITY OR NON-INFRINGEMENT OF ANY INTELLECTUAL PROPERTY RIGHT; ALL SUCH WARRANTIES ARE HEREBY EXPRESSLY DISCLAIMED. SKYWORKS DOES NOT WARRANT THE ACCURACY OR COMPLETENESS OF THE INFORMATION, TEXT, GRAPHICS OR OTHER ITEMS CONTAINED WITHIN THESE MATERIALS. SKYWORKS SHALL NOT BE LIABLE FOR ANY DAMAGES, INCLUDING BUT NOT LIMITED TO ANY SPECIAL, INDIRECT, INCIDENTAL, STATUTORY, OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION, LOST REVENUES OR LOST PROFITS THAT MAY RESULT FROM THE USE OF THE MATERIALS OR INFORMATION, WHETHER OR NOT THE RECIPIENT OF MATERIALS HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

Skyworks products are not intended for use in medical, lifesaving or life-sustaining applications, or other equipment in which the failure of the Skyworks products could lead to personal injury, death, physical or environmental damage. Skyworks customers using or selling Skyworks products for use in such applications do so at their own risk and agree to fully indemnify Skyworks for any damages resulting from such improper use or sale.

Customers are responsible for their products and applications using Skyworks products, which may deviate from published specifications as a result of design defects, errors, or operation of products outside of published parameters or design specifications. Customers should include design and operating safeguards to minimize these and other risks. Skyworks assumes no liability for applications assistance, customer product design, or damage to any equipment resulting from the use of Skyworks products outside of Skyworks' published specifications or parameters.

Skyworks, the Skyworks symbol, Sky5®, SkyOne®, SkyBlue™, Skyworks Green™, Clockbuilder®, DSPLL®, ISOModem®, ProSLIC®, and SiPHY® are trademarks or registered trademarks of Skyworks Solutions, Inc. or its subsidiaries in the United States and other countries. Third-party brands and names are for identification purposes only and are the property of their respective owners. Additional information, including relevant terms and conditions, posted at [www.skyworksinc.com](http://www.skyworksinc.com), are incorporated by reference.

Skyworks Solutions, Inc. | Nasdaq: SWKS | [sales@skyworksinc.com](mailto:sales@skyworksinc.com) | [www.skyworksinc.com](http://www.skyworksinc.com)

USA: 781-376-3000 | Asia: 886-2-2735 0399 | Europe: 33 (0)1 43548540 |    