PCK946

Low voltage 1 : 10 CMOS clock driver

Rev. 01 — 13 December 2005 Product data sheet

1. General description

The PCK946 is a low voltage CMOS 1 : 10 clock buffer. The 10 outputs can be configured into a standard fan-out buffer or into 1× and ½× combinations. The ten outputs were designed and optimized to drive 50 Ω series or parallel terminated transmission lines. With output-to-output skews of 350 ps, the PCK946 is ideal as a clock distribution chip for synchronous systems which need a tight level of skew from a large number of outputs.

With an output impedance of approximately 7 Ω, in both the HIGH and LOW logic states, the output buffers of the PCK946 are ideal for driving series terminated transmission lines. More specifically, each of the 10 PCK946 outputs can drive two series terminated transmission lines. With this capability, the PCK946 has an effective fan-out of 1 : 20 in applications using point-to-point distribution schemes.

The PCK946 has the capability of generating 1× and ½× signals from a 1× source. The design is fully static; the signals are generated and re-timed inside the chip to ensure minimal skew between the 1× and ½× signals. The device features selectability to allow the user to select the ratio of 1× outputs to ½× outputs.

Two independent LVCMOS/LVTTL compatible clock inputs are available. Designers can take advantage of this feature to provide redundant clock sources or the addition of a test clock into the system design. With the TCLK_SEL input pulled HIGH, the TCLK1 input is selected.

All of the control inputs are LVCMOS/LVTTL compatible. The DSELn pins choose between 1× and ½× outputs. A LOW on the DSELn pins will select the 1× output. The MR/$\overline{OE}$ input will reset the internal flip-flops and 3-state the outputs when it is forced HIGH.

The PCK946 is fully 3.3 V compatible. The 32-lead LQFP package was chosen to optimize performance, board space, and cost of the device. The 32-lead LQFP package has a 7 mm × 7 mm body size with a conservative 0.8 mm pin spacing.

2. Features

- 2 selectable LVCMOS/LVTTL clock inputs
- 350 ps output-to-output skew
- Drives up to 20 series terminated independent clock lines
- Maximum input/output frequency of 150 MHz
- 3-stateable outputs
- 32-lead LQFP packaging
- 3.3 V V_{CC} supply voltage

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3. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
PCK946BD	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1

4. Functional diagram

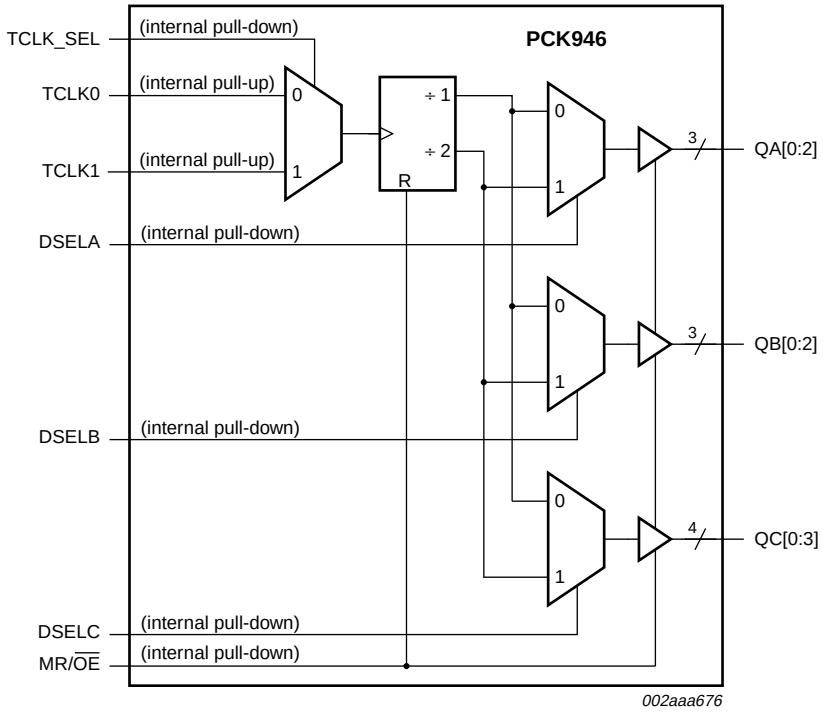


Fig 1. Functional diagram of PCK946

5. Pinning information

5.1 Pinning

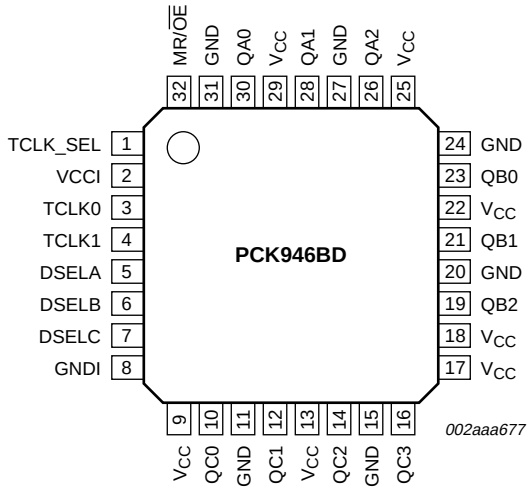


Fig 2. Pin configuration for LQFP32

5.2 Pin description

Table 2: Pin description

Symbol	Pin	Description
DSELA, DSELB, DSELC	5, 6, 7	output bank divide select input
GND	11, 15, 20, 24, 27, 31	ground
GNDI	8	ground
MR/$\overline{OE}$	32	internal reset and output (high-impedance) control
QA0, QA1, QA2	30, 28, 26	bank A outputs
QB0, QB1, QB2	23, 21, 19	bank B outputs
QC0, QC1, QC2, QC3	10, 12, 14, 16	bank C outputs
TCLK_SEL	1	CMOS clock select input
TCLK0, TCLK1	3, 4	CMOS clock inputs
V_{CC}	9, 13, 17, 18, 22, 25, 29	supply voltage
VCCI	2	supply voltage

6. Functional description

6.1 Function table

Table 3: TCLK_SEL function table

TCLK_SEL	Input
0	TCLK0
1	TCLK1

Table 4: DSELn function table

DSELn	Outputs
0	1×
1	½×

Table 5: MR/$\overline{OE}$ function table

MR/$\overline{OE}$	Outputs
0	enabled
1	high-impedance

7. Limiting values

Table 6: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.3	+4.6	V
V_I	input voltage		–0.3	V_{CC} + 0.3	V
I_I	input current	CMOS inputs	-	±20	mA
T_{stg}	storage temperature		–40	+125	°C

8. Static characteristics

Table 7: Static characteristics

T_{amb} = 0 °C to +70 °C; V_{CC} = 3.3 V ± 0.3 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	HIGH-state input voltage			2.0	-	3.6	V
V_{IL}	LOW-state input voltage			-	-	0.8	V
V_{OH}	HIGH-state output voltage	I_{OH} = –20 mA	[1]	2.5	-	-	V
V_{OL}	LOW-state output voltage	I_{OL} = 20 mA	[1]	-	-	0.4	V
I_I	input current		[2]	-	-	±120	µA
C_i	input capacitance			-	-	4	pF
C_{PD}	power dissipation capacitance	per output		-	25	-	pF
$I_{q(max)}$	maximum quiescent supply current			-	1	2	mA

[1] The PCK946 can drive 50 Ω transmission lines on the incident edge. Each output can drive one 50 Ω parallel terminated transmission line to the termination voltage of $V_T = 0.5V_{CC}$. Alternately, the device drives up to two 50 Ω series terminated transmission lines.

[2] I_I current is a result of internal pull-up/pull-down resistors.

9. Dynamic characteristics

Table 8: Dynamic characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{max}	maximum input clock frequency		[1]	150	-	-	MHz
t_{PLH}	LOW-to-HIGH propagation delay	TCLK to Qn	[1] [2]	4.5	7.5	11.5	ns
t_{PHL}	HIGH-to-LOW propagation delay	TCLK to Qn	[1] [2]	4.5	7.5	11.5	ns
$t_{sk(o)}$	output skew time	output-to-output	[1] [2]				
		f_{max} < 100 MHz; same frequency outputs		-	-	350	ps
		f_{max} < 100 MHz; different frequency outputs		-	-	350	ps
		f_{max} > 100 MHz; same frequency outputs		-	-	350	ps
		f_{max} > 100 MHz; different frequency outputs		-	-	450	ps
$t_{sk(pr)}$	process skew time	part-to-part	[3]	-	2.0	4.5	ns
t_{PZL}	OFF-state to LOW propagation delay		[2]	-	3	11	ns
t_{PZH}	OFF-state to HIGH propagation delay		[2]	-	3	11	ns
t_{PLZ}	LOW to OFF-state propagation delay		[2]	-	3	11	ns
t_{PHZ}	HIGH to OFF-state propagation delay		[2]	-	3	11	ns
t_r	rise time	output; 0.8 V to 2.0 V	[2]	0.1	0.5	1.0	ns
t_f	fall time	output; 2.0 V to 0.8 V	[2]	0.1	0.5	1.0	ns

[1] Driving 50 Ω transmission lines.

[2] Termination is 50 Ω to $0.5V_{CC}$.

[3] Part-to-part skew at a given temperature and voltage.

10. Application information

10.1 Driving transmission lines

The PCK946 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10 Ω the drivers can drive either parallel or series terminated transmission lines.

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $0.5V_{CC}$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the PCK946 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3, illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fan-out of the PCK946 clock driver is effectively doubled due to its capability to drive multiple lines.

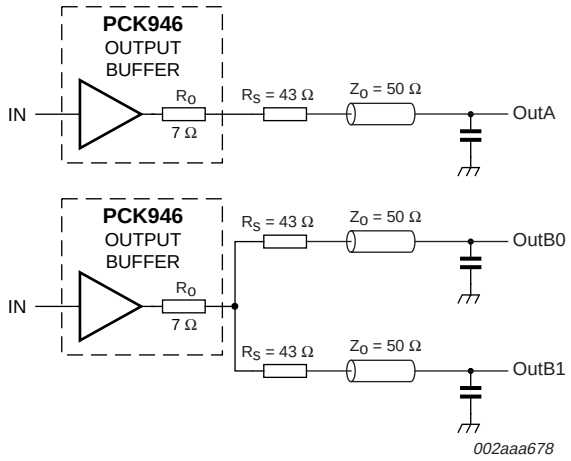


Fig 3. Single versus dual transmission lines

The waveform plots of Figure 4 show simulation results of an output driving a single line versus two lines. In both cases the drive capability of the PCK946 output buffers is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the PCK946. The output waveform in Figure 4 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 43 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S\left(\frac{Z_o}{R_s + R_o + Z_o}\right) = 3.0\left(\frac{25}{53.5}\right) = 1.40\ V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.8 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

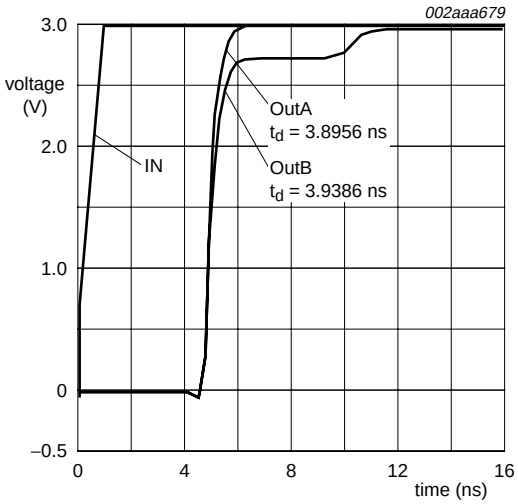
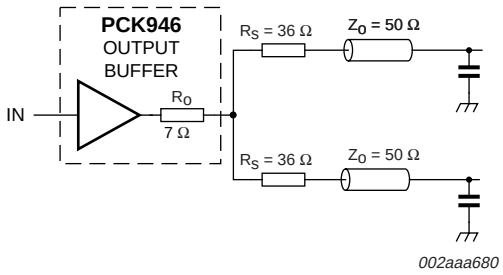


Fig 4. Single versus dual waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



7 Ω + 36 Ω || 36 Ω = 50 Ω || 50 Ω

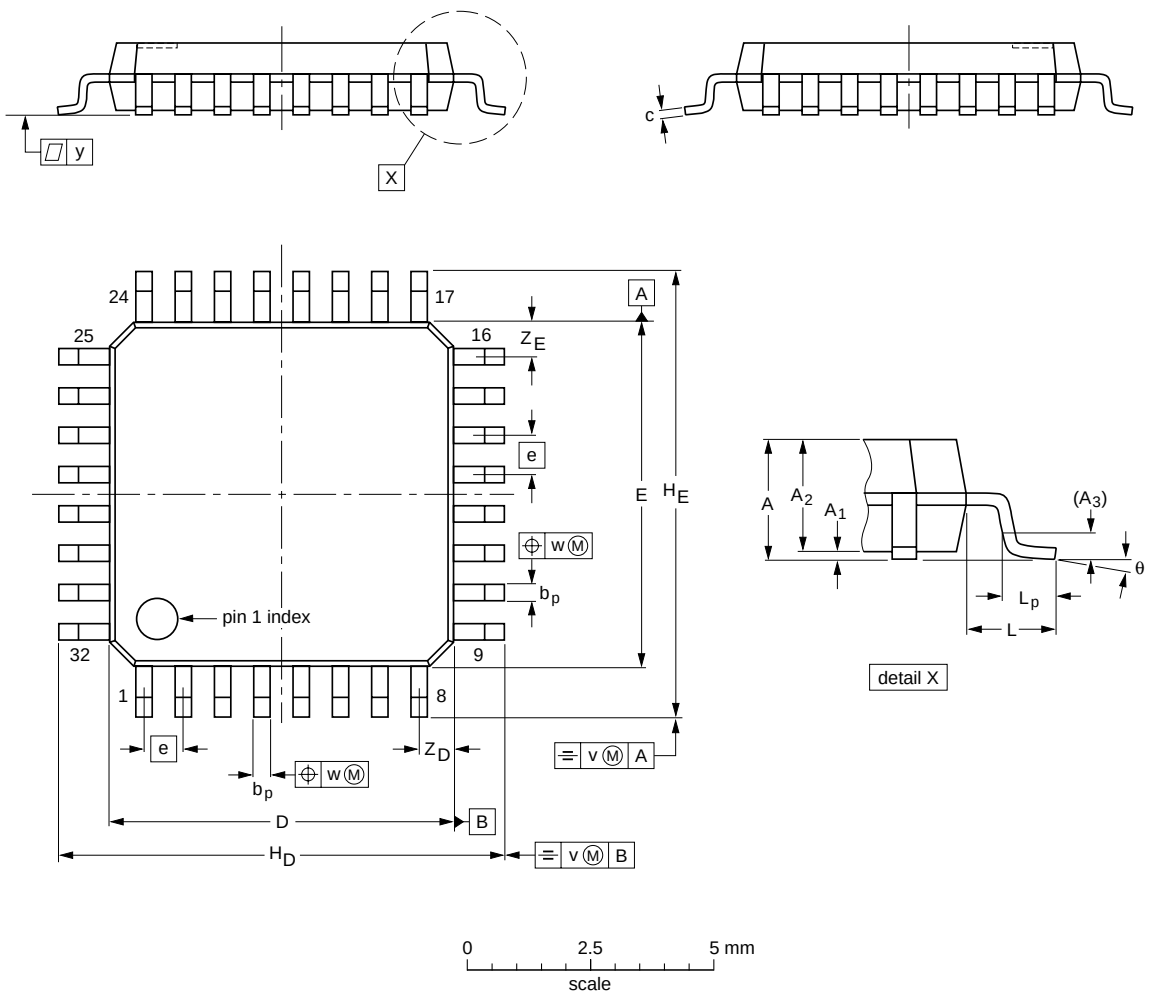
25 Ω = 25 Ω

Fig 5. Optimized dual line termination

SPICE level output buffer models are available for engineers who want to simulate their specific interconnect schemes. In addition IV characteristics are in the process of being generated to support the other board level simulators in general use.

11. Package outline

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm **SOT358-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1	0.75 0.45	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT358 -1	136E03	MS-026				~~03-02-25~~ 05-11-09

Fig 6. Package outline SOT358-1 (LQFP32)

12. Soldering

12.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

12.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

12.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

12.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

12.5 Package related soldering information

Table 9: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

13. Abbreviations

Table 10: Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Silicon
LVCMOS	Low Voltage Complementary Metal Oxide Silicon
LVTTL	Low Voltage Transistor-Transistor Logic

14. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PCK946_1	20051213	Product data sheet	-	9397 750 12296	-

15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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20. Contents

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