

1.1 Scope.

This specification covers the requirements for 12-bit, high speed digital-to-analog converters (DACs). The AD9712B/883B is a 12-bit ECL-compatible DAC which features update rates of 100 Msps minimum; the TTL-compatible AD9713B/883B will update at 80 Msps minimum.

1.2 Part Number.

| Device | Part Number | Device | Part Number |
|--------|------------------|--------|------------------|
| -1 | AD9712BS(X)/883B | -3 | AD9713BS(X)/883B |
| -2 | AD9712BT(X)/883B | -4 | AD9713BT(X)/883B |

SMD Number 5962-90911 in development.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

| (X) | Package | Description |
|-----|---------|------------------------------|
| Q | Q-28 | 28-Pin Ceramic DIP |
| E | E-28A | 28-Pin Leadless Chip Carrier |

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

| | |
|-----------------------------------------------------------|-------------------|
| Positive Supply Voltage ($+V_S$) | +6 V |
| Positive Supply Voltage ($-V_S$) | -7 V |
| Analog-to-Digital Ground Voltage Differential | 0.5 V |
| Digital Input Voltages (D_1 - D_{12} , LATCH ENABLE) | |
| AD9712B | 0 V to $-V_S$ |
| AD9713B | -0.5 V to $+V_S$ |
| Internal Reference Output Current | 500 μA |
| Control Amplifier Input Voltage Range | 0 V to -4.0 V |
| Control Amplifier Output Current | ± 2.5 mA |
| Reference Input Voltage (V_{REF}) | -3.7 V to $-V_S$ |
| Analog Output Current | 30 mA |
| Operating Temperature Range (Case) | |
| AD9712B/AD9713BSE/SQ/TE/TQ | -55°C to +125°C |
| Junction Temperature | +175°C |
| Storage Temperature Range (Case) | -65°C to +150°C |
| Lead Soldering Temperature (10 sec) | +300°C |

1.5 Thermal Characteristics.

Maximum junction temperature should not be allowed to exceed +175°C. Typical thermal impedances with parts soldered in place; no air flow:

- 28-pin ceramic DIP: $\theta_{JA} = 32^\circ\text{C}/\text{W}$, $\theta_{JC} = 10^\circ\text{C}/\text{W}$;
- 28-pin LCC: $\theta_{JA} = 41^\circ\text{C}/\text{W}$, $\theta_{JC} = 13^\circ\text{C}/\text{W}$.

AD9712B/AD9713B—SPECIFICATIONS

Table I.

| Test | Symbol | Device | Design Limits ¹ | Sub Group 1 | Sub Group 2, 3 | Sub Group 4 | Sub Group 5, 6 | Sub Group 9 | Test Conditions ² | Units |
|-------------------------------------------|------------------|------------------|----------------------------|-------------|----------------|----------------|----------------|-------------|------------------------------|-----------|
| Differential Nonlinearity | DNL | -1, -3 -2, -4 | | | | ±1.5 ±1.0 | ±2.0 ±1.5 | | | LSB |
| Integral Nonlinearity | INL | -1, -3 -2, -4 | | | | ±1.75 ±1.25 | ±2.0 ±1.75 | | | LSB |
| Zero-Scale Offset Error | I _{OS} | All | | 2.5 | 5.0 | | | | | μA max |
| Full-Scale Gain Error | | All | | 5 | 8.0 | | | | | % max |
| Internal Reference Voltage | V _{IR} | All | | -1.11 | -1.09 | | | | | V min |
| | | | | -1.25 | -1.27 | | | | | V max |
| Internal Reference Output Current | I _{IR} | All | -50 | | | | | | | μA min |
| | | | +500 | | | | | | | μA max |
| Output Compliance Range | V _{OC} | All | -1.2 | | | | | @ +25°C | | V min |
| | | | +2 | | | | | @ +25°C | | V max |
| Output Resistance | R _O | All | 2.0 | | | | | @ +25°C | | kΩ min |
| | | | 3.0 | | | | | @ +25°C | | kΩ max |
| Output Update Rate ³ | | -1, -2 -3, -4 | 100 80 | | | | | @ +25°C | | Msp/s min |
| Digital Logic "1" Input Voltage | V _{IH} | -1, -2 -3, -4 | | -1.0 2.0 | -1.0 2.0 | | | | | V min |
| Digital Logic "0" Input Voltage | V _{IL} | -1, -2 -3, -4 | | -1.5 0.8 | -1.5 0.8 | | | | | V max |
| Digital Logic "1" Input Current | I _{IH} | All | | 20 | 20 | | | | | μA max |
| Digital Logic "0" Input Current | V _{IL} | -1, -2 -3, -4 | | 10 600 | 10 600 | | | | | μA max |
| Input Setup Time ⁴ | t _S | All | -0.8 | | | | | | | ns min |
| Input Hold Time ⁵ | t _H | All | 2.0 | | | | | | | ns min |
| Latch Pulse Width (LOW) (transparent) | t _{LPW} | All | 2.8 | | | | | | | ns min |
| +V _S Supply Current | +I _S | -3, -4 | | 12 | 14 | | | | | mA max |
| -V _S Supply Current | -I _S | -1, -2 -3, -4 | | 178 184 | 183 188 | | | | | mA max |
| Power Supply Rejection Ratio ⁶ | PSRR | All | | | | 125 | | @ +25°C | | μA/V max |

NOTES

¹Value shown is over full temperature range unless otherwise noted in Test Condition. Number in this column indicates specification is guaranteed but not tested.

²+V_S = +5 V; -V_S = -5.2 V; reference voltage = -1.2 V; R_{SET} = 7.5 kΩ; V_{OUT} = 0 V (virtual ground), unless otherwise indicated.

³Data registered into DAC accurately at this rate; does not imply settling to 12-bit accuracy.

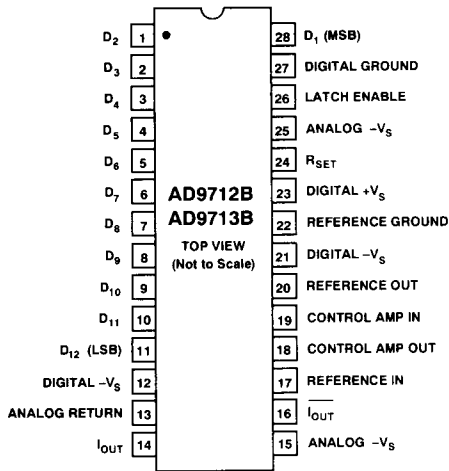
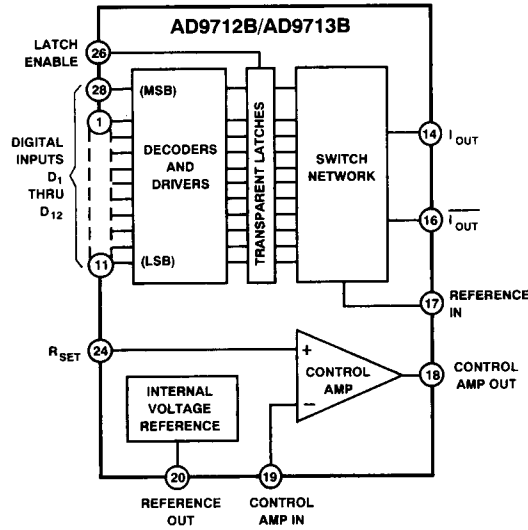
⁴Data must remain stable for specified time prior to falling edge of LATCH ENABLE signal.

⁵Data must remain stable for specified time after rising edge of LATCH ENABLE signal.

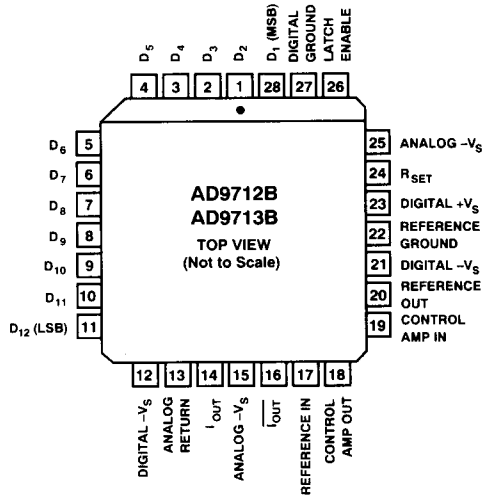
⁶Measured at ±5% of +V_S (AD9713B only) and -V_S (AD9712B or AD9713B) using external reference.

Specifications subject to change without notice.

3.2.1 Functional Block Diagram and Terminal Assignments.



DIP Pinout Designations



Ceramic LCC Pinout Designations

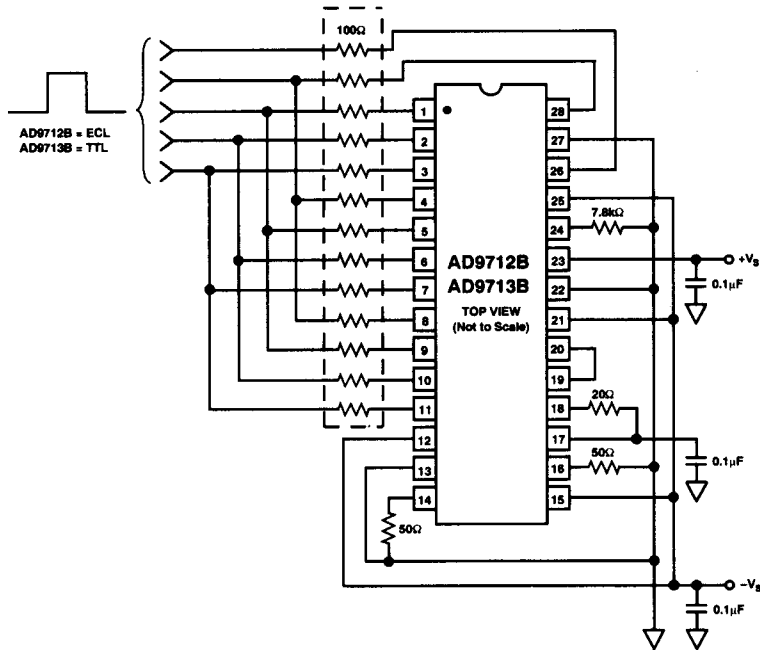
AD9712B/AD9713B

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (D-56).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015, Test Condition (B).



DIP Burn-In Diagram