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**REVISION HISTORY**

2/12—Revision 0: Initial Version

## SPECIFICATIONS

$V_{DD} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $I_{OUT} = \text{virtual GND}$ ,  $GND = 0\text{ V}$ ,  $V_{REF} = 10\text{ V}$ ,  $T_A = \text{full operating temperature range}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Condition	5 V $\pm$ 10%	Unit
<b>STATIC PERFORMANCE<sup>1</sup></b>				
Resolution	N	1 LSB = $V_{REF}/2^{16} = 153\ \mu\text{V}$ when $V_{REF} = 10\text{ V}$	16	Bits
Relative Accuracy	INL		$\pm 3$	LSB max
Differential Nonlinearity	DNL	Monotonic	-1/+2	LSB max
Output Leakage Current	$I_{OUT}$	Data = 0x0000, $T_A = 25^\circ\text{C}$	10	nA max
		Data = 0x0000, $T_A = T_A \text{ maximum}$	20	nA max
Full-Scale Gain Error	$G_{FSE}$	Data = 0xFFFF	$\pm 1/\pm 4$	mV typ/max
Full-Scale Temperature Coefficient <sup>2</sup>	$TCV_{FS}$		1	ppm/ $^\circ\text{C}$ typ
<b>REFERENCE INPUT</b>				
$V_{REF}$ Range	$V_{REF}$		-15/+15	V min/max
Input Resistance	$R_{REF}$		5	k $\Omega$ typ <sup>3</sup>
Input Capacitance <sup>2</sup>	$C_{REF}$		5	pF typ
<b>ANALOG OUTPUT</b>				
Output Current	$I_{OUT}$	Data = 0xFFFF	2	mA typ
Output Capacitance <sup>2</sup>	$C_{OUT}$	Code dependent	200	pF typ
<b>LOGIC INPUTS AND OUTPUT</b>				
Logic Input Low Voltage	$V_{IL}$		0.8	V max
Logic Input High Voltage	$V_{IH}$		2.4	V min
Input Leakage Current	$I_{IL}$		10	$\mu\text{A}$ max
Input Capacitance <sup>2</sup>	$C_{IL}$		10	pF max
<b>INTERFACE TIMING<sup>2, 4</sup></b>				
Clock Input Frequency	$f_{CLK}$		50	MHz
Clock Width High	$t_{CH}$		10	ns min
Clock Width Low	$t_{CL}$		10	ns min
$\overline{CS}$ to Clock Setup	$t_{CSS}$		0	ns min
Clock to $\overline{CS}$ Hold	$t_{CSH}$		10	ns min
Data Setup	$t_{DS}$		5	ns min
Data Hold	$t_{DH}$		10	ns min
<b>SUPPLY CHARACTERISTICS</b>				
Power Supply Range	$V_{DD \text{ RANGE}}$		4.5/5.5	V min/max
Positive Supply Current	$I_{DD}$	Logic inputs = 0 V	10	$\mu\text{A}$ max
Power Dissipation	$P_{DISS}$	Logic inputs = 0 V	0.055	mW max
Power Supply Sensitivity	$P_{SS}$	$\Delta V_{DD} = \pm 5\%$	0.006	%/% max
<b>AC CHARACTERISTICS<sup>4</sup></b>				
Output Voltage Settling Time	$t_S$	To $\pm 0.1\%$ of full scale, Data = 0x0000 to 0xFFFF to 0x0000	0.5	$\mu\text{s}$ typ
Reference Multiplying Bandwidth	BW	$V_{REF} = 100\text{ mV rms}$ , data = 0xFFFF	6.6	MHz typ
DAC Glitch Impulse	Q	$V_{REF} = 0\text{ V}$ , data = 0x7FFF to 0x8000	7	nV-sec
Feedthrough Error	$V_{OUT}/V_{REF}$	Data = 0x0000, $V_{REF} = 100\text{ mV rms}$ , same channel	-83	dB
Digital Feedthrough	Q	$C_S = 1$ and $f_{CLK} = 1\text{ MHz}$	7	nV-sec
Total Harmonic Distortion	THD	$V_{REF} = 5\text{ V p-p}$ , data = 0xFFFF, $f = 1\text{ kHz}$	-103	dB typ
Output Spot Noise Voltage	$e_N$	$f = 1\text{ kHz}$ , BW = 1 Hz	12	nV/ $\sqrt{\text{Hz}}$

<sup>1</sup> All static performance tests (except  $I_{OUT}$ ) are performed in a closed-loop system using an external precision OP177 I-to-V converter amplifier. The  $R_{FB}$  terminal is tied to the amplifier output. The +IN op amp is grounded, and the DAC  $I_{OUT}$  is tied to the -IN op amp. Typical values represent average readings measured at  $25^\circ\text{C}$ .

<sup>2</sup> These parameters are guaranteed by design and are not subject to production testing.

<sup>3</sup> All ac characteristic tests are performed in a closed-loop system using an AD8038 I-to-V converter amplifier except for THD where an AD8065 was used.

<sup>4</sup> All input control signals are specified with  $t_R = t_F = 2.5\text{ ns}$  (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

TIMING DIAGRAM

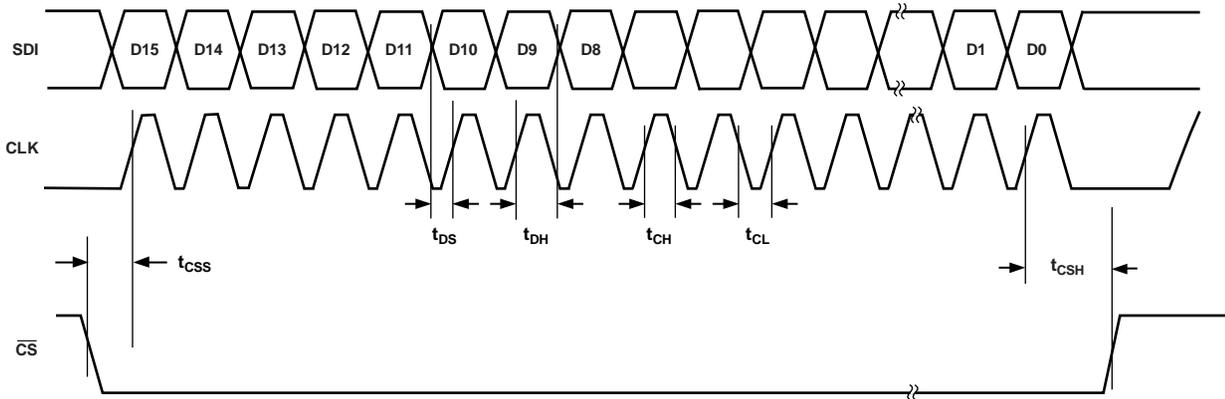


Figure 2. Timing Diagram

10082-016

## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
$V_{DD}$ to GND	-0.3 V to +8 V
$V_{REF}$ to GND	-18 V to +18 V
Logic Inputs to GND	-0.3 V to +8 V
$V(I_{OUT})$ to GND	-0.3 V to $V_{DD} + 0.3$ V
Input Current to Any Pin Except Supplies	$\pm 50$ mA
Package Power Dissipation	$(T_{J_{Max}} - T_A)/\theta_{JA}$
Thermal Resistance, $\theta_{JA}$	
8-Lead Surface Mount (MSOP)	150°C/W
Maximum Junction Temperature ( $T_{J_{Max}}$ )	150°C
Operating Temperature Range	
Enhanced Plastic (EP Version)	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature	
RM-8 (Vapor Phase, 60 sec)	215°C
RM-8 (Infrared, 15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CLK	Clock Input. Positive-edge triggered, clocks data into shift register.
2	SDI	Serial Register Input. Data loads directly into the shift register MSB first. Extra leading bits are ignored.
3	R <sub>FB</sub>	Internal Matching Feedback Resistor. This pin connects to an external op amp for voltage output.
4	V <sub>REF</sub>	DAC Reference Input Pin. Establishes DAC full-scale voltage. Constant input resistance vs. code.
5	I <sub>OUT</sub>	DAC Current Output. This pin connects to the inverting terminal of the external precision I-to-V op amp for voltage output.
6	GND	Analog and Digital Ground.
7	V <sub>DD</sub>	Positive Power Supply Input. Specified range of operation at 5 V ± 10%.
8	$\overline{CS}$	Chip Select. Active low digital input. Transfers shift-register data to DAC register on rising edge.

### TYPICAL PERFORMANCE CHARACTERISTICS

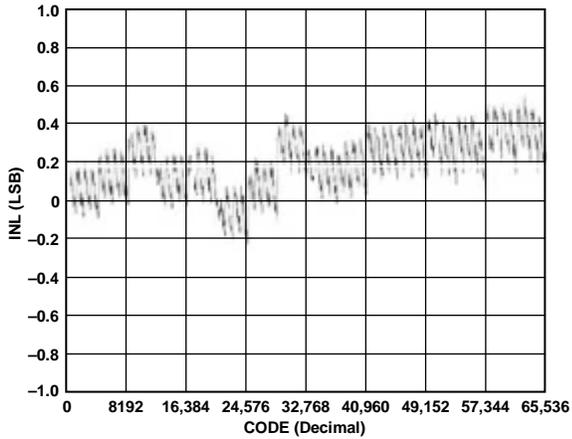


Figure 4. Integral Nonlinearity Error

10082-005

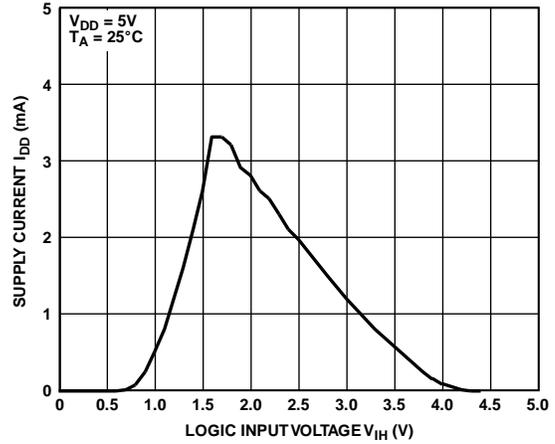


Figure 7. Supply Current,  $I_{DD}$  vs. Logic Input Voltage,  $V_{IH}$

10082-010

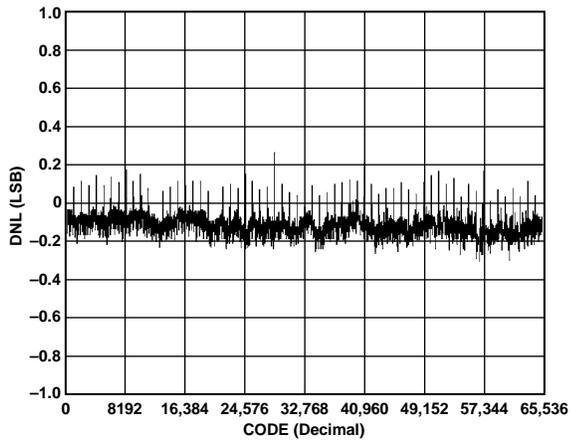


Figure 5. Differential Nonlinearity Error

10082-006

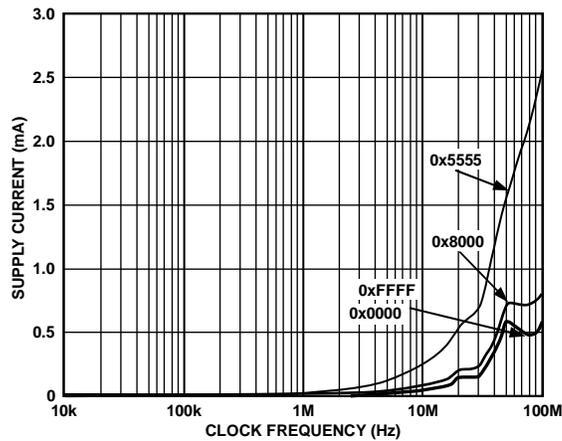


Figure 8. Supply Current vs. Clock Frequency

10082-011

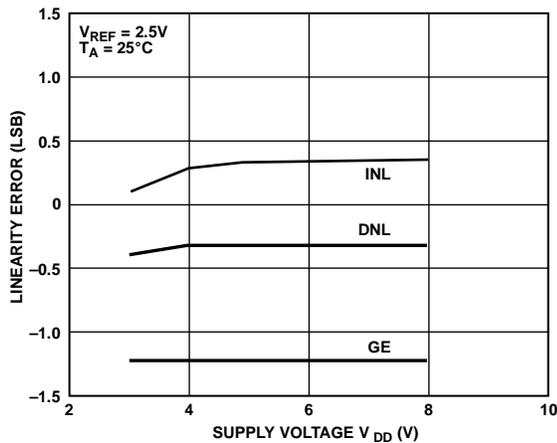


Figure 6. Linearity Error vs. Supply Voltage,  $V_{DD}$

10082-009

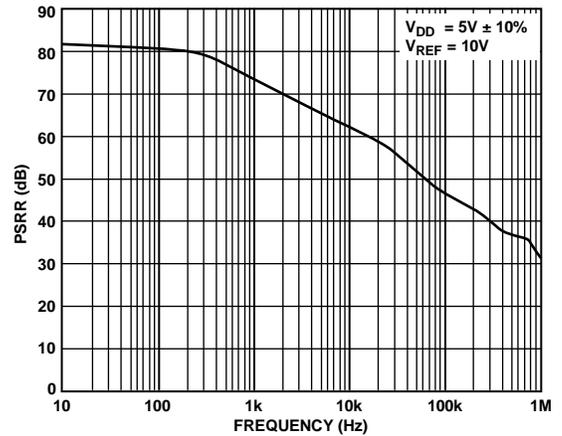


Figure 9. Power Supply Rejection Ratio (PSRR) vs. Frequency

10082-012

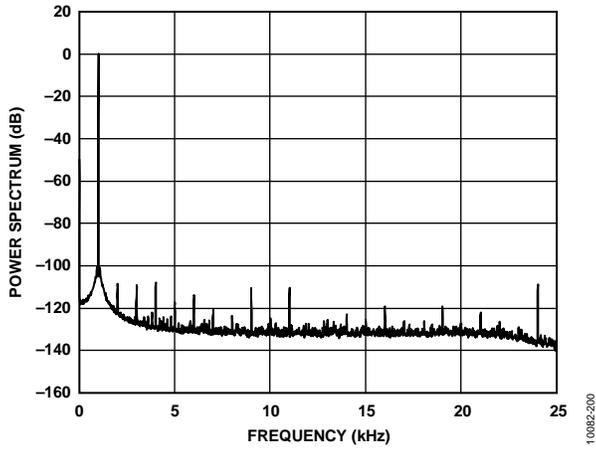


Figure 10. Analog Total Harmonic Distortion

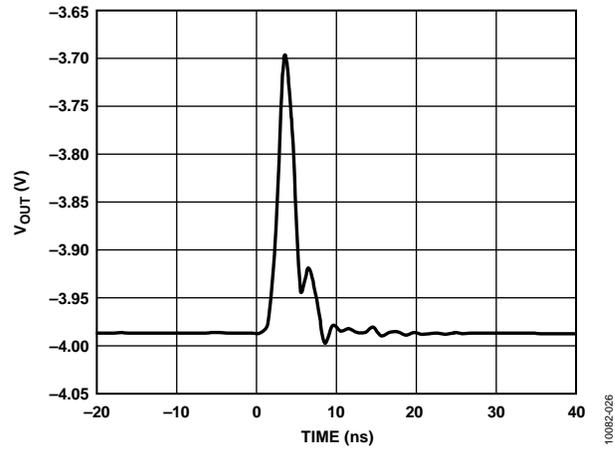


Figure 12. Midscale Transition and Digital Feedthrough

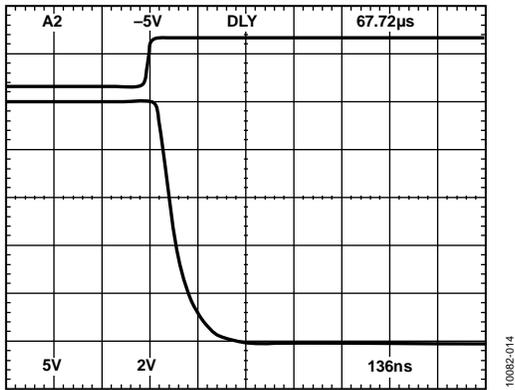
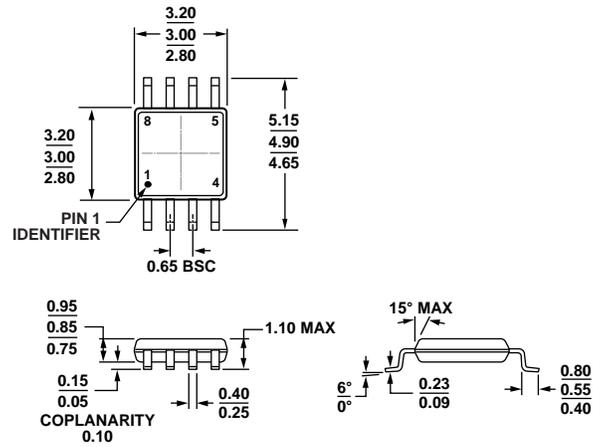


Figure 11. Settling Time

### OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 13. 8-Lead Mini Small Outline Package [MSOP] (RM-8)

Dimensions shown in millimeters

10-07-2009-B

### ORDERING GUIDE

Model <sup>1, 2</sup>	INL (LSB)	RES (LSB)	Temperature Range	Package Description	Package Option	Branding
AD5543SRMZ-EP	±3	16	-55°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	DHR

<sup>1</sup> The AD5543 contains 1040 transistors. The die size measures 55 mil × 73 mil or 4,015 sq. mil.

<sup>2</sup> Z = RoHS Compliant Part.

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