FAIRCHILD
SEMICONDUCTOR®

SPT5230

10-BIT, 36 MWPS TRIPLE VIDEO DAC

FEATURES

- 10-Bit Triple Video Digital-to-Analog Converter
- Output Full-Scale Voltage 0.5 to 2.0 Vp-p
- 36 MWPS Operation (typ)
- Low Power: 280 mW (1 Vp-p Output)
- 5 V Monolithic CMOS
- 52-pin QFP Package (10mm x 10mm, 0.65 mm pitch)

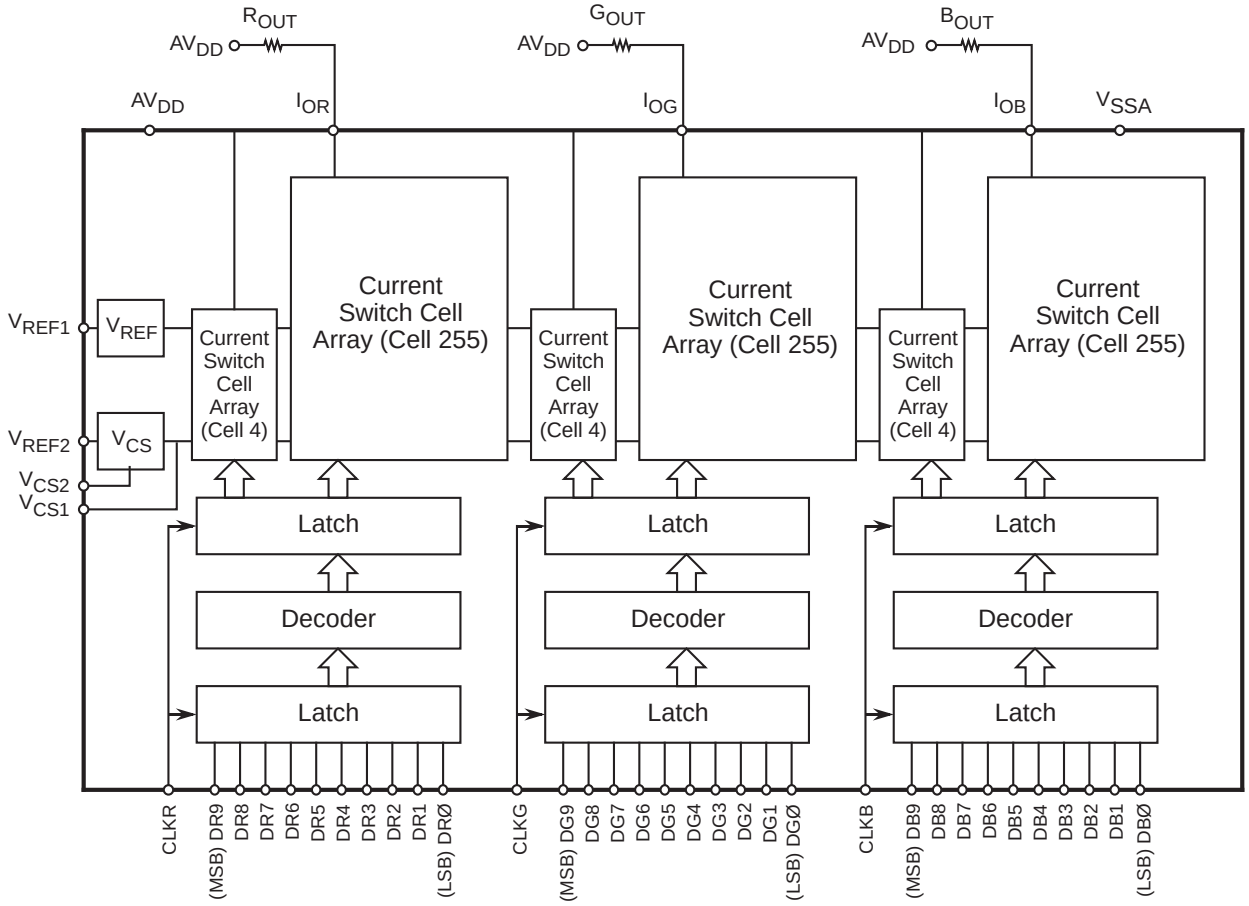
APPLICATIONS

- Desktop Video Processing
- CCIR-601 Video Signal Processing
- RGB Color Monitors
- Image Processing
- Direct Digital Synthesis

GENERAL DESCRIPTION

The SPT5230 is a 10-bit, 36 MWPS triple video digital-to-analog converter specifically designed for high performance, high resolution color graphics monitor applications and video processing applications. A single external resistor controls the full-scale output current. The differential linearity errors of the DACs are guaranteed to be a maximum of ±1.0 LSB over the full temperature range. The device is available in a 52-lead QFP package over the commercial temperature range.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1]

Supply Voltages

AV_{DD} (measured to AV_{SS}) ..... –0.3 to 7.0 V

Input Voltage

Clock and Data ..... AV_{SS} to AV_{DD}

Output Current

I_{OUT} ..... 0 to 14 mA

Temperature

Operating, ambient ..... 0 to +70 °C

Storage ..... –55 to + 125 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

f_{CLK} = 27 MWPS, AV_{DD} = 5.0 V, Output Pull-Up Load = 75 Ω, T_A = 25 °C, AV_{SS} = 0.0 V

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC Performance						
Resolution				10.0		Bits
Differential Linearity	$T_A = T_{MIN}$ to T_{MAX}	I	–1.0		1.0	LSB
Integral Linearity		I	–2.5		2.0	LSB
Analog Outputs						
Output Voltage Range	V_{CS2} = +2.1 V	I	3.0		5.0	V
Conversion Rate		I	27	36		MWPS
Output Offset Voltage		I		2.4	14	mV
Signal-to-Noise Ratio		I	46	52		dB
Settling Time[1]		I		16	23	ns
Propagation Delay (t_{pd})		V		10	12	ns
Crosstalk		I	–49	–54		dB
FS Control Voltage (V_{CS2})		V	2.0		4.0	V
Digital Inputs and Timing						
Input Current, Logic High	V_{IH} = 5 V	I			5	µA
Logic Low	V_{IL} = 0 V	I	–5			µA
Set-Up Time, Data and Controls (t_S)		I	5			ns
Hold Time, Data and Controls (t_h)		I	10			ns
Clock Duty Cycle		V	40		60	%
Power Supply Requirements						
Supply Voltage		I	4.75		5.25	V
Supply Current	1 Vp-p Output	IV			56	mA
	2 Vp-p Output	I			100	mA
Power Dissipation	1 Vp-p Output	IV			280	mW
	2 Vp-p Output	I		485	500	mW

[1]Full-scale settling time to within ±2% of full scale.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

INTERFACE CONSIDERATIONS

Figure 4 shows a typical interface circuit of the SPT5230 in normal circuit operation.

SUPPLY AND GROUND CONSIDERATIONS

Fairchild suggests that all power supply pins (AV_{DD}) be tied together and decoupled using a 0.1 µF ceramic capacitor in parallel with a 10 µF tantalum capacitor.

EXTERNAL REFERENCE VOLTAGE (V_{REF1})

A +3 V (±10%) voltage reference should be externally generated for the V_{REF1} pin using the simple voltage divider shown in figure 4. Connect a 0.1 µF bypass capacitor between V_{REF1} and AV_{SS} as close to the pin as possible.

EXTERNAL REFERENCE VOLTAGE (V_{REF2})

V_{REF2} needs to be externally connected to AV_{DD} through a 1.2 kΩ (5%) resistor. Connect a 0.1 µF bypass capacitor between V_{REF2} and AV_{SS} as close to the pin as possible.

CONTROL VOLTAGE DECOUPLING (V_{CS1})

This is a decoupling pin for the control voltage internal circuitry. An external 0.1 µF capacitor should be connected between V_{CS1} and AV_{SS} as close to the pin as possible.

FULL-SCALE ADJUST CONTROL (V_{CS2})

V_{CS2} is an external control voltage input that controls the peak-to-peak full scale output voltage. This is the only external voltage that has direct control over the SPT5230 output voltage. The voltage output swings between AV_{DD} (+5 V) and a value controlled by V_{CS2}.

Assuming that an output load resistor of 75 Ω is connected between the output and AV_{DD}, figure 2 shows what the output voltage will be for the digital inputs all equal to logic 0, as V_{CS2} is varied from 2 V to 4 V. Figure 3 shows the peak-to-peak output voltage versus V_{CS2} and table I shows an example in which V_{CS2} is equal to 2.1 V.

CURRENT OUTPUTS

Each red, green and blue current output should have a load resistor connected to AV_{DD}. The resistors are typically 75 Ω and should be kept in the 72 Ω to 85 Ω range. The outputs should drive a high impedance load such as a voltage follower.

OUTPUT LEVEL SHIFTING CIRCUIT

The SPT5230 voltage output will swing from +3.0 V to +4.99 V for V_{CS2} = 2.1 V as shown in table I. If level shifting of the output is desired, Fairchild recommends use of the circuit shown in figure 5. The desired –FS voltage is fed into the collector of the emitter to achieve the desired level shift. (Note the phase inversion that will occur due to the common emitter.) Choose any appropriate video op amp with adequate power supply head room.

Table I – Binary Codes
1 LSB = 1.953 mV, $V_{CS2} \approx$ 2.1 V

Step	Digital Input A9 (MSB)	A8	A7	A6	A5	A4	A3	A2	A1	A0 (LSB)	Analog Out (V)
0	0	0	0	0	0	0	0	0	0	0	3.000000
1	0	0	0	0	0	0	0	0	0	1	3.001953
2	0	0	0	0	0	0	0	0	1	0	3.003906
3	0	0	0	0	0	0	0	0	1	1	3.005859
.				.					.		
.				.					.		
.				.					.		
1022	1	1	1	1	1	1	1	1	1	0	4.996094
1023	1	1	1	1	1	1	1	1	1	1	4.998047

Figure 1 – Timing Diagram

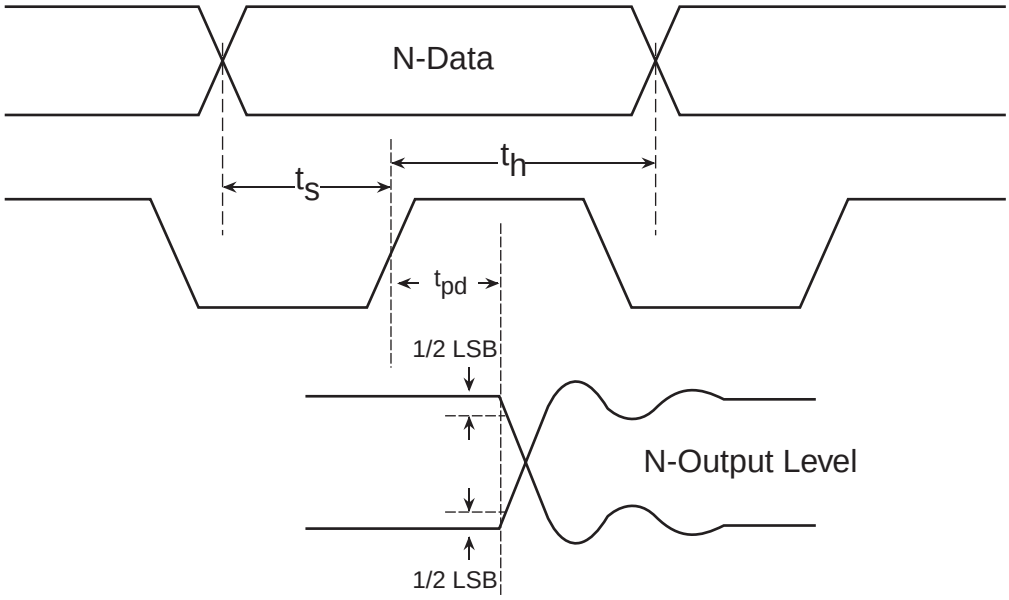
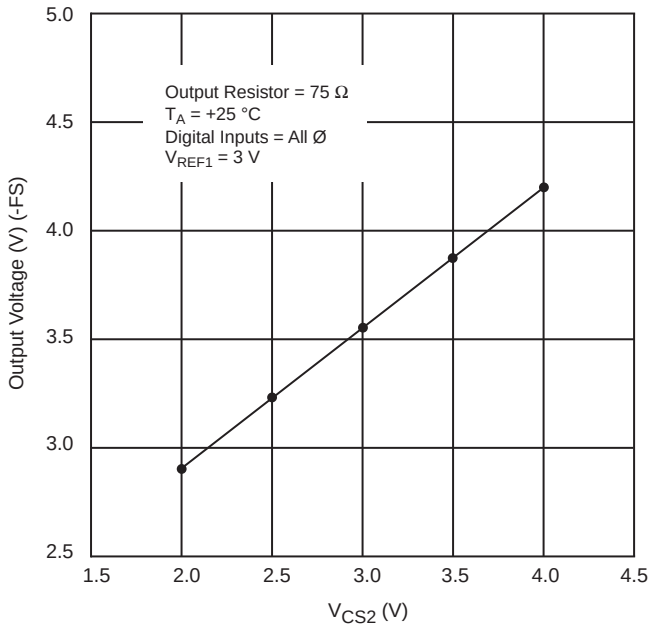


Figure 2 – Output Voltage with All Digital Inputs = Ø versus V_{CS2}



NOTE: For Digital Inputs = All 1, Output Voltage = +4.998047 V.

Figure 3 – Output Voltage (Vp-p) versus V_{CS2}

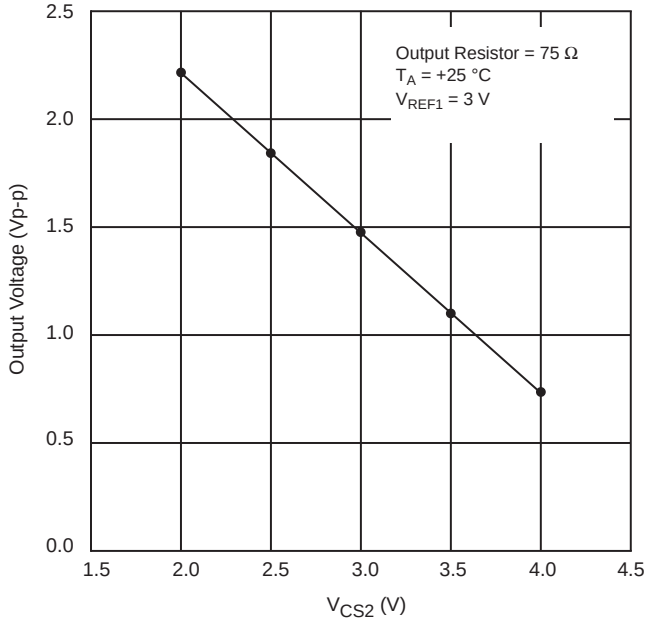


Figure 4 – Typical Interface Circuit

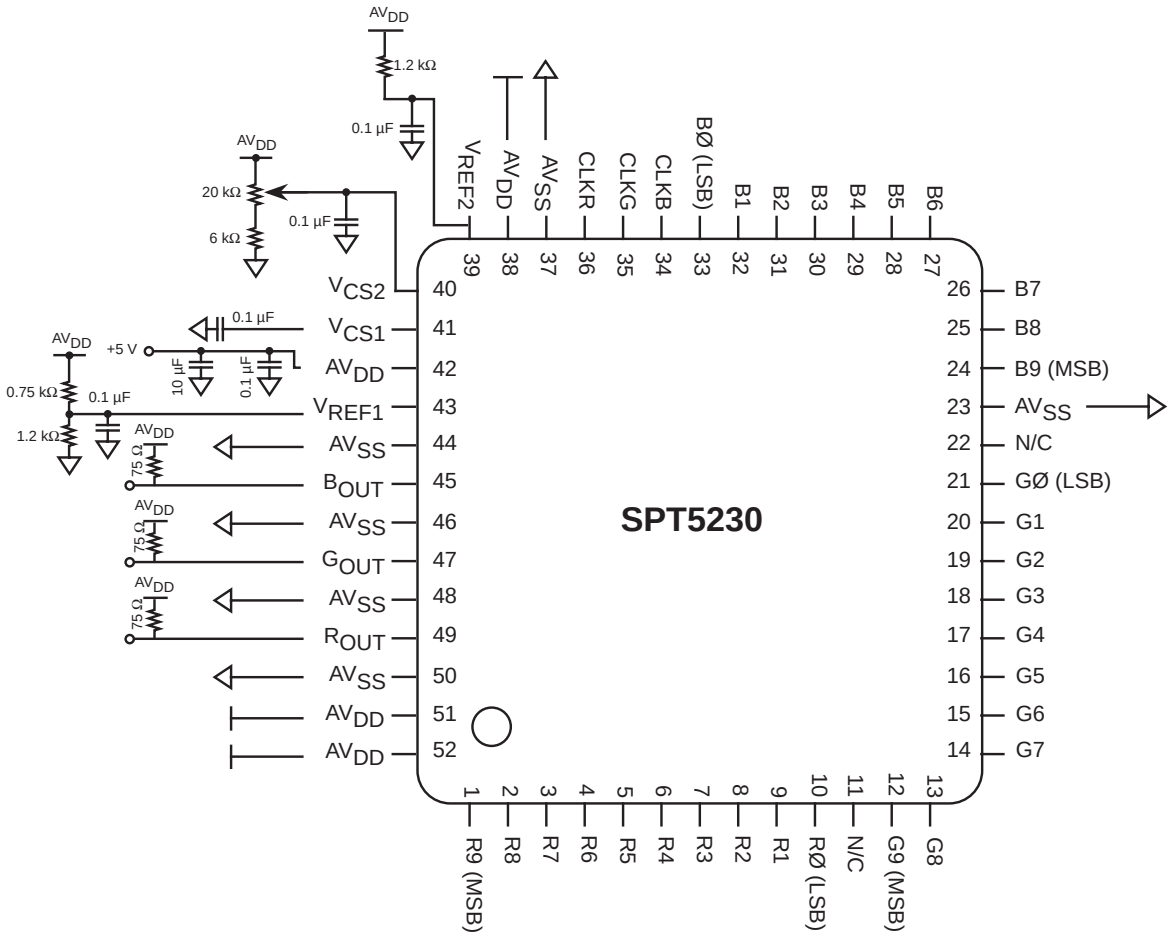
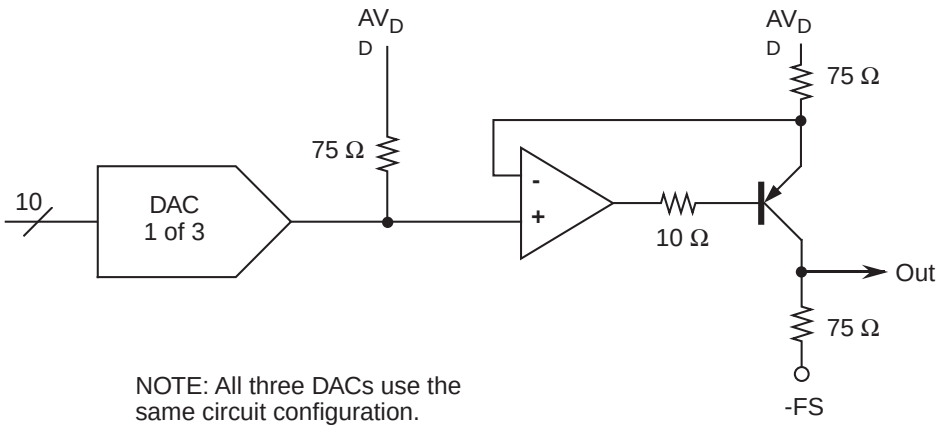


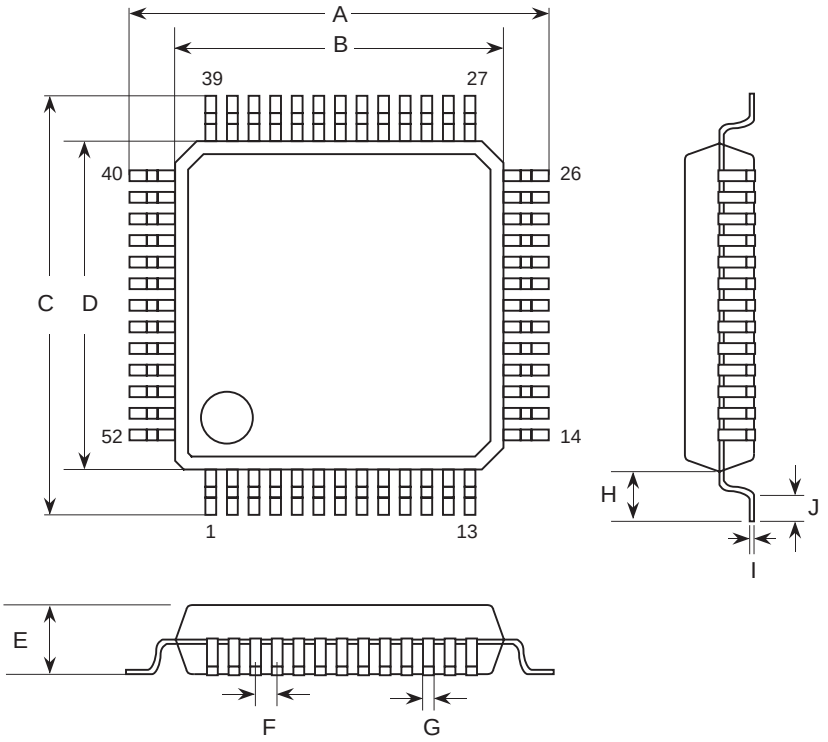
Figure 5 – Recommended Output Level Shifting Circuit



NOTE: All three DACs use the same circuit configuration.

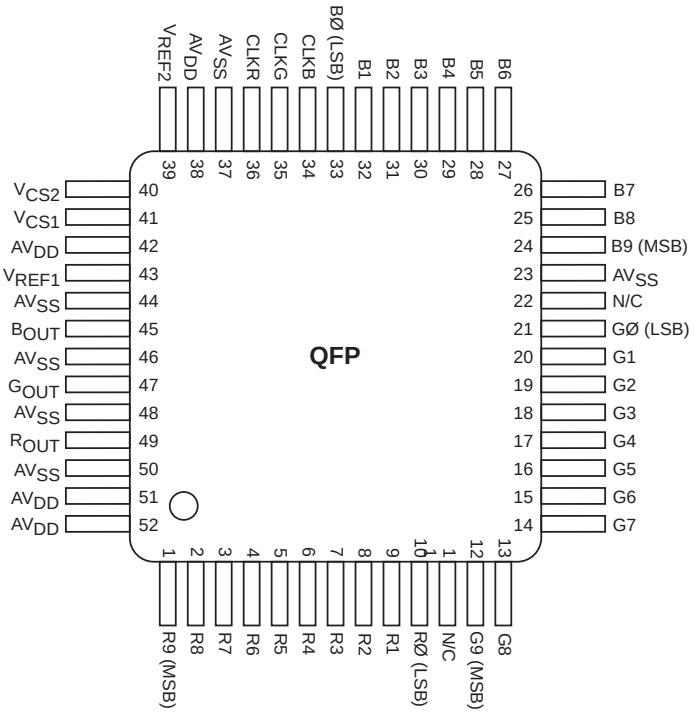
PACKAGE OUTLINE

52-Lead QFP



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.507	0.523	13.0	13.4
B	0.386	0.394	9.9	10.1
C	0.507	0.523	13.0	13.4
D	0.386	0.394	9.9	10.1
E	0.070	0.090	1.80	2.30
F	0.025 typ		0.65 typ	
G	0.008	0.016	0.2	0.4
H	0.062 typ		1.6 typ	
I	0.004	0.008	0.1	0.2
J	0.023	0.039	0.6	1.0

PIN ASSIGNMENTS



PIN FUNCTIONS

Name	Function
R_{OUT}	Red Analog Current Output
G_{OUT}	Green Analog Current Output
B_{OUT}	Blue Analog Current Output
R0–R9	Red Data Inputs
G0–G9	Green Data Inputs
B0–B9	Blue Data Inputs
CLKR	Red Clock Input
CLKG	Green Clock Input
CLKB	Blue Clock Input
V_{REF1}	Voltage Reference Input 1 (A 0.1 µF ceramic capacitor should be used.)
V_{REF2}	Voltage Reference Input 2 (A 0.1 µF ceramic capacitor should be used.)
V_{CS1}	Control Voltage Decoupling (A 0.1 µF ceramic capacitor should be used.)
V_{CS2}	Full-Scale Adjust Control Voltage (A 0.1 µF ceramic capacitor should be used.)
AV_{SS}	Analog Ground
AV_{DD}	Analog Power Supply Voltage
N/C	No Connection

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
SPT5230SCT	0 to +70 °C	52L QFP

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