

### 1.1 Scope.

This specification covers the detail requirements for a precision, ultrahigh speed, current/voltage output 12-bit resolution, multiplying D/A converter.

### 1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD668SQ/883B

### 1.23 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-24.

### 1.3 Absolute Maximum Ratings ( $T_A = +25^\circ\text{C}$ unless otherwise noted)

$V_{CC}$ to REFCOM	0 V to +18 V
$V_{EE}$ to REFCOM	0 V to -18 V
REFCOM to LCOM	+100 mV to -10 V
ACOM to LCOM	$\pm 100$ mV
THCOM to LCOM	$\pm 500$ mV
REFCOM to REFIN (1, 2)	18 V
$I_{BPO}$ to LCOM	$\pm 5$ V
$I_{OUT}$ to LCOM	-5 V to $V_{TH}$
Digital Inputs to THCOM	-500 mV to +7 V
REFIN1 to REFIN2	36 V
$V_{TH}$ to THCOM	-0.7 V to +1.4 V
Logic Threshold Control Input Current	5 mA
Power Dissipation	670 mW
Storage Temperature Range Q (Cerdip) Package	-65°C to +150°C
Junction Temperature	+175°C
Lead Temperature Range (Soldering 10 seconds)	+300°C

### 1.5 Thermal Characteristics.

Thermal Resistance:  $\theta_{JC} = 25^\circ\text{C}/\text{W}$   
 $\theta_{JA} = 75^\circ\text{C}/\text{W}$

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Table 1.

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Test Condition <sup>1</sup>	Units
Relative Accuracy <sup>2</sup>	RA	-1	1/2	1/2	3/4	All Bits with Positive Errors On, All Bits with Negative Errors On	±LSB max
Differential Nonlinearity <sup>2</sup>	DNL	-1	1	1	1	Major Carry Errors	±LSB max
Gain Error <sup>2</sup>	A <sub>E</sub>	-1	1.0	1.0		All Bits On	±% FSR max
Gain Temperature Coefficient <sup>3</sup>	TCA <sub>E</sub>	-1	40 150		40	All Bits On, V <sub>OUT</sub> Mode All Bits On, I <sub>OUT</sub> Mode	± ppm/°C max ± ppm/°C typ
Unipolar Offset Error <sup>2</sup>	V <sub>OS</sub>	-1	0.20	0.20		All Bits Off	±% FSR max
Unipolar Offset TC <sup>3</sup>	TCV <sub>OS</sub>	-1	8		8	All Bits Off	± ppm/°C max
Bipolar Offset Error <sup>2</sup>	B <sub>POE</sub>	-1	1.0	1.0		All Bits Off, Bipolar	±% FSR max
Bipolar Offset TC <sup>3</sup>	TCB <sub>POE</sub>	-1	25		25	All Bits Off, Bipolar	± ppm/°C max
Bipolar Zero Error <sup>2</sup>	B <sub>PZE</sub>	-1	0.50	0.50		MSB On, All Other Bits Off, Bipolar	±% FSR max
Bipolar Zero TC <sup>3</sup>	TCB <sub>PZE</sub>	-1	20		20	MSB On, All Other Bits Off, Bipolar	± ppm/°C max
Analog Offset Error <sup>2</sup>	A <sub>VOS</sub>	-1	1.0	1.0		All Bits On	±% of V <sub>NOM</sub> max
Analog Offset TC <sup>3</sup>	TCA <sub>VOS</sub>	-1	20		20	All Bits On	± ppm of V <sub>NOM</sub> max
Output Resistance	R <sub>OUT</sub>	-1	160 240				Ω min Ω max
Voltage Settling Time	t <sub>SV</sub>	-1	110				ns typ to 0.025%
Current Settling Time	t <sub>SI</sub>	-1	90				ns typ to 0.025%
Full-Scale Transition	t <sub>FS</sub>	-1	11			10% to 90% Rise Time 90% to 10% Fall Time	ns typ
Glitch Impulse	GI	-1	350				pV sec typ
Compliance Voltage	CV	-1	2 1.2				-V min +V max
Output Current	I <sub>OUT</sub>	-1		10.137 10.343		Unipolar All Bits On	+mA min +mA max
				5.017 5.223		Bipolar All Bits On	+mA min +mA max
Power Supply Rejection Ratio	PSRR	-1	0.05	0.05		V <sub>CC</sub> = +15 V ± 10%, +12 V ± 10% V <sub>EE</sub> = -15 V ± 10%, -12 V ± 10%	±% FS/V max
Power Supply Current <sup>4, 5</sup>	I <sub>CC</sub> I <sub>EE</sub>	-1 -1	32 9	32 9		All Bits High	+mA max -mA max
Power Consumption	P <sub>C</sub>	-1	615				mW max
Digital Input High Voltage	V <sub>IH</sub>	-1	2.0	2.0	2.0		+V min
Digital Input Low Voltage	V <sub>IL</sub>	-1	0.8	0.8	0.8		+V max
Digital Input High Current	I <sub>IH</sub>	-1	10	10	10	V <sub>IH</sub> = 2 V	±μA max
Digital Input Low Current	I <sub>IL</sub>	-1	0.5 100	0.5 100	0.5 200	V <sub>IL</sub> = 0.0 V	-μA min -μA max

NOTES

<sup>1</sup>V<sub>CC</sub> = +15 V, V<sub>EE</sub> = -15 V, V<sub>IH</sub> = 2.0 V, V<sub>IL</sub> = 0.8 V, REFIN2 = +5 V in series with a 50 Ω resistor, REFIN1 = GND, T<sub>A</sub> = +25°C unless otherwise specified.

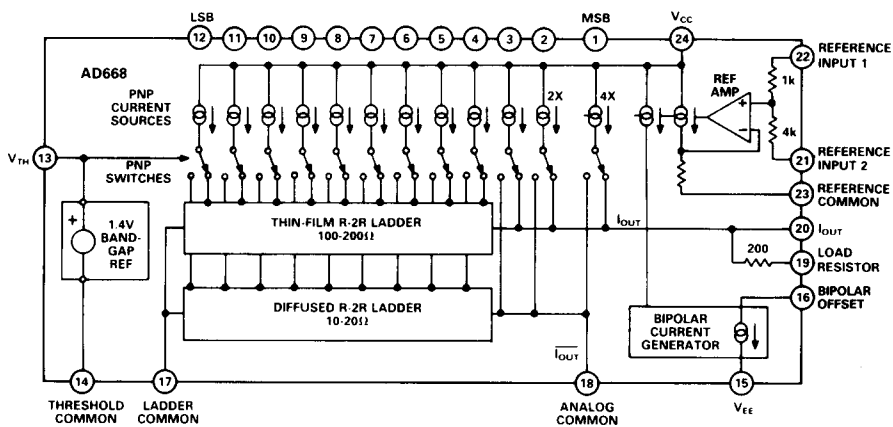
<sup>2</sup>Measured in I<sub>OUT</sub> mode.

<sup>3</sup>Measured in V<sub>OUT</sub> mode.

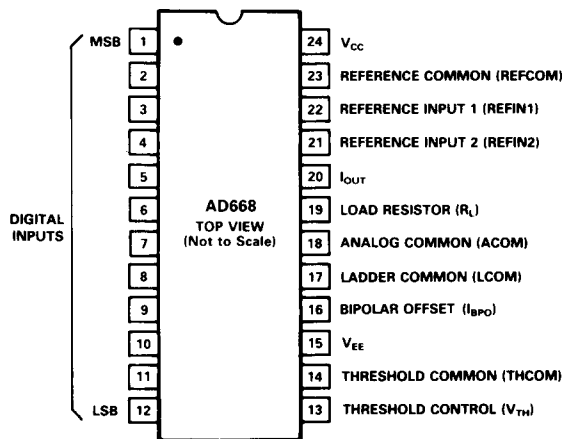
<sup>4</sup>Guaranteed for +10.8 V ≤ V<sub>CC</sub> ≤ +16.5 V.

<sup>5</sup>Guaranteed for -10.8 V ≤ V<sub>EE</sub> ≤ -16.5 V.

## 3.2.1 Functional Block Diagram and Terminal Assignments.



24-Lead Cerdip Package



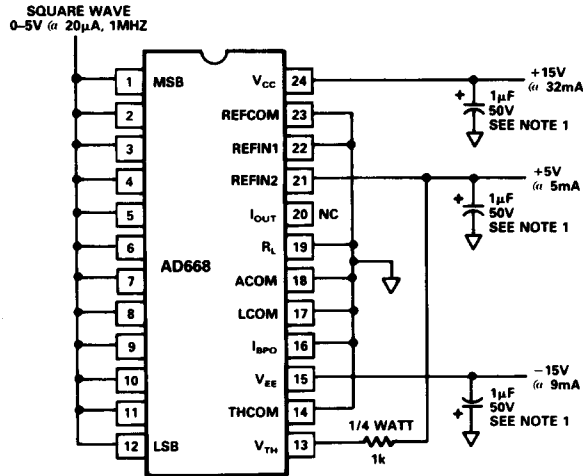
## 3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (56).

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## 4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



### NOTES

1. CAPACITORS EVERY 10 DEVICES.
2. ALL CURRENT RATINGS ARE MAX/PART.