T-51-09-12

BURR-BROWN®

DAC811L

LCC Microprocessor-Compatible 12-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- SINGLE INTEGRATED CIRCUIT CHIP
- MICROCOMPUTER INTERFACE: DOUBLE BUFFERED LATCH
- VOLTAGE OUTPUT: ±10V, ±5V, +10V
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- ±1/2LSB MAXIMUM NONLINEARITY OVER TEMPERATURE
- GUARANTEED SPECIFICATIONS AT ±12V AND ±15V SUPPLIES
- TTL/5V CMOS-COMPATIBLE LOGIC INPUTS
- HERMETIC SURFACE MOUNT PACKAGE

DESCRIPTION

The DAC811L is a complete single-chip integrated circuit microcomputer-compatible 12-bit digital-to-analog converter. The chip includes a precision voltage reference, microcomputer interface logic, double-buffered latch, and a 12-bit D/A converter with a voltage output amplifier. Fast current switches and a laser-trimmed thin-film resistor network provide a highly accurate and fast D/A converter.

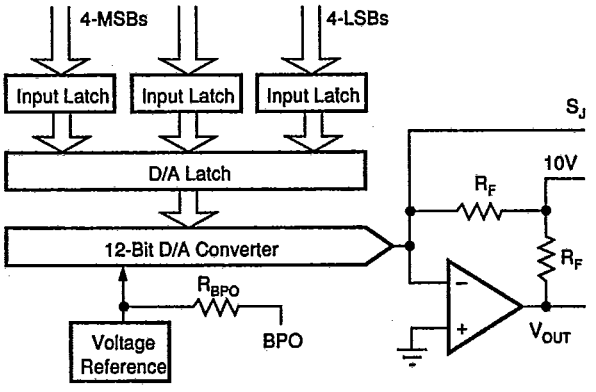
Microcomputer interfacing is facilitated by a double-buffered latch. The input latch is divided into three 4-bit nibbles to permit interfacing to 4-, 8-, 12-, or 16-bit buses and to hand right- or left-justified data. The 12-bit data in the input latches in transferred to the D/A latch to hold the output value.

Input gating logic is designed so that loading the last nibble or byte of data can be accomplished simultaneously with the transfer of data (previously stored in adjacent latches) from adjacent input latches to the D/A latch. This feature avoids spurious analog output values while using an interface technique that saves computer instructions.

The DAC811L is laser trimmed at the wafer level and is specified to ±1/4LSB maximum linearity error (B and S grades) at 25°C and ±1/2LSB maximum over the temperature range. All grades are guaranteed monotonic over the specification temperature range.

The DAC811L is available in four performance grades. DAC811AL and BL are specified over –25°C to +85°C; DAC811RL and DAC811SL are specified over –55°C to +125°C.

All grades are packaged in a 0.45" (12mm) hermetically sealed 28-pin leadless chip carrier package.



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SPECIFICATIONS

ELECTRICAL

T_A = +25°C. $\pm V_{CC}$ = 12V or 15V unless otherwise noted.

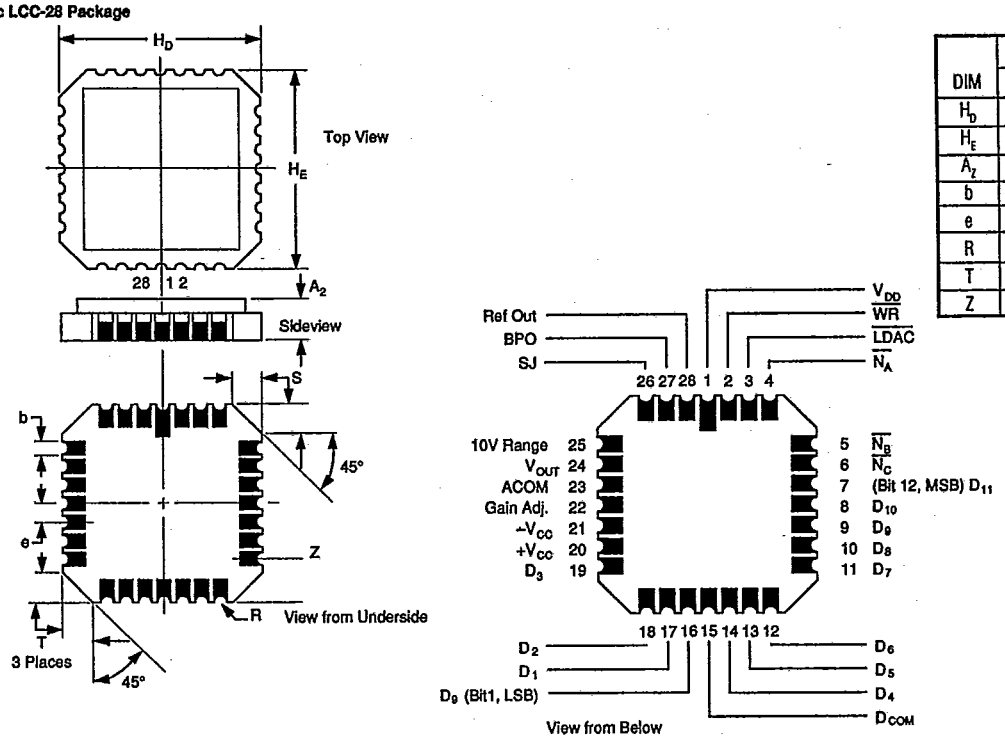
PARAMETER	DAC811 AL			DAC811BL			DAC811RL			DAC811SL			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUT													
Resolution			12			*			*			*	Bits
Codes[1]		USB, BOB			*			*			*		
Digital Inputs Over Temperature Range[2]													
V_{IN}	+2.0		+15	*		*	*		*	*		*	VDC
V_{IL}	0.0		+0.8	*		*	*		*	*		*	VDC
I_{IH}, V_I = +2.7V			+10			*			*			*	µA
I_{IL}, V_I = +0.4V			±20			*			*			*	µA
Digital Interface Timing Over Temperature Range													
t_{WP}, $\overline{WR}$ Pulse Width	50			*			80			*			ns
t_{AW}1, $\overline{N_X}$ and $\overline{LDAC}$ Valid to End of $\overline{WR}$	50			*			80			*			ns
t_{DW}, Data Valid to End of $\overline{WR}$	80			*			80			*			ns
t_{DH}, Data Valid Hold Time	0			*			+10			*			ns
ACCURACY													
Linearity Error		±1/4	±1/2		±1/8	±1/4		±1/4	±1/2		±1/8	±1/4	LSB
Differential Linearity Error		±1/2	±3/4		±1/4	±1/2		±1/2	±3/4		±1/4	±1/2	LSB
Gain Error[3]		±0.1	±0.2		*	*		*	*		*	*	%
Offset Error[3, 4]		±0.05	±0.15		*	*		*	*		*	*	% of FSR[5]
Monotonicity		Guaranteed			*			*			*		
Power Supply Sensitivity: $+V_{CC}$		±0.001	±0.003		*	*		*	*		*	*	% of FSR/%V_{CC}
$-V_{CC}$		±0.002	±0.006		*	*		*	*		*	*	% of FSR/%V_{CC}
V_{DD}		±0.0005	±0.0015		*	*		*	*		*	*	% of FSR/%V_{DD}
DRIFT (Over Specification Temperature Range)													
Gain		±10	±30		±10	±20		±15	±30		±15	±30	ppm/°C
Unipolar Offset		±5	±10		±5	±7		±5	±10		±5	±7	ppm of FSR/°C
Bipolar Zero		±5	±10		±5	±7		±5	±10		±5	±7	ppm of FSR/°C
Linearity Error Over Temperature Range		±1/2	±3/4		±1/4	±1/2		±1/2	±3/4		±1/4	1/2	LSB
Monotonicity Over Temperature Range		Guaranteed			*			*			*		
SETTLING TIME[6] (to within ±0.01% of FSR of Final Value; 2kΩ load)													
For Full Scale Range Change, 20V Range		3	4		*	*		*	*		*	*	µs
10V Range		3	4		*	*		*	*		*	*	µs
For 1LSB Change at Major Carry[7]		1			*			*			*		µs
Slew Rate[6]	8	12		*	*		*	*		*	*		V/µs
ANALOG OUTPUT													
Voltage Range ($\pm V_{CC}$ = 15V)[8]: Unipolar		0 to +10			*			*			*		V
Bipolar		±5, ±10			*			*			*		V
Output Current	±5			*			*			*			mA
Output Impedance (at DC)		0.2			*			*			*		Ω
Short Circuit to Common Duration		Indefinite			*			*			*		Ω
REFERENCE VOLTAGE													
Voltage	+6.2	+6.3	+6.4	*	*	*	*	*	*	*	*	*	V
Source Current Available for External Loads	+2.0			*			*			*			mA
Temperature Coefficient		±10	±30		±10	±20		±10	±30		±10	±20	ppm/°C
Short Circuit to Common Duration		Indefinite			*			*			*		
POWER SUPPLY REQUIREMENTS													
Voltage: $+V_{CC}$	+11.4	+15	+16.5	*	*	*	*	*	*	*	*	*	VDC
$-V_{CC}$	−11.4	−15	−16.5	*	*	*	*	*	*	*	*	*	VDC
V_{DD}	+4.5	+5	+5.5	*	*	*	*	*	*	*	*	*	VDC
Current (no load): $+V_{CC}$		+16	+25		*	*	*	*	*	*	*	*	mA
$-V_{CC}$		−23	−35		*	*	*	*	*	*	*	*	mA
V_{DD}		+8	+15		*	*	*	*	*	*	*	*	mA
Potential at DCOM with Respect to ACOM[9]		±0.5			*			*			*		V
Power Dissipation		625	800		*	*		*	*		*	*	mW
TEMPERATURE RANGE													
Specification: A, B	−25		+85	*		*	*		*	*		*	°C
R, S							−55		+125	*		*	°C
Storage: A, B, R, S	−65		+150	*		*	*		*	*		*	°C

*Same as specification to immediate left.

NOTES; (1) USB = Unipolar Straight Binary; BOB = Bipolar Offset Binary. (2) –TTL, LSTTL and 54/74 HC compatible. (3) Adjustable to zero with external trim potentiometer. (4) Error at input code 000_{16} for both unipolar and bipolar ranges. (5) FSR means Full Scale Range and in 20V for the ±10V range. (6) Maximum represents the 3σ limit. Not 100% tested for this parameter. (7) At the major carry, $7FF_{16}$ to 800_{16} and 800_{16} to $7FF_{16}$. (8) Minimum supply voltage required for ±10V output swing is ±13.5V. Output swing for ±11.4V supplies is at least –8V to+8V. (9) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

MECHANICAL

Ceramic LCC-28 Package



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
H_D	.442	.458	11.23	11.63
H_E	.442	.458	11.23	11.63
A_2	.064	.100	1.63	2.54
b	.022	.028	0.56	0.71
e	.050 BASIC		1.27 BASIC	
R	.008R TYP		0.20R TYP	
T	.040 TYP		1.016 TYP	
Z	.075 TYP		1.91 TYP	

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$	0 to +18V
$-V_{CC}$ to ACOM	0 to –18V
V_{DD} to DCOM	0 to +7V
V_{DD} to ACOM	±7V
ACOM to DCOM	±7V
Digital Inputs (pins 2-14, 16-19) to DCOM	–0.4V to +18V
External Voltage Applied to 10V Range Resistor	±12V
Ref Out	Indefinite short to ACOM
External Voltage Applied to DAC Output	–5V to +5V
Power Dissipation	1000mW
Operating Temperature	
AL, BL	–25°C to +85°C
RL, SL	–55°C to +125°C
Storage Temperature	–65°C to +150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

DAC811 X L

Basic Model Number

Performance Grade Code
B, A; –25°C to +85°C
S, R; –55°C to +125°C

Package Code
L: 28-pin Leadless Chip Carrier

TABLE I. Digital Input Codes.

DIGITAL INPUT MSB ↓	DIGITAL INPUT LSB ↓	ANALOG OUTPUT USB Unipolar Straight Binary	ANALOG OUTPUT BOB Bipolar Offset Binary	ANALOG OUTPUT BTC* Binary Two's Complement
111111111111		+Full Scale	+Full Scale	–1LSB
100000000000		+1/2 Full Scale	Zero	–Full Scale
011111111111		1/2 Full Scale –1 LSB	–1 LSB	+Full Scale
000000000000		Zero	–Full Scale	Zero

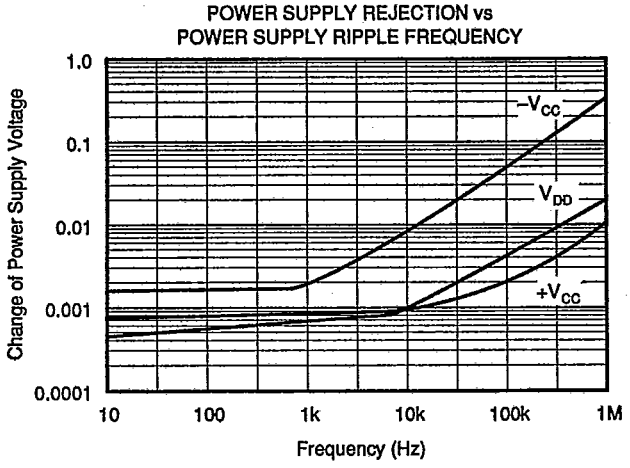
*Invert the MSB of the BOB code with external inverter to obtain BTC code.

PIN NOMENCLATURE

PIN	NAME	FUNCTION
1	V_{DD}	Logic Supply, +5V.
2	$\overline{WR}$	WRITE, command signal to load latches. Logic low loads latches.
3	$\overline{LDAC}$	LOAD D/A CONVERTER, enables $\overline{WR}$ to load the D/A latch. Logic low enables.
4	$\overline{N_A}$	NIBBLE A, enables $\overline{WR}$ to load input latch A (the most significant nibble. Logic low enables.
5	$\overline{N_B}$	NIBBLE B, enables $\overline{WR}$ to load input latch B. Logic low enables.
6	$\overline{N_C}$	NIBBLE C, enables $\overline{WR}$ to load input latch C. (the least significant nibble). Logic low enables.
7	D_{11}	DATA, Bit 12, MSB, positive true.
8	D_{10}	DATE, Bit 11.
9	D_9	DATA, Bit 10.
10	D_8	DATA, Bit 9.
11	D_7	DATA, Bit 8.
12	D_6	DATA, Bit 7.
13	D_5	DATA, Bit 6.
14	D_4	DATA, Bit 5.
15	DCOM	DIGITAL COMMON, V_{DD} supply return.
16	D_0	DATA, Bit 1, LSB.
17	D_1	DATA, Bit 2.
18	D_2	DATA, Bit 3.
19	D_3	DATA, Bit 4.
20	$+V_{CC}$	Analog Supply Input, +15V or +12V.
21	$-V_{CC}$	Analog Supply Input, –15V or –12V.
22	GAIN ADJ	To externally adjust gain.
23	ACOM	ANALOG COMMON, $\pm V_{CC}$ supply return.
24	V_{OUT}	D/A converter voltage output.
25	10V RANGE	Connect to pin 24 for 10V range.
26	SJ	SUMMING JUNCTION of output amplifier
27	BPO	BIPOLAR OFFSET. Connect to pin 26 for Bipolar Operation.
28	REF OUT	6.3V reference output.

TYPICAL PERFORMANCE CURVE

T_A = +25°C, V_S = ±15VDC, V_{DD} = +5VDC unless otherwise noted. For applications information refer to PDS-503.



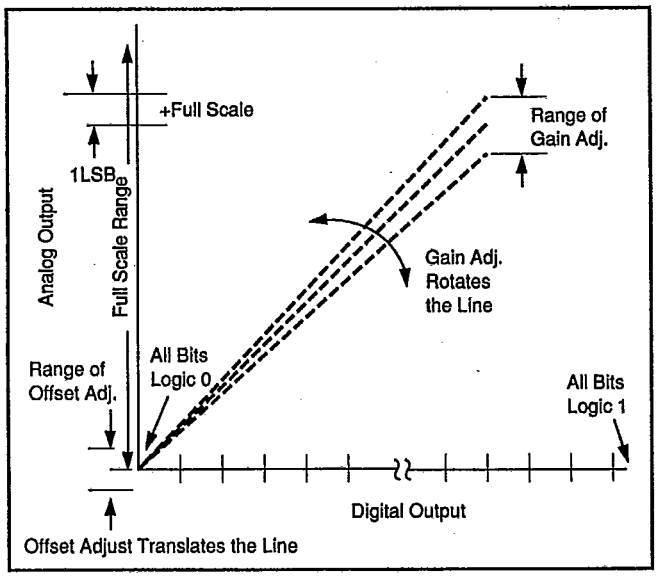
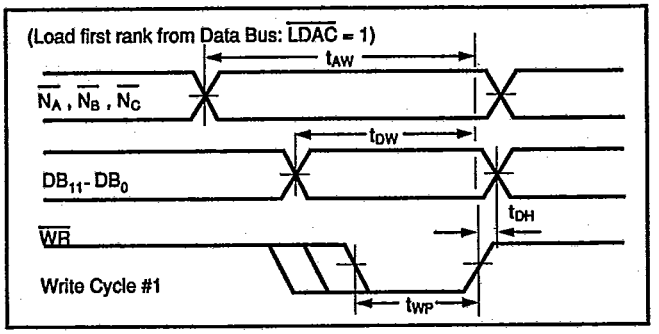
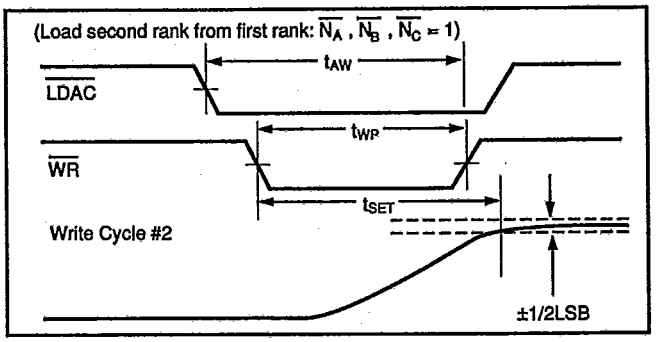


FIGURE 1. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

TIMING DIAGRAM





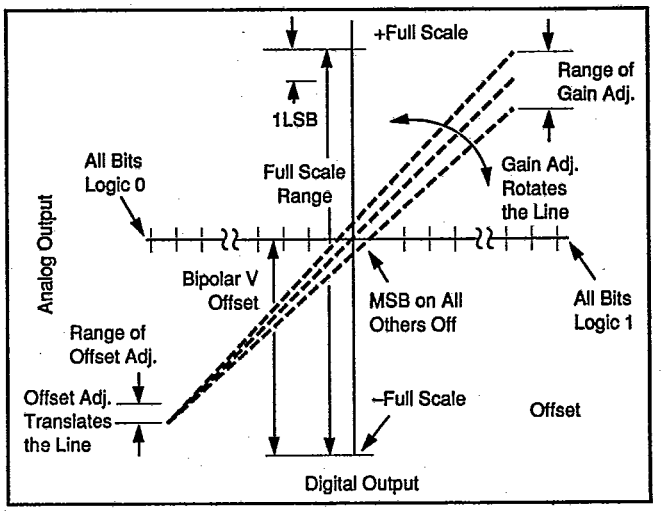


FIGURE 2. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

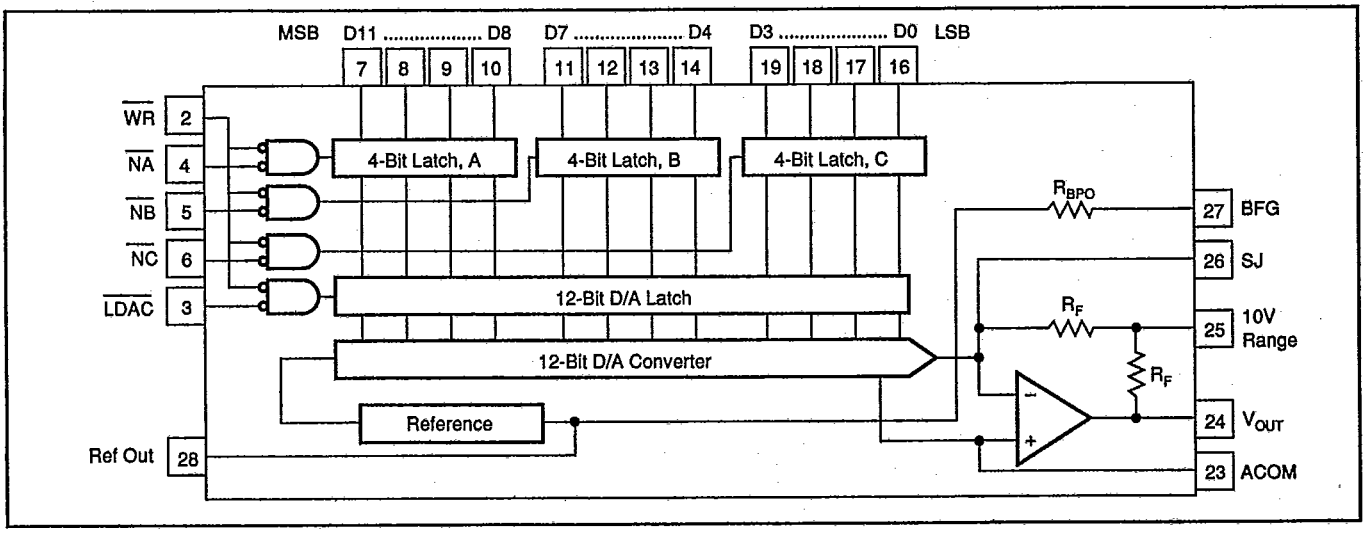


FIGURE 3. DAC811L Block Diagram.