



CMOS Low-Cost 8-Bit Buffered Multiplying DAC

AD7524

T.51-09-08

1.1 Scope.

This specification covers the detail requirements for an 8-bit monolithic CMOS multiplying digital-to-analog converter with on-chip latches for direct interface to most microprocessors. The AD7524 can be used with any supply voltage from +5V to +15V.

1.2 Part Number.

The complete part number per Tables 1 and 2 of this specification is as follows:

Device	Part Number ¹
-1	AD7524S(X)/883B
-2	AD7524T(X)/883B
-3	AD7524U(X)/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D16	16-Pin Side-Brazed Ceramic
Q	Q16	16-Pin Cerdip
E	E20A	20-Contact LCC

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted)

V_{DD} to GND	-0.3V, +17V
V_{RFB} to GND	$\pm 25\text{V}$
V_{REF} to GND	$\pm 25\text{V}$
Digital Input Voltage to GND	-0.3V to V_{DD}
V_{OUT1}, V_{OUT2} (Pin 1, Pin 2) to Ground	-0.3V to V_{DD}
Power Dissipation	
Up to +75°C	450mW
Derates above +75°C	6mW/°C
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{jc} = 35^\circ\text{C/W}$ for D16, Q16 and E20A
 $\theta_{ja} = 120^\circ\text{C/W}$ for D16, Q16 and E20A

AD7524 - SPECIFICATIONS

Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2,3	Sub Group 4	Test Condition ¹ $V_{DD} = +15V$	Units
Resolution	RES	-1,2,3	8					Bits
Relative Accuracy	RA	-1	1/2	1/2	1/2			± LSB max
		-2	1/4	1/2	1/4	1/4		
		-3	1/8	1/2	1/8	1/8		
Gain Error ²	AE	-1,2,3	0.6	0.5	0.6			± % FSR max
Gain Tempco	TC _{AE}	-1,2,3	10				From +25°C to T_{max} to T_{min}	± ppm/°C max
Power Supply Rejection	PSRR	-1,2,3	0.04	0.02	0.04		$\Delta V_{DD} = \pm 10\%$	± %/° max
Output Leakage Current I_{OUT1} I_{OUT2}	I_{OL}	-1,2,3	200	50	200		DB0-DB7 = 0V, $\overline{WR} = \overline{CS} = 0V$	± nA max
	I_{OL}	-1,2,3	200	50	200		DB0-DB7 = V_{DD} , $\overline{WR} = \overline{CS} = 0V$	± nA max
Output Current Settling Time	t_{SL}	-1,2,3	350				$T_o \pm 1/2LSB$; $R_{OUT1} = 100\Omega$ $C_{OUT1} = 13pF$; $\overline{WR} = \overline{CS} = 0V$; DB0-DB7 = 0V to V_{DD} or V_{DD} to 0V	ns max
Feedthrough Error ³	FT	-1,2,3	50				$V_{REF} = +10V$, 100kHz Sinewave; DB0-DB7 = 0V; $\overline{WR} = \overline{CS} = 0V$	mV p-p max
Input Resistance (Pin 15)	R_{IN}	-1,2,3	5	5	5			kΩ min
			20	20	20			kΩ max
Digital Input High Voltage	V_{IH}	-1,2,3	13.5	13.5	13.5			V min
Digital Input Low Voltage	V_{IL}	-1,2,3	1.5	1.5	1.5			V max
Digital Input Leakage Current	I_{IN}	-1,2,3	10	1	10		$V_{IN} = 0V$ or V_{DD}	± μA max
Digital Input Capacitance DB0-DB7 \overline{WR} , \overline{CS}	C_{IN}	-1,2,3	5					pF max
		-1,2,3	20					pF max
Output Capacitance	C_{OUT1}	-1,2,3	120				DB0-DB7 = V_{DD} ; $\overline{WR} = \overline{CS} = 0V$	pF max
	C_{OUT2}	-1,2,3	30					
	C_{OUT1}	-1,2,3	30				DB0-DB7 = 0V; $\overline{WR} = \overline{CS} = 0V$	pF max
	C_{OUT2}	-1,2,3	120					
Supply Current	I_{DD}	-1,2,3	2	2	2		All Digital Inputs = V_{IL} or V_{IH} All Digital Inputs = 0V or V_{DD}	mA max
			500	100	500			μA max
Chip Select to Write Setup Time ⁴	t_{CS}	-1,2,3	150					ns min
Chip Select to Write Hold Time ⁴	t_{CH}	-1,2,3	0					ns min
Write Pulse Width ⁴	t_{WR}	-1,2,3	150					ns min
Data Setup Time ⁴	t_{DS}	-1,2,3	100					ns min
Data Hold Time ⁴	t_{DH}	-1,2,3	10					ns min

NOTES

¹ $V_{OUT1} = V_{OUT2} = 0V$; $V_{REF} = +10V$ unless otherwise stated.²Measured using internal R_{FB} and includes effect of leakage current and gain TC.³Feedthrough error can be reduced by connecting the metal lid on the package to ground.⁴Timing per Figure 1.

Table 1.

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Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹ $V_{DD} = +5V$	Units
Resolution	RES	-1, 2, 3	8					Bits
Relative Accuracy	RA	-1, 2, 3	1/2	1/2	1/2			± LSB max
Gain Error ²	AE	-1, 2, 3	1.4	1.0	1.4			± % FSR max
Gain Tempco	TC _{AE}	-1, 2, 3	40				From +25°C to T_{max} to T_{min}	± ppm/°C max
Power Supply Rejection	PSRR	-1, 2, 3	0.16	0.08	0.16		$\Delta V_{DD} = \pm 10\%$	± %/° max
Output Leakage Current I_{OUT1} I_{OUT2}	I_{OL}	-1, 2, 3	400	50	400		DB0-DB7 = 0V; $\overline{WR} = \overline{CS} = 0V$	± nA max
	I_{OL}	-1, 2, 3	400	50	400		DB0-DB7 = V_{DD} ; $\overline{WR} = \overline{CS} = 0V$	± nA max
Output Current Settling Time	t_{SL}	-1, 2, 3	500				$T_o \pm 1/2LSB$; $R_{OUT1} = 100\Omega$ $C_{OUT1} = 13pF$; $\overline{WR} = \overline{CS} = 0V$; DB0-DB7 = 0V to V_{DD} or V_{DD} to 0V	ns max
Feedthrough Error ³	FT	-1, 2, 3	50				$V_{REF} = +10V$, 100kHz Sinewave; DB0-DB7 = 0V; $\overline{WR} = \overline{CS} = 0V$	mV p-p max
Input Resistance (Pin 15)	R_{IN}	-1, 2, 3	5	5	5			kΩ min
			20	20	20			kΩ max
Digital Input High Voltage	V_{IH}	-1, 2, 3	2.4	2.4	2.4			V min
Digital Input Low Voltage	V_{IL}	-1, 2, 3	0.8	0.8	0.8			V max
Digital Input Leakage Current	I_{IN}	-1, 2, 3	10	1	10		$V_{IN} = 0V$ or V_{DD}	± μA max
Digital Input Capacitance DB0-DB7 $\overline{WR}, \overline{CS}$	C_{IN}	-1, 2, 3	5					pF max
			20					pF max
Output Capacitance	C_{OUT1}	-1, 2, 3	120				DB0-DB7 = V_{DD} ; $\overline{WR} = \overline{CS} = 0V$	pF max
	C_{OUT2}	-1, 2, 3	30					
	C_{OUT1}	-1, 2, 3	30				DB0-DB7 = 0V; $\overline{WR} = \overline{CS} = 0V$	pF max
	C_{OUT2}	-1, 2, 3	120					
Supply Current	I_{DD}	-1, 2, 3	2	2	2		All Digital Inputs = V_{IL} or V_{IH}	mA max
			500	100	500		All Digital Inputs = 0V or V_{DD}	μA max
Chip Select to Write Setup Time ⁴	t_{CS}	-1, 2, 3	240					ns min
Chip Select to Write Hold Time ⁴	t_{CH}	-1, 2, 3	0					ns min
Write Pulse Width ⁴	t_{WR}	-1, 2, 3	240					ns min
Data Setup Time ⁴	t_{DS}	-1, 2, 3	170					ns min
Data Hold Time ⁴	t_{DH}	-1, 2, 3	10					ns min

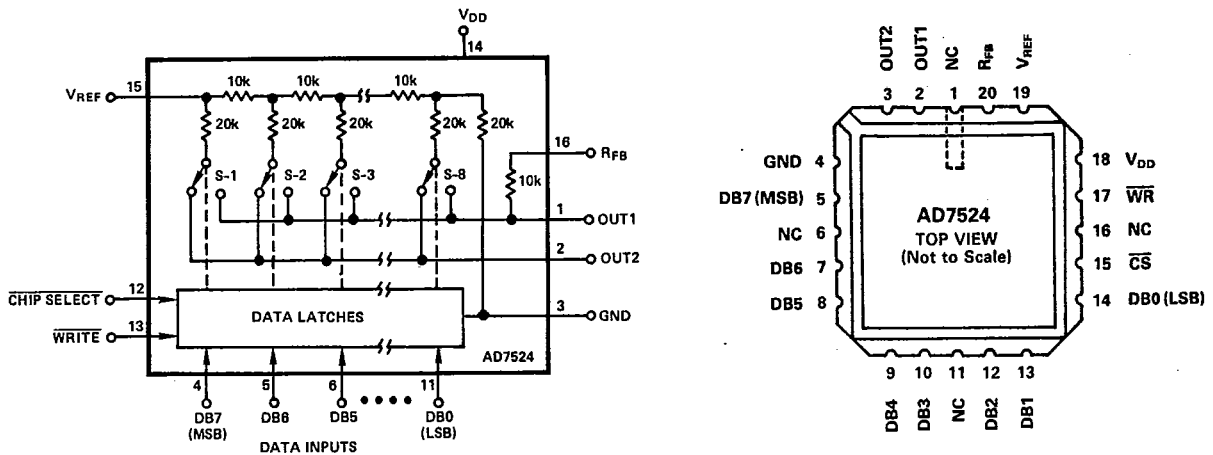
NOTES

¹ $V_{OUT1} = V_{OUT2} = 0V$; $V_{REF} = +10V$ unless otherwise stated.²Measured using internal R_{FB} and includes effect of leakage current and gain TC.³Feedthrough error can be reduced by connecting the metal lid on the package to ground.⁴Timing per Figure 1.

Table 2.

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3.2.1 Functional Block Diagram and Terminal Assignments.

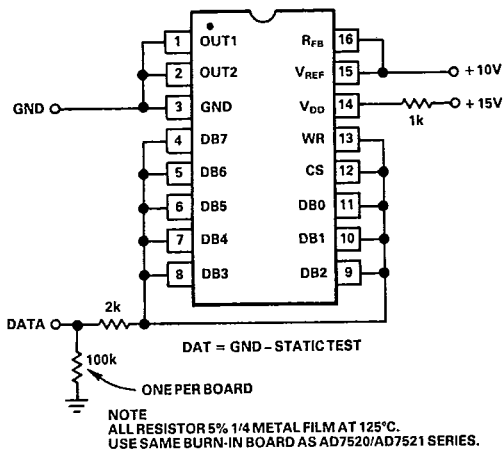


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

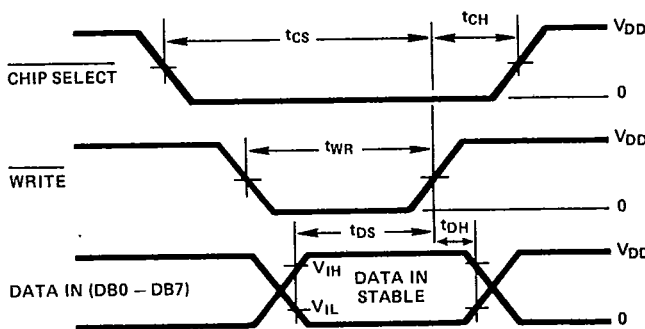
Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



\overline{CS}	\overline{WR}	MODE	DAC RESPONSE
L	L	Write	DAC responds to data bus (DB0 – DB7) inputs
H	X	Hold	Data bus (DB0 – DB7) is locked out;
X	H	Hold	DAC holds last data present when WR or CS assumed HIGH state.

L = Low State, H = High State, X = Don't Care.

Table 3. Mode Selection Table



- NOTES:
- All input signal rise and fall times measured from 10% to 90% of V_{DD} . $V_{DD} = +5V$, $t_r = t_f = 20ns$; $V_{DD} = +15V$, $t_r = t_f = 40ns$.
 - Timing Measurement Reference level is $\frac{V_{IH} + V_{IL}}{2}$
 - $t_{DS} + t_{DH}$ is approximately constant at 145ns min at +25°C, $V_{DD} = +5V$ and $t_{WR} = 170ns$ min. The AD7524 is specified for a minimum t_{DH} of 10ns, however, in applications where $t_{DH} > 10ns$, t_{DS} may be reduced accordingly up to the limit $t_{DS} = 65ns$, $t_{DH} = 80ns$.

Figure 1. Write Cycle Timing Diagram