

**1.1 Scope.**

This specification covers the detail requirements for a monolithic CMOS 12-bit multiplying digital-to-analog converter designed for serial interface applications.

**1.2 Part Number.**

The complete part number per Table 1 of this specification is as follows:

Device	Part Number <sup>1</sup>
-1	AD7543S(X)/883B
-2	AD7543T(X)/883B
-3	AD7543GT(X)/883B

**NOTE**

<sup>1</sup>See paragraph 1.2.3 for package identifier.

**1.2.3 Case Outline.**

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-16	16-Pin Cerdip
E	E-20A	20-Contact LCC

**1.3 Absolute Maximum Ratings.** ( $T_A = 25^\circ\text{C}$  unless otherwise noted. Pin numbers refer to DIP package.)

$V_{DD}$ to AGND	0V, +7V
$V_{DD}$ to DGND	0V, +7V
AGND to DGND	$V_{DD}$
DGND to AGND	$V_{DD}$
Digital Input Voltage to DGND (Pins 4-11, 13)	-0.3V, +15V
$V_{PIN1}, V_{PIN2}$ to AGND	-0.3V, +15V
$V_{REF}$ to AGND	$\pm 25\text{V}$
$V_{RFB}$ to AGND	$\pm 25\text{V}$
Power Dissipation	
Up to +75°C	450mW
Derates above +75°C	6mW/°C
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

**1.5 Thermal Characteristics.**

Thermal Resistance  $\theta_{JC} = 35^\circ\text{C}/\text{W}$  for Q-16 and E-20A  
 $\theta_{JA} = 120^\circ\text{C}/\text{W}$  for Q-16 and E-20A

**8**  
 DIGITAL-TO-ANALOG CONVERTERS

# AD7543—SPECIFICATIONS

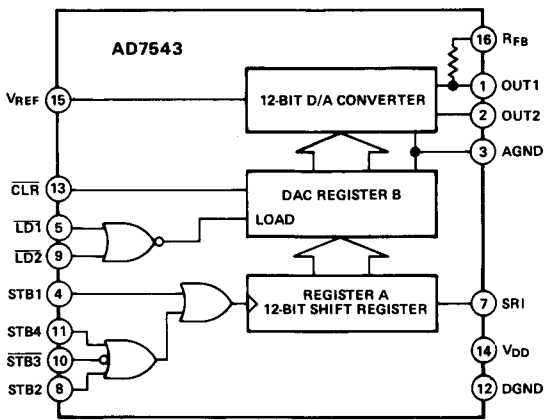
Table 1.

Test	Symbol	Device	Design Limit $T_{min}, T_{max}$	Sub Group 1	Sub Group 2,3	Sub Group 4	Test Condition <sup>1</sup>	Units
Resolution	RES	-1, 2, 3	12					Bits
Relative Accuracy	RA	-1	1	1	1			± LSB max
		-2, 3	1/2	1	1/2	1/2		
Differential Nonlinearity	DNL	-1	2	2	2		Monotonic to 11 Bit from $T_{min}$ to $T_{max}$	± LSB max
		-2, 3	1	2	1	1	Monotonic to 12 Bit from $T_{min}$ to $T_{max}$	
Gain Error <sup>2</sup>	AE	-1, 2	14.5	12.3	14.5			± LSB max
		-3	2	12.3	2	1		
Gain Tempo	TC <sub>AE</sub>	-1, 2, 3	5					± ppm/°C max
Supply Rejection ( $\Delta$ Gain/ $\Delta$ V <sub>DD</sub> )	PSRR	-1, 2, 3	0.01	0.005	0.01		$\Delta$ V <sub>DD</sub> = ± 5%	± % per % max
Output Leakage Current I <sub>OUT1</sub> (Pin 4) I <sub>OUT2</sub> (Pin 5)	I <sub>OUT1</sub> I <sub>OUT2</sub>	-1, 2, 3	200	± 10	200		DAC Registers Loads with All 0's	± nA max
		-1, 2, 3	200	± 10	200		DAC Register Loads with All 1's	
Output Current Settling Time	t <sub>SI</sub>	-1, 2, 3	2				To ± 1/2LSB R <sub>OUT1</sub> = 100Ω, C <sub>OUT1</sub> = 13pF DAC. Output Measured from Falling Edge of LD1 and LD2.	μs max
Feedthrough Error <sup>3</sup>	FTE	-1, 2, 3	2.5				V <sub>REF</sub> = 10V, 10kHz Sinewave	mV p-p max
Reference Input Resistance (Pin 15)	R <sub>IN</sub>	-1, 2, 3	8	8	8			kΩ min
			25	25	25			kΩ max
Digital Input High Voltage	V <sub>IH</sub>	-1, 2, 3	3.0	3.0	3.0			V min
Digital Input Low Voltage	V <sub>IL</sub>	-1, 2, 3	0.8	0.8	0.8			V max
Digital Input Leakage Current	I <sub>IN</sub>	-1, 2, 3	1	1	1		V <sub>IN</sub> = 0V or V <sub>DD</sub>	± μA max
Digital Input Capacitance	C <sub>IN</sub>	-1, 2, 3	8					pF max
Output Capacitance C <sub>OUT1</sub> (Pin 1) C <sub>OUT2</sub> (Pin 2) C <sub>OUT1</sub> (Pin 1) C <sub>OUT2</sub> (Pin 2)	C <sub>OUT1</sub> C <sub>OUT2</sub> C <sub>OUT1</sub> C <sub>OUT2</sub>	-1, 2, 3	260				Digital Inputs = V <sub>IH</sub> . DAC Register Loaded with 1111 1111 1111	pF max
			75				Digital Inputs = V <sub>IH</sub> . DAC Register Loaded with 1111 1111 1111	pF max
			75				Digital Inputs = V <sub>IL</sub> . DAC Register Loaded with 0000 0000 0000	pF max
			260				Digital Inputs = V <sub>IL</sub> . DAC Register Loaded with 0000 0000 0000	pF max
Serial Input to Strobe Setup Time <sup>4</sup>	t <sub>DS1</sub> t <sub>DS4</sub> t <sub>DS3</sub> t <sub>DS2</sub>	-1, 2, 3	100				STB1 Used as a Strobe	ns min
			0				STB4 Used as a Strobe	
			0				STB3 Used as a Strobe	
			40				STB2 Used as a Strobe	
Serial Input to Strobe Hold Time <sup>4</sup>	t <sub>DH1</sub> t <sub>DH4</sub> t <sub>DH3</sub> t <sub>DH2</sub> t <sub>SR1</sub> t <sub>STB1</sub> t <sub>STB4</sub> t <sub>STB3</sub> t <sub>STB2</sub> t <sub>LD1</sub> t <sub>LD2</sub> t <sub>ASB</sub> t <sub>CLR</sub>	-1, 2, 3	70				STB1 Used as a Strobe	ns min
			250				STB4 Used as a Strobe	
			250				STB3 Used as a Strobe	
			200				STB2 Used as a Strobe	
			160				SR1 Data Pulse Width <sup>4</sup>	
			160				STB1 Pulse Width <sup>4</sup>	
			230				STB4 Pulse Width <sup>4</sup>	
			230				STB3 Pulse Width <sup>4</sup>	
			180				STB2 Pulse Width <sup>4</sup>	
			300				Min Time Between Strobing LSB into Register A and Loading Register B <sup>4</sup>	
			300				Min Time Between Strobing LSB into Register A and Loading Register B <sup>4</sup>	
			80				Min Time Between Strobing LSB into Register A and Loading Register B <sup>4</sup>	
			400				CLK Pulse Width <sup>4</sup>	

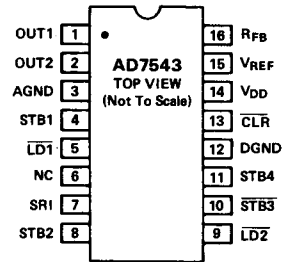
**NOTES**

- <sup>1</sup>V<sub>DD</sub> = +5V; V<sub>OUT1</sub> = V<sub>OUT2</sub> = 0V, V<sub>REF</sub> = +10V unless otherwise stated.
- <sup>2</sup>Measured using internal feedback resistor and includes the effect of 5ppm max gain TC.
- <sup>3</sup>Feedthrough can be further reduced by connecting the metal lid to ground.
- <sup>4</sup>Timing per Figure 1.

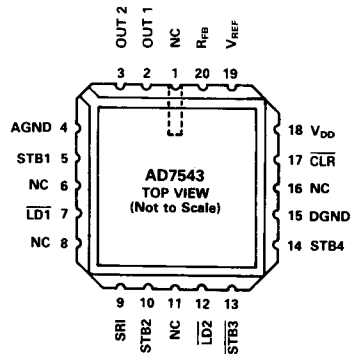
## 3.2.1 Functional Block Diagram and Terminal Assignments.



### DIP (Q) Package



### LCC (E) Package

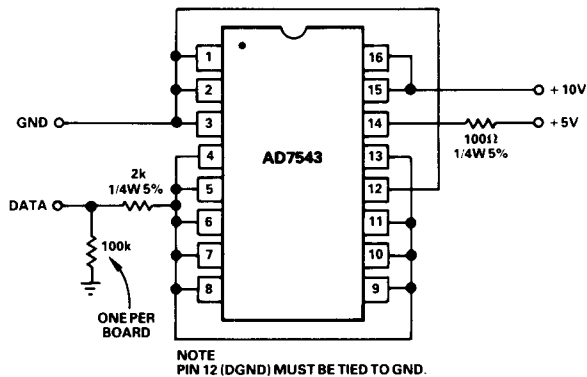


## 3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

## 4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



# AD7543

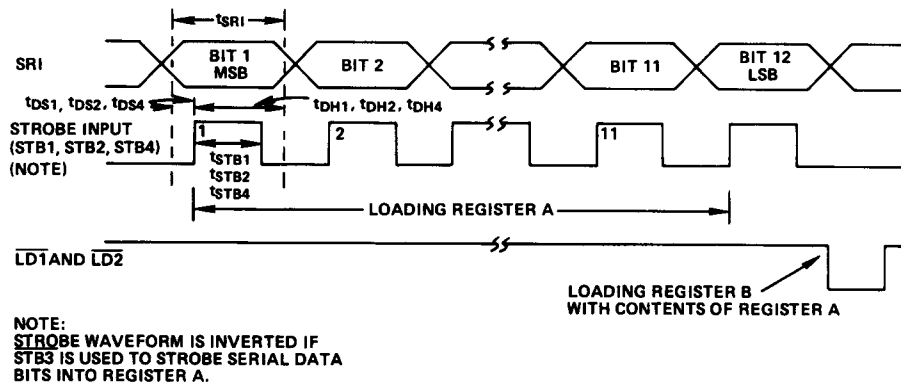


Figure 1. Timing Diagram

Table 2. Truth Table

AD7543 Logic Inputs							AD7543 Operation	Notes
Register A Control Inputs				Register B Control Inputs				
STB4	STB3	STB2	STB1	CLR	LD2	LD1		
0	1	0	1	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
0	1	1	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
0	1	0	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
1	1	0	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
1	X	X	X				No Operation (Register A)	3
X	0	X	X					
X	X	1	X					
X	X	X	1					
				0	X	X	Clear Register B To Code 0000 0000 0000 (Asynchronous Operation)	1,3
				1	1	X	No Operation (Register B)	3
				1	X	1	No Operation (Register B)	3
				1	0	0	Load Register B With The Contents Of Register A	3

NOTES:

- CLR = 0 Asynchronously resets Register B to 0000 0000 0000, but has no effect on Register A.
- Serial data is loaded into Register A MSB first, on edges shown. 1 is positive edge, 0 is negative edge.
- 0 = Logic LOW, 1 = Logic HIGH, X = Don't Care.