### 1.1 Scope.

This specification covers the detail requirements for a precision, ultrahigh speed, current/voltage output 12-bit resolution D/A converter with internal high stability buried Zener reference.

### 1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

| Device | Part Number |
|---|---|
| -1 | AD568SQ/883B |
| -2 | AD568SE/883B |

### 1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

| Device | Package | Description |
|---|---|---|
| -1 | Q-24 | 24-Pin DIP |
| -2 | E-28A | 28-Pin LCC |

### 1.3 Absolute Maximum Ratings. ($T_A$ = +25°C unless otherwise noted)

| | |
|---|---|
| $V_{CC}$ to RefCOM | 0V to +18V |
| $V_{EE}$ to RefCOM | 0V to −18V |
| RefCOM to LCOM | +100mV to −10V |
| ACOM to LCOM | ±100mV |
| THCOM to LCOM | ±500mV |
| SPANs to LCOM | ±12V |
| $I_{BPO}$ to LCOM | ±5V |
| $I_{OUT}$ to LCOM | −5V to $V_{TH}$ |
| Digital Inputs to THCOM | −500mV to +7V |
| Voltage Across Span Resistors | 12V |
| $V_{TH}$ to THCOM | −0.7V to +1.4V |
| Logic Threshold Control Input Current | 5mA |
| Power Dissipation | 1000mW |
| Storage Temperature Range Q (Cerdip) Package | −65°C to +150°C |
| Junction Temperature | 175°C |
| Lead Temperature (Soldering, 10secs) | +300°C |

### 1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC}$ = 25°C/W for Q-24
$\theta_{JA}$ = 75°C/W for Q-24
$\theta_{JC}$ = 42°C/W for E-28A
$\theta_{JA}$ = 125°C/W for E-28A

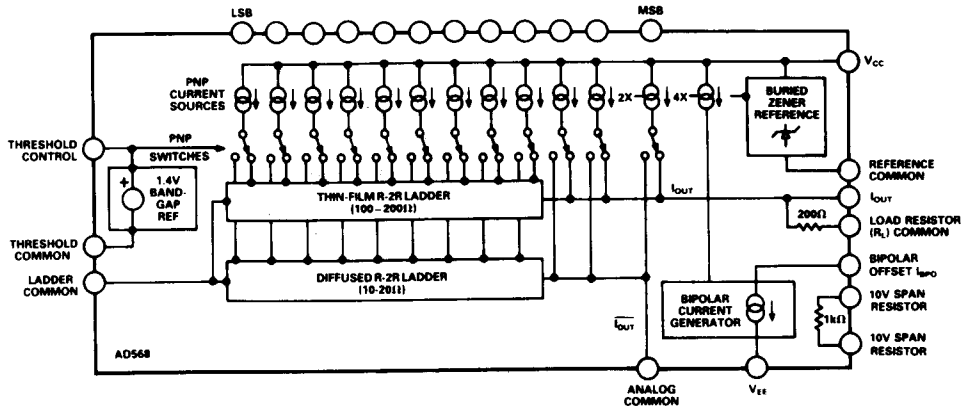
# AD568—SPECIFICATIONS

Table 1.

| Test | Symbol | Device | Design Limit @ +25°C | Sub Group 1 | Sub Group 2, 3 | Test Condition[1] | Units |
|---|---|---|---|---|---|---|---|
| Relative Accuracy[2] | RA | −1 | 1/2 | 1/2 | 3/4 | All Bits with Positive Errors On, All Bits with Negative Errors On | ± LSB max |
| | | −2 | 1/2 | 1/2 | 1 | | |
| Differential Nonlinearity[2] | DNL | −1, 2 | 1 | 1 | 1 | Major Carry Errors | ± LSB max |
| Gain Error[2] | $A_E$ | −1, 2 | 1.0 | 1.0 | | All Bits On | ± % FSR max |
| Gain Temperature Coefficient | $TCA_E$ | −1 | 50 | | 50 | All Bits On, $V_{OUT}$ Mode | ± ppm/°C max |
| | | −2 | 60 | | 60 | | |
| | | −1, 2 | 150 | | 150 | All Bits On, $I_{OUT}$ Mode | |
| Unipolar Offset Error[2] | $V_{OS}$ | −1, 2 | 0.20 | 0.20 | | All Bits Off | ± % FSR max |
| Unipolar Offset TC[3] | $TCV_{OS}$ | −1, 2 | 5 | | 5 | All Bits Off | ± ppm/°C max |
| Bipolar Offset Error[2] | $B_{POE}$ | −1, 2 | 1.0 | 1.0 | | All Bits Off, Bipolar | ± % FSR max |
| Bipolar Offset TC[3] | $TCB_{POE}$ | −1 | 30 | | 30 | All Bits Off, BIP | ± ppm/°C max |
| | | −2 | 40 | | 40 | | |
| Bipolar Zero Error[2] | $B_{PZE}$ | −1, 2 | 0.20 | 0.20 | | MSB On, All Other Bits Off, Bipolar | ± % FSR max |
| Bipolar Zero TC[3] | $TCB_{PZE}$ | −1, 2 | 15 | | 15 | MSB On, All Other Bits Off, Bipolar | ± ppm/°C max |
| Output Resistance | $R_{OUT}$ | −1, 2 | 160 | | | | Ω min |
| | | | 240 | | | | Ω max |
| Voltage Settling Time | $t_{SV}$ | −1, 2 | 50 | | | | ns typ to 0.025% |
| Current Settling Time | $t_{SI}$ | −1, 2 | 35 | | | | ns typ to 0.025% |
| Full-Scale Transition | $t_{FS}$ | −1, 2 | 11 | | | 10% to 90% Reset Time 90% to 10% Fall Time | ns typ |
| Glitch Impulse | GI | −1, 2 | 350 | | | | pV-sec typ |
| Compliance Voltage | CV | −1, 2 | 2 | | | | − V min |
| | | | 1.2 | | | | + V max |
| Output Current | $I_{OUT}$ | −1, 2 | | 10.137<br>10.343 | | Unipolar<br>All Bits On | + mA min<br>+ mA max |
| | | | | 5.017<br>5.223 | | Bipolar<br>All Bits On | + mA min<br>+ mA max |
| Power Supply Rejection Ratio | PSRR | −1, 2 | 0.05 | 0.05 | | $V_{CC}$ = + 13.5V to + 16.5V<br>$V_{EE}$ = − 13.5V to − 16.5V | ± % FS/V max |
| Power Supply Current[4, 5] | $I_{CC}$ | −1, 2 | 32 | 32 | | All Bits High | + mA max |
| | $I_{EE}$ | −1, 2 | 8 | 8 | | | − mA max |
| Power Consumption | $P_C$ | −1, 2 | 625 | | | | mW max |
| Digital Input High Voltage | $V_{IH}$ | −1, 2 | 2.0 | 2.0 | 2.0 | | + V min |
| Digital Input Low Voltage | $V_{IL}$ | −1, 2 | 0.8 | 0.8 | 0.8 | | + V max |
| Digital Input High Current | $I_{IH}$ | −1, 2 | 10 | 10 | 10 | $V_{IH}$ = 2V | ± μA max |
| Digital Input Low Current | $I_{IL}$ | −1, 2 | 0.5 | 0.5 | 0.5 | $V_{IL}$ = 0.0V | − μA min |
| | | | 100 | 100 | 200 | | − μA max |

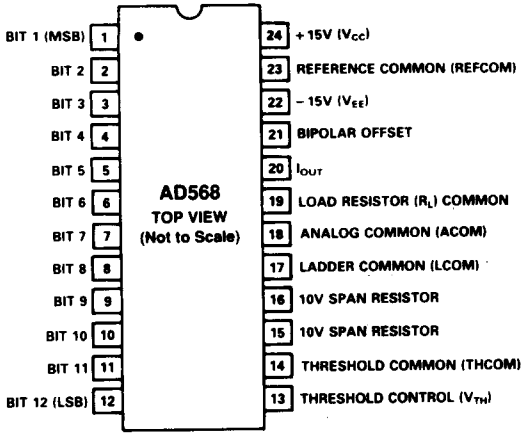
NOTES
[1]$V_{CC}$ = + 15V, $V_{EE}$ = − 15V, $V_{IH}$ = 2.0V, $V_{IL}$ = 0.8V, $T_A$ = + 25°C unless otherwise specified.
$V_{IH}$ = + 2.0V and $V_{IL}$ = 0.8V guaranteed design limits at − 55°C and + 125°C.
[2]Measured in $I_{OUT}$ mode.
[3]Measured in $V_{OUT}$ mode.
[4]Guaranteed for + 13.5≤$V_{CC}$≤ + 16.5V.
[5]Guaranteed for − 13.5≤$V_{EE}$≤ − 16.5V.

### 3.2.1 Functional Block Diagram and Terminal Assignments.

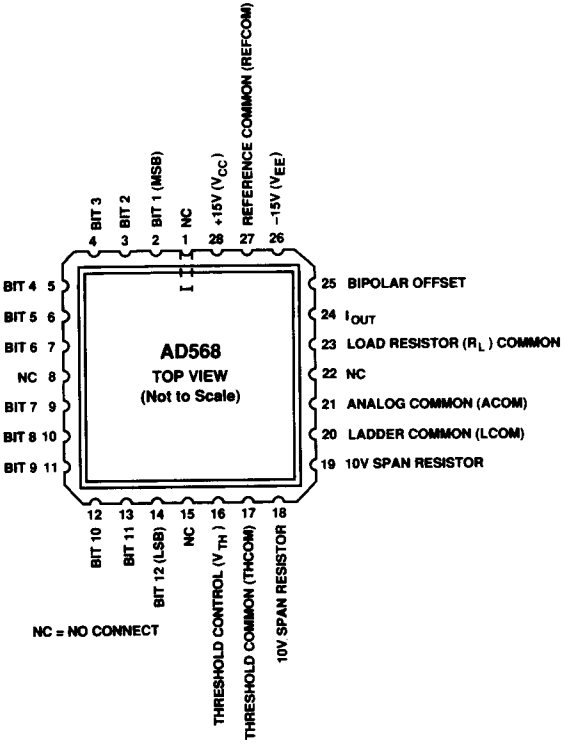





**24-Lead "Skinny" Cerdip Package**




**28-Lead LCC Package**




### 3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (56).

### 4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).