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## MAX22007

# Four-Channel 12-Bit Configurable Analog Output with Integrated Voltage Reference

### General Description

The MAX22007 is a software-configurable four-channel analog output device that drives a voltage or current output on each channel. All outputs are protected to  $\pm 42V_{P-P}$  for high-voltage supply of  $HVDD = 8V$  to  $20V$  and  $HVSS = -2V$  to  $0V$ .

Each output channel of the MAX22007 features a 12-bit DAC with fast settling time using a shared internal voltage reference. The device offers low-offset, high-voltage amplifiers to condition the signal from low-voltage DAC outputs to high-voltage or current outputs. If one output is miswired, all other outputs remain unaffected and function normally. For each channel, an internal comparator can be used to determine the load impedance and allows the microcontroller to intelligently select for voltage or current output mode. All outputs are kept safe by integrated current protection for functional and thermal robustness. The MAX22007 also includes a thermal shutdown circuit that protects the device when the junction temperature exceeds  $165^{\circ}C$  (typ).

The MAX22007 communicates with a microcontroller using a SPI interface at clock rates up to  $30MHz$  with an optional eight-bit CRC for improved data integrity. Eight GPIOs can be used to interface and control other resources in the application circuit. The MAX22007 operates from a  $2.7V$  to  $5.5V$   $V_{DD}$  low-voltage supply and an  $8V$  to  $24V$   $HVDD$  positive high-voltage supply. The negative voltage supply  $HVSS$  can be set between  $-2V$  and  $0V$ .

The MAX22007 is available in an  $8mm \times 8mm$  56-pin TQFN package and operates over the  $-40^{\circ}C$  to  $+85^{\circ}C$  temperature range with  $2.5kV$  HBM ESD protection on all pins.

### Applications

- Building Automation Analog Outputs
- Configurable Analog Output Cards
- Factory Automation Analog Outputs
- Process Automation
- Programmable Logic Controllers

### Benefits and Features

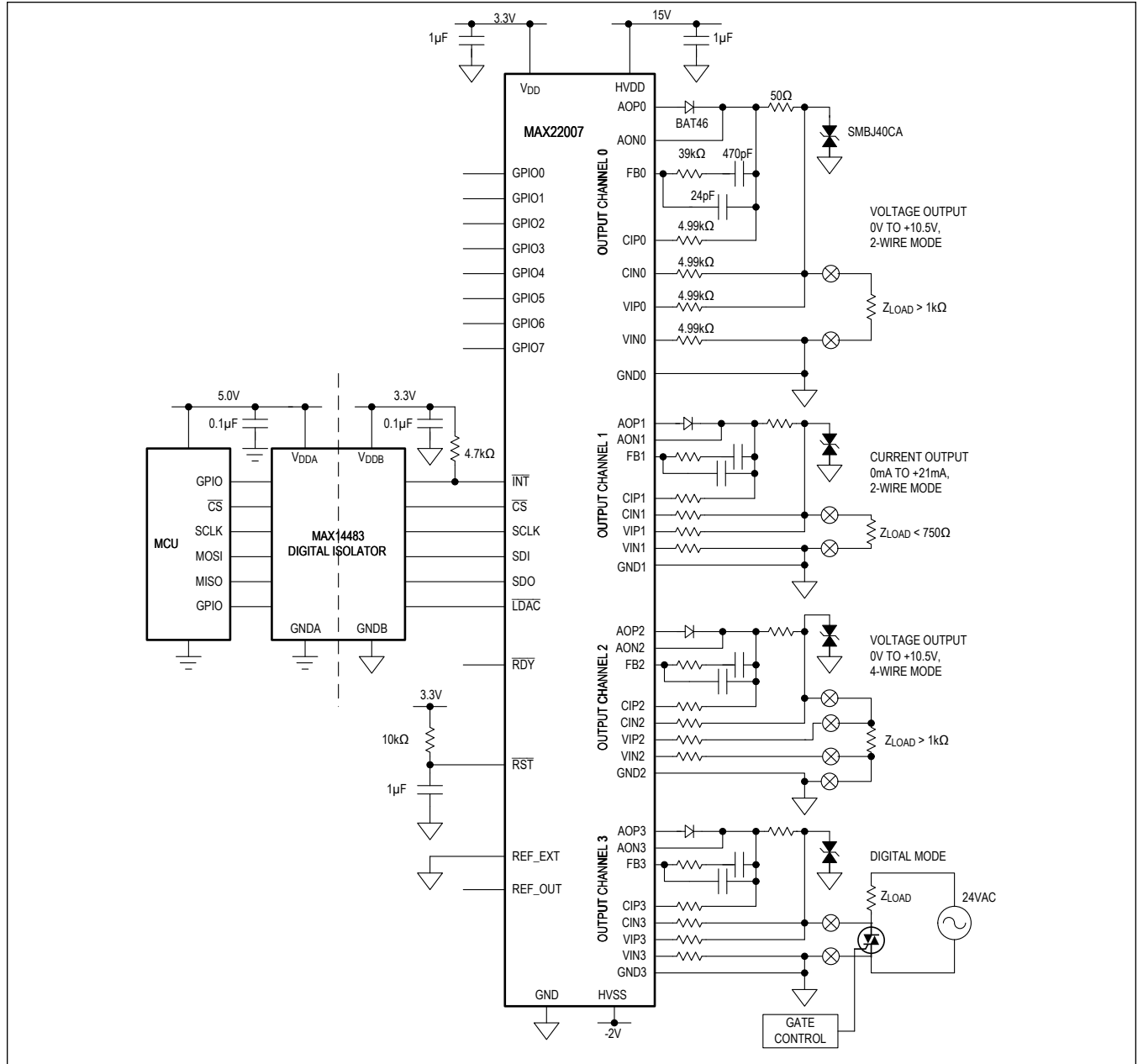
- Configurable Outputs
  - Each Output Individually Configurable
  - Internal Comparator to Allow Calculating Load Impedance for Voltage-Mode or Current-Mode
  - Voltage Mode is  $0V$  to  $10.5V$  Linear Range with  $12.5V$  Overrange for Loads from  $1k\Omega$  to  $1M\Omega$
  - Current Mode is  $0mA$  to  $21mA$  Linear Range with  $25mA$  Overrange for Loads from  $0\Omega$  to  $750\Omega$
- System Accuracy
  - V/I Output Resolution is 12-Bits
  - Factory Calibrated for Gain and Offset Error within  $\pm 0.2\%$  at  $+25^{\circ}C$
  - V/I Total Unadjusted Error Less Than  $\pm 1\%$  from  $-40^{\circ}C$  to  $+85^{\circ}C$
- Robust with Integrated Diagnostics
  - $\pm 42V_{P-P}$  Protection for Output Drivers
  - $\pm 1kV$  Surge Protection with  $4.99k\Omega$  Series Resistors at Input Pins
  - $\pm 2.5kV$  HBM ESD Protection on All Pins
  - Outputs have Short-Circuit and Overvoltage Protection with External Diodes
  - Thermal Monitoring and Shutdown Protection
- Simple and Low-Cost Interface
  - Up to  $30MHz$  SPI Serial Interface with Optional 8-Bit CRC
  - Daisy-Chain Mode to Reduce System Cost
  - $V_{DD} = 2.7V$  to  $5.5V$  for Easy Interface to the Microcontroller
  - High Voltage Output Supplies:
    - $HVDD: +8V$  to  $+24V$
    - $HVSS: -2V$  to  $0V$
- Robust Performance in a Compact Package
  - $-40^{\circ}C$  to  $85^{\circ}C$  Operating Temperature Range
  - 56-pin TQFN,  $8mm \times 8mm$

[Ordering Information and Typical Application Circuits](#) appear at the end of the datasheet.

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Quad Configurable Analog Output



**Absolute Maximum Ratings**

V <sub>DD</sub> to GND.....	-0.3V to +6V	AON <sub>-</sub> to HVSS .....	-70V to +70V
V <sub>DD</sub> to HVSS.....	-0.3V to +6V	INT, CS, SCLK, SDI to GND .....	-0.3V to +6V
GND <sub>-</sub> to GND.....	-0.3V to +0.3V	All Other Pins to GND .....	-0.3V to min(+6V, (V <sub>DD</sub> + 0.3V))
HVDD to HVSS .....	-0.3V to +40V	Maximum Current into AOP <sub>-</sub> , AON <sub>-</sub> .....	±100mA
HVDD to AON <sub>-</sub> .....	-70V to +70V	Maximum Current into Any Other Pin .....	±50mA
HVDD to GND .....	-0.3V to +40V	Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
HVDD to GND <sub>-</sub> .....	-0.3V to +40V	56-TQFN (derate 47.6mW/°C above +70°C) .....	3809.5mW
GND to HVSS.....	-0.3V to +6V	Operating Temperature Range .....	-40°C to +85°C
GND <sub>-</sub> to HVSS.....	-0.3V to +6V	Junction Temperature .....	+150°C
AOP <sub>-</sub> to HVDD.....	-70V to +0.3V	Storage Temperature Range .....	-65°C to +150°C
FB <sub>-</sub> , CIP <sub>-</sub> , CIN <sub>-</sub> , VIP <sub>-</sub> , VIN <sub>-</sub> to HVSS .....	-0.3V to min(+40V, ((V <sub>HVDD</sub> - V <sub>HVSS</sub> ) + 0.3V))	Lead Temperature (soldering, 10s).....	+300°C
CIP <sub>-</sub> , CIN <sub>-</sub> , VIP <sub>-</sub> , VIN <sub>-</sub> to HVSS (with 4.99kΩ series resistors).....	-42V to +42V	Soldering Temperature (reflow) .....	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Package Information**

**56-PIN TQFN**

Package Code	T5688+4C
Outline Number	<a href="#">21-0135</a>
Land Pattern Number	<a href="#">90-0047</a>
<b>Thermal Resistance, Four-Layer Board:</b>	
Junction to Ambient (θ <sub>JA</sub> )	21°C/W
Junction to Case (θ <sub>JC</sub> )	1°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

**Electrical Characteristics**

(V<sub>DD</sub> = 3.3V, V<sub>HVDD</sub> = +15V, V<sub>HVSS</sub> = 0V, Internal Reference, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>ANALOG OUTPUT-VOLTAGE MODE</b>						
Output-Voltage Range	V <sub>OUT</sub>	DAC full-scale range (Note 2)	0 to 12.5			V
		Linear range, V <sub>HVSS</sub> = 0V (Notes 2, 3)	0.3		10.5	
		Linear Range, V <sub>HVSS</sub> = -2V (Notes 2, 3)	0.02		10.5	
Dropout Voltage		V <sub>OUT</sub> = 12.5V, sourcing 25mA, measured between HVDD and AOP <sub>-</sub> , gain compression < 1%			1.0	V
Output-Current Protection		Output shorted to HVDD or HVSS, threshold current (Note 4)		50		mA
		Output shorted to HVDD or HVSS, average current (Note 4)		7		

**Electrical Characteristics (continued)**

( $V_{DD} = 3.3V$ ,  $V_{HVDD} = +15V$ ,  $V_{HVSS} = 0V$ , Internal Reference,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ ) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AOP_ and AON_ High-Impedance Leakage Current		$V_{OUT} = 0V$ to $+10.5V$		±25		μA
Offset Error	$V_{OFF}$	$T_A = +25^{\circ}C$ , no load, extrapolated from the linear range (Note 5)			±10	mV
Offset Drift		$T_A = -40^{\circ}C$ to $85^{\circ}C$ (Note 6)		±10		μV/°C
Gain Error		$T_A = +25^{\circ}C$ , no load (Note 5)			±0.2	%
Gain Drift		$T_A = -40^{\circ}C$ to $85^{\circ}C$ (Note 6)		±10		ppm/°C
INL Error	INL	$T_A = +25^{\circ}C$ , no load (Note 5)	-1	±0.5	+1	LSB
INL Drift		$T_A = -40^{\circ}C$ to $85^{\circ}C$ (Note 6)		±1		μV/°C
Output Noise	$V_n$	10kHz BW		100		μV <sub>RMS</sub>
Voltage Output Total Unadjusted Error	$V_{TUE}$	$V_{OUT} = 0.02V$ to $10.5V$ , no load (Notes 5, 7)			±100	mV
Voltage Crosstalk	$V_{CT}$	Channel under test is in voltage mode with $V_{OUT} = 10.5V$ , $I_{OUT} = 10mA$ . All other channels are in current mode forcing 0mA and 20mA to a 0Ω load. The crosstalk is the voltage variation of the channel under test. (Note 6)			25	mV
Supply Rejection Ratio	PSRR	DC, $V_{OUT} = 300mV$ , $V_{HVDD} = +8V$ to $+24V$		100		dB
Load Regulation		$0 \leq I_{LOAD} \leq +10.5mA$ , measured at $V_{OUT} = +10.5V$ , output change due to self-heating excluded		±0.1		mV
VIP_ and VIN_ Input-Voltage Range		(Note 3)	$V_{HVSS}$		$V_{HVDD} - 2.5$	V
VIP_ and VIN_ Input Current		$V_{VIP\_}$ , $V_{VIN\_} = 20mV$ to $10.5V$		±2		μA
Settling Time		Resistive load from 1kΩ to 10MΩ; settling to 1% of step size for $V_{OUT} = 20mV$ to $10.5V$		0.3		ms
		Capacitive load up to 1μF; settling to 1% of step size for $V_{OUT} = 20mV$ to $10.5V$		1		
<b>ANALOG OUTPUT-CURRENT MODE</b>						
Output-Current Range	$I_{OUT}$	$R_{SENSE} = 50\Omega$ , DAC full-scale range (Note 8)		0 to 25		mA
		Linear range, $V_{HVSS} = 0V$ (Notes 3, 8)	1.5	21		
		Linear range, $V_{HVSS} = -2V$ (Notes 3, 8)	0.04	21		
Dropout Voltage		$V_{HVDD} = 12V$ , Sourcing 25mA, measured between HVDD and AOP_, gain compression < 1%			0.85	V
Offset Error	$I_{OFF}$	$T_A = +25^{\circ}C$ , $R_{LOAD} = 250\Omega$ , extrapolated from the linear range (Note 5)			±20	μA

**Electrical Characteristics (continued)**

( $V_{DD} = 3.3V$ ,  $V_{HVDD} = +15V$ ,  $V_{HVSS} = 0V$ , Internal Reference,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ ) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Offset Drift		$T_A = -40^{\circ}C$ to $85^{\circ}C$ (Note 6)		$\pm 20$		nA/ $^{\circ}C$
Gain Error		$T_A = +25^{\circ}C$ , $R_{LOAD} = 250\Omega$ (Note 5)			$\pm 0.2$	%
Gain Drift		$T_A = -40^{\circ}C$ to $85^{\circ}C$ (Note 6)		$\pm 10$		ppm/ $^{\circ}C$
INL Error	INL	$T_A = +25^{\circ}C$ , $R_{LOAD} = 250\Omega$ (Note 5)	-1	+0.5	+1	LSB
INL Drift		$T_A = -40^{\circ}C$ to $85^{\circ}C$ (Note 6)		$\pm 5$		nA/ $^{\circ}C$
Output Noise	$I_n$	10kHz BW		0.5		$\mu A_{RMS}$
Current Output Total Unadjusted Error	$I_{TUE}$	$I_{OUT} = 40\mu A$ to $21mA$ , $R_{LOAD} = 250\Omega$ (Notes 5, 9)			$\pm 200$	$\mu A$
Current Crosstalk	$I_{CT}$	Channel under test is in current mode with $I_{OUT} = 21mA$ , $V_{OUT} = 10V$ . All other channels are in current mode forcing $0mA$ and $20mA$ to a $0\Omega$ load. The crosstalk is the current variation of the channel under test. (Note 6)			50	$\mu A$
Supply Rejection	PSR	DC, $I_{OUT} = 3mA$ , $V_{HVDD} = +8V$ to $+24V$		0.1		$\mu A/V$
CIP_ and CIN_ Input-Voltage Range		(Note 3)	$V_{HVSS}$		$V_{HVDD} - 2.5$	V
CIP_ and CIN_ Input Current		$V_{CIP\_}$ , $V_{CIN\_} = 0V$ to $+12V$		$\pm 2$		$\mu A$
Common-Mode Rejection	CMR	Current mode, $V_{CIN\_} = 0V$ to $+11V$ , measured at $I_{OUT} = 1.5mA$			10	$\mu A/V$
CIP_ to CIN_ Differential-Input Range				1.25		V
CIP_ to CIN_ Differential-Input Impedance				100		k $\Omega$
Settling Time		Resistive load up to $250\Omega$ ; settling to 1% of step size for $I_{OUT} = 40\mu A$ to $21mA$		0.5		ms
		Resistive load up to $500\Omega$ ; settling to 1% of step size for $I_{OUT} = 40\mu A$ to $21mA$		1.0		
		Inductive load up to $1mH$ ; settling to 1% of step size for $I_{OUT} = 40\mu A$ to $21mA$		0.5		
<b>COMPARATOR</b>						
Offset	$V_{OFF}$			$\pm 50$		mV
Delay	$t_{DELAY}$			64		$\mu s$
Nominal Trip Voltage	$V_{TH}$			500		mV
<b>REFERENCE</b>						
REF_OUT Output Voltage	$V_{REF\_OUT}$	$T_A = +25^{\circ}C$	2.494	2.5	2.506	V
Output-Voltage Temperature Coefficient		$T_A = -40^{\circ}C$ to $+85^{\circ}C$ (Note 6)		$\pm 10$	$\pm 25$	ppm/ $^{\circ}C$

**Electrical Characteristics (continued)**

( $V_{DD} = 3.3V$ ,  $V_{HVDD} = +15V$ ,  $V_{HVSS} = 0V$ , Internal Reference,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ ) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DIGITAL INPUTS</b>						
Input Logic-Low Voltage	$V_{IL}$				$0.3 \times V_{DD}$	V
Input Logic-High Voltage	$V_{IH}$		$0.7 \times V_{DD}$			V
Input Hysteresis	$V_{HYS}$			300		mV
Input Leakage Current	$I_{IN}$		-1		+1	$\mu A$
Input Capacitance	$C_{IN}$			10		pF
<b>DIGITAL OUTPUTS</b>						
Output Logic-Low Voltage	$V_{OL}$	$I_{OL} = 4mA$ , sinking			0.4	V
Output Logic-High Voltage (SDO, $\overline{RDY}$ , GPIO7 to GPIO0)	$V_{OH}$	$I_{OH} = 4mA$ , sourcing	$0.9 \times V_{DD}$			V
Three-State Leakage Current			-10		+10	$\mu A$
Three-State Output Capacitance				10		pF
<b>SPI TIMEOUT</b>						
Timeout Interval Accuracy		With respect to nominal value	-50		+50	%
<b>SUPPLIES</b>						
Analog Supply Voltage	$V_{DD}$		2.7	3.3	$V_{HVSS} + 5.5$	V
Positive High-Voltage Supply	$V_{HVDD}$		8		$V_{HVSS} + 24$	V
		$\pm 42V_{P-P}$ output protection (Note 6)	8		20	
Negative High-Voltage Supply	$V_{HVSS}$		-2	0	0	V
Analog Supply Quiescent Current	$I_{DD}$	All channels and comparators powered up		1.5		mA
High-Voltage Quiescent Current	$I_{HV}$	All channels and comparators powered up, no load current		4.5		mA
<b>TIMING CHARACTERISTICS</b>						
SCLK Frequency	$f_{SCLK}$				30	MHz
SCLK Clock Period	$t_{CP}$		33			ns
SCLK Pulse-Width High	$t_{CH}$		13			ns
SCLK Pulse-Width Low	$t_{CL}$	Read transactions must also meet $t_{DOT}$	13			ns
$\overline{CS}$ Fall Setup Time	$t_{CSS0}$	$\overline{CS}$ falling edge to 1st SCLK rising edge setup time	10			ns

**Electrical Characteristics (continued)**

( $V_{DD} = 3.3V$ ,  $V_{HVDD} = +15V$ ,  $V_{HVSS} = 0V$ , Internal Reference,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ ) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Rise Setup Time	$t_{CSS1}$	SCLK rising edge to $\overline{CS}$ rising edge setup time	5			ns
$\overline{CS}$ Fall Hold Time	$t_{CSH0}$	SCLK rising edge to $\overline{CS}$ falling edge hold time	0			ns
$\overline{CS}$ Pulse-Width High	$t_{CSW}$	Minimum $\overline{CS}$ pulse-width high	150			ns
SDI Setup Time	$t_{DS}$	SDI setup time to SCLK rising edge	10			ns
SDI Hold Time	$t_{DH}$	SDI hold time after SCLK rising edge	5			ns
SDO Transition Time	$t_{DOT}$	SDO transition valid after SCLK falling edge			20	ns
SDO Hold Time	$t_{DOH}$	Output remains valid after falling edge of SCLK	3			ns
SDO Disable Time	$t_{DOD}$	Last SCLK falling edge to SDO disable, $C_{LOAD} = 20pF$			25	ns
$\overline{RDY}$ Fall Transition Time	$t_{RT0}$	Last SCLK falling edge to $\overline{RDY}$ falling edge			40	ns
$\overline{RDY}$ Rise Transition Time	$t_{RT1}$	$\overline{CS}$ rise to $\overline{RDY}$ rise			40	ns
<b>THERMAL PROTECTION</b>						
Chip Thermal Shutdown Temperature	$T_{CSDN}$	Temperature rising		165		$^{\circ}C$
Chip Thermal Warning Temperature	$T_{CWARN}$	Temperature rising		145		$^{\circ}C$
Chip Thermal Warning Hysteresis	$T_{HYS}$			10		$^{\circ}C$
<b>EMC PROTECTION</b>						
ESD	$V_{ESD}$	All pins, Human Body Model		$\pm 2.5$		kV
Surge	$V_{SURGE}$	AOP_, AON_, FB_, CIP_, CIN_, VIP_, VIN_ to GND, IEC 61000-4-5 with external 4.99k $\Omega$ series resistors on CIP_, CIN_, VIP_ and VIN_ pins, and a bidirectional TVS on AOP_ and AON_ pins.		$\pm 1$		kV

**Note 1:** Limits are 100% tested at  $T_A = +25^{\circ}C$ , unless otherwise noted. Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization.

**Note 2:** The output voltage is measured at the sense voltage input (VIP\_). The minimum supply voltage required is the sum of the output voltage  $V_{OUT}$ , the voltage across the sense resistor, the diode forward voltage, and the dropout voltage. For a 25mA load current, a +12V output, a 50 $\Omega$  sense resistor, and a diode forward voltage of 550mV (BAT46), the minimum required supply voltage is +14.8V.

**Note 3:** Offset Error, Gain Error, INL Error, and Settling Times are only guaranteed in the linear range. For Analog Output Current Mode Offset Error, Gain Error, INL Error, and Settling Times are only guaranteed in the specified Input Common-Mode Range ( $V_{CIP\_} + V_{CIN\_}$ )/2 of 0V to +12V. Offset Error, Gain Error, and INL Error are measured using the following DAC codes:

- Analog Output Voltage Mode:
  - $V_{HVSS} = 0V$ : code 98 and code 3441
  - $V_{HVSS} = -2V$ : code 6 and code 3441
- Analog Output Current Mode:
  - $V_{HVSS} = 0V$ : code 245 and code 3441
  - $V_{HVSS} = -2V$ : code 6 and code 3441

The minimum and maximum specification of the linear range and input-voltage range are guaranteed through Offset Error, Gain Error, and INL Error.

**Note 4:** The threshold current specifies the typical current that triggers the short-circuit protection. The average current that accounts for self-heating of the device is significantly smaller due to the duty cycle when OVC\_CNFG is set to logic low.

**Note 5:** Measured with only one channel powered up.

**Note 6:** Guaranteed by design and characterization. Not tested in production.

**Note 7:** The Voltage Output Total Unadjusted Error ( $V_{TUE}$ ) does not include errors caused by Voltage Crosstalk and Load Regulation.

**Note 8:** The minimum supply voltage required is the output current times the sum of the load and cable resistors, the voltage across the sense resistor, the diode forward voltage, and the dropout voltage. For a 25mA output current, a load resistor of 500Ω, a cable resistance of 250Ω, a 50Ω sense resistor, and a diode forward voltage of 550mV (BAT46), the minimum required supply voltages is +21.4V.

**Note 9:** The Current Output Total Unadjusted Error ( $I_{TUE}$ ) does not include errors caused by Current Crosstalk and Common-Mode Rejection (if a load resistance other than 250Ω is used).

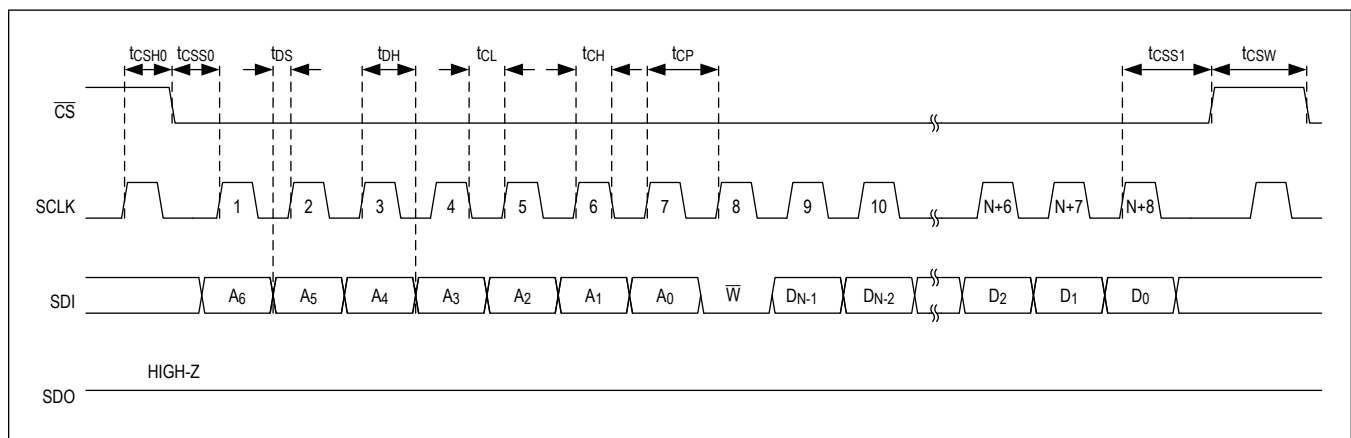


Figure 1. SPI Write Timing ( $N = 16$  when CRC is disabled, and  $N = 24$  when CRC is enabled)



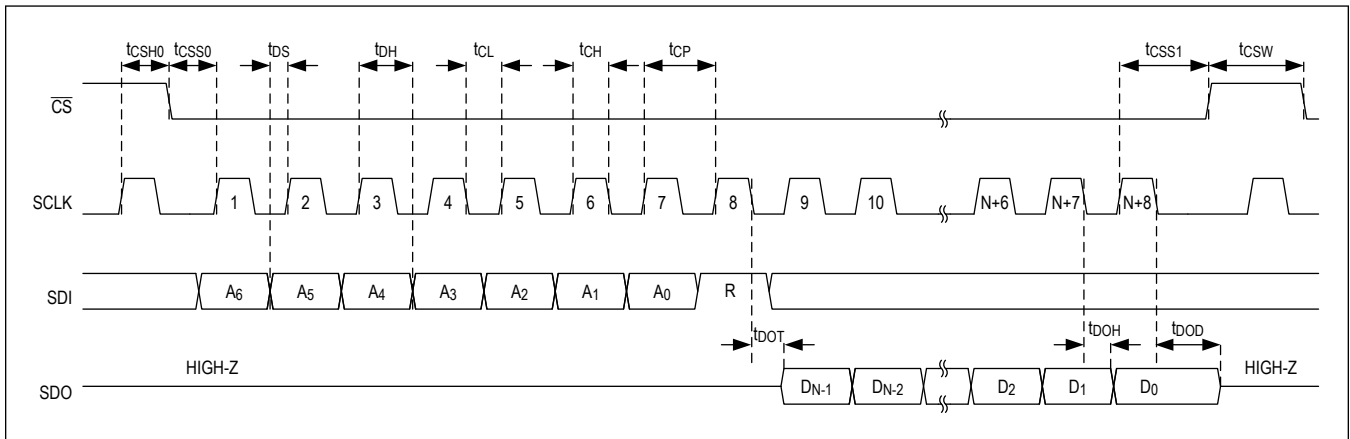


Figure 2. SPI Read Timing ( $N = 16$  when CRC is disabled, and  $N = 24$  when CRC is enabled)

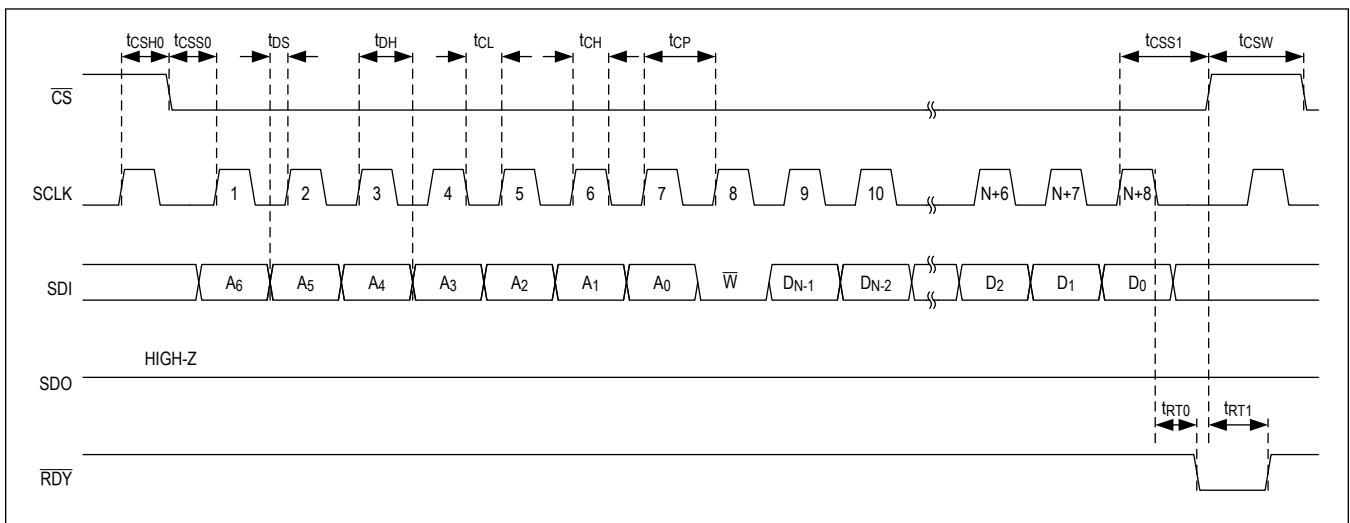
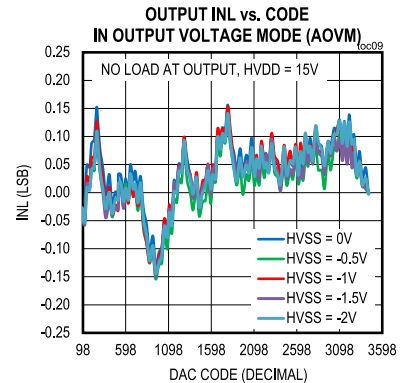
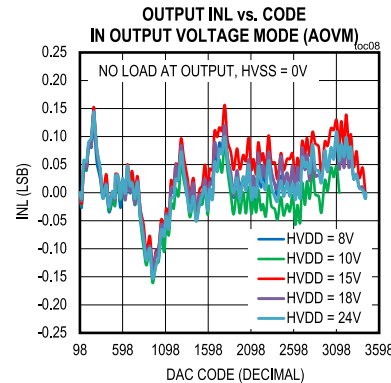
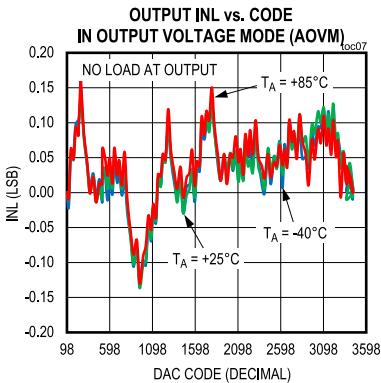
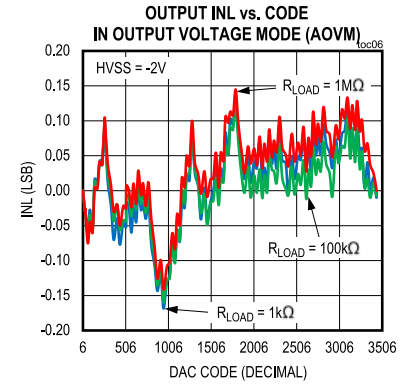
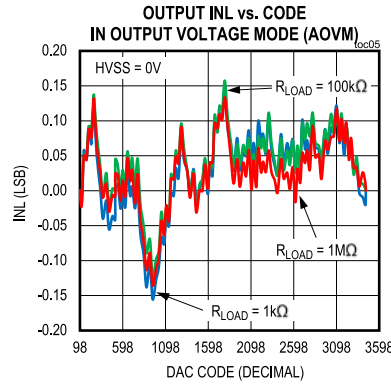
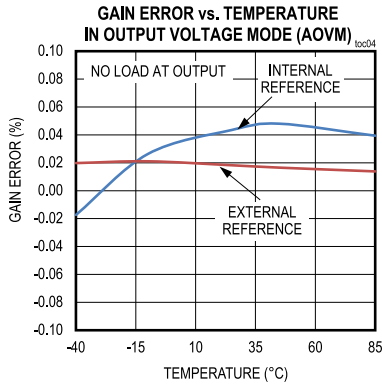
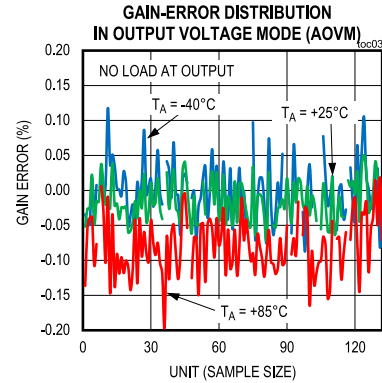
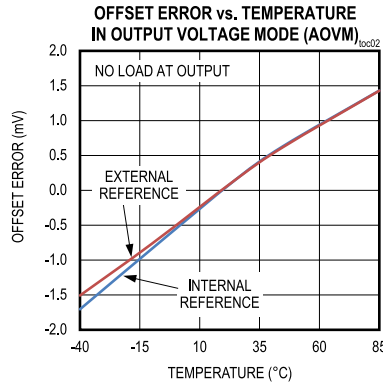
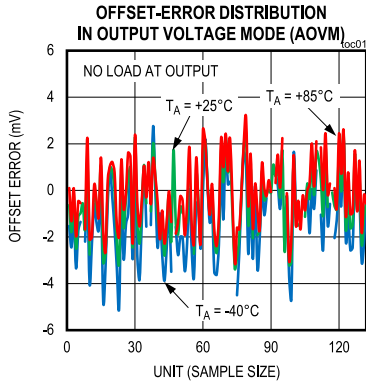


Figure 3. Elongated SPI Write Timing for Daisy-Chain Applications ( $N = 16$  when CRC is disabled, and  $N = 24$  when CRC is enabled)

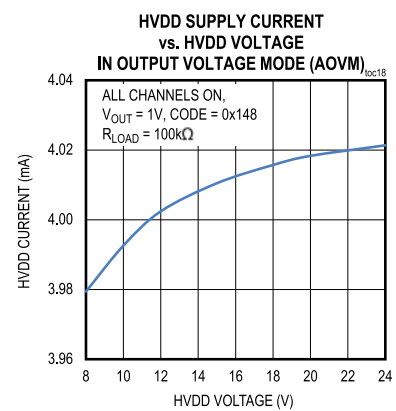
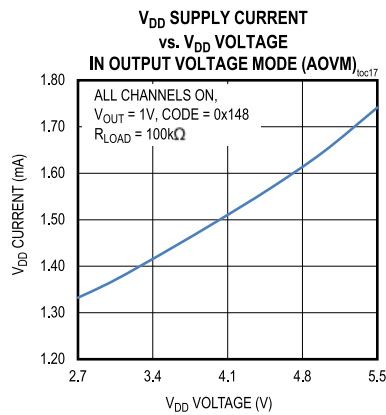
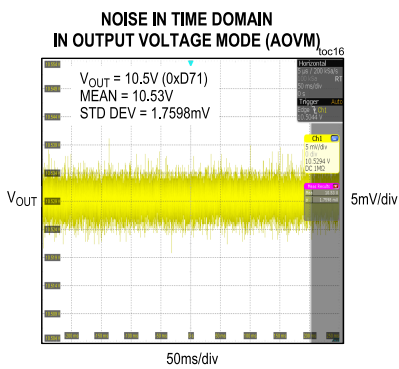
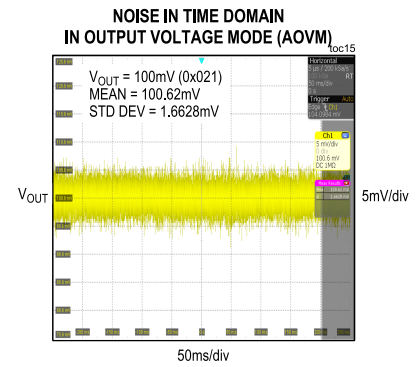
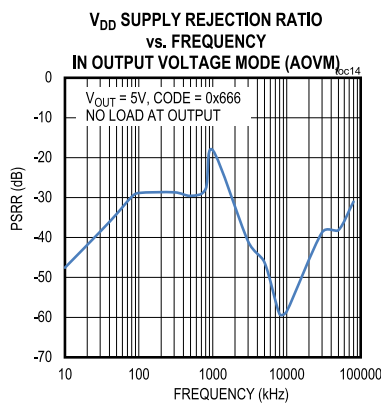
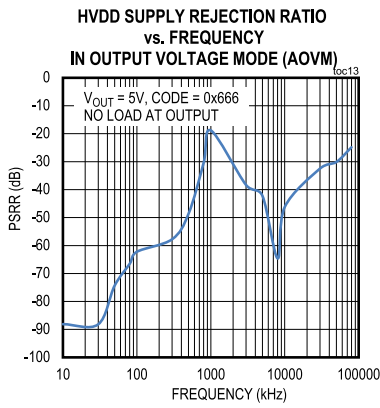
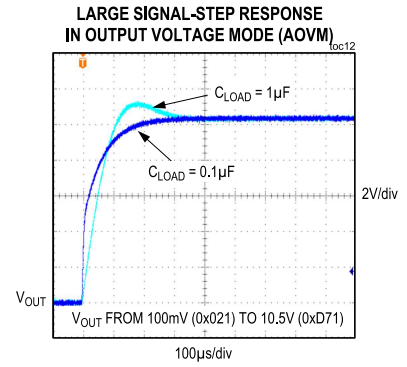
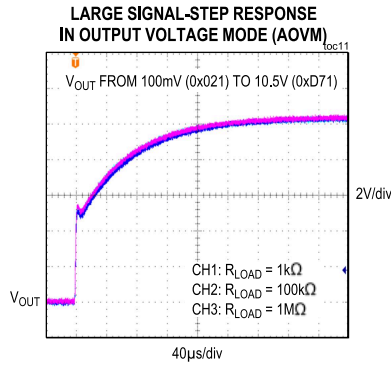
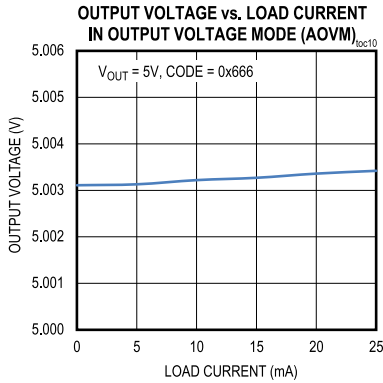
Typical Operating Characteristics

( $V_{DD} = +3.3V$ ,  $V_{HVDD} = +15V$ ,  $V_{HVSS} = 0V$ , Internal Reference,  $T_A = 25^\circ C$ , unless otherwise noted)



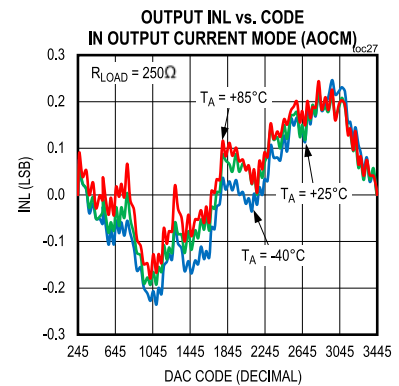
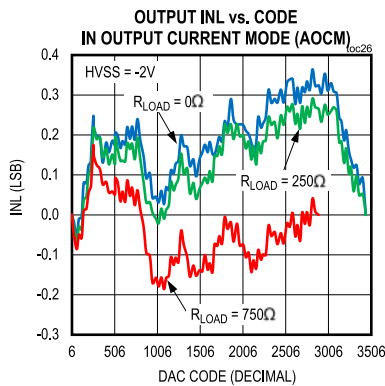
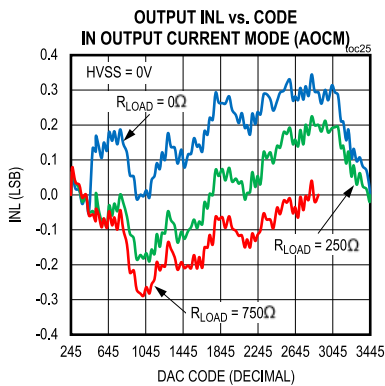
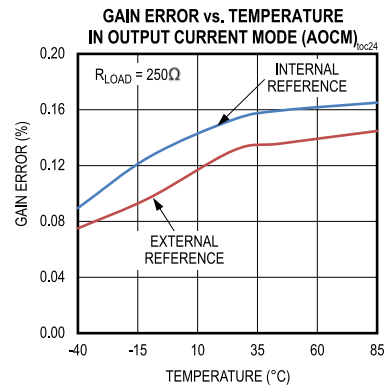
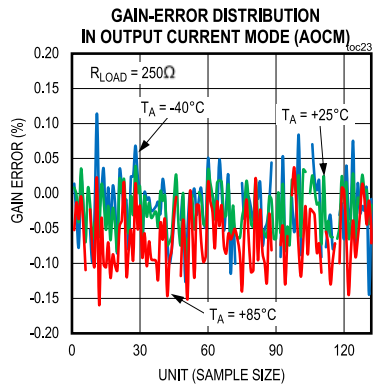
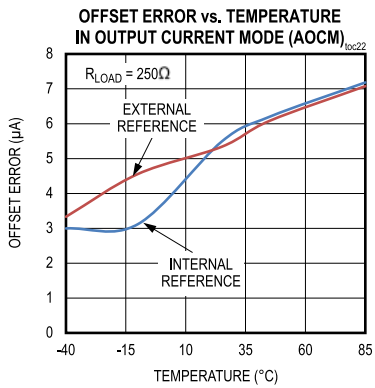
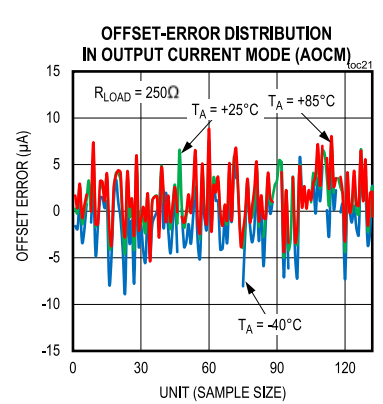
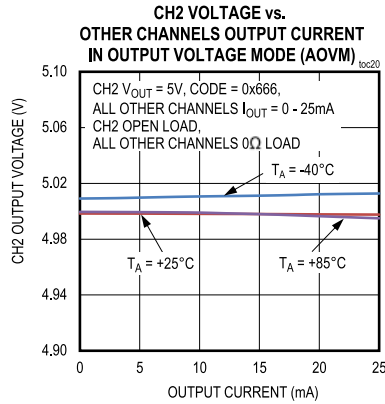
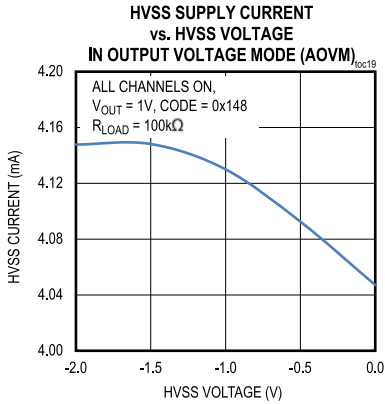
Typical Operating Characteristics (continued)

( $V_{DD} = +3.3V$ ,  $V_{HVDD} = +15V$ ,  $V_{HVSS} = 0V$ , Internal Reference,  $T_A = 25^\circ C$ , unless otherwise noted)



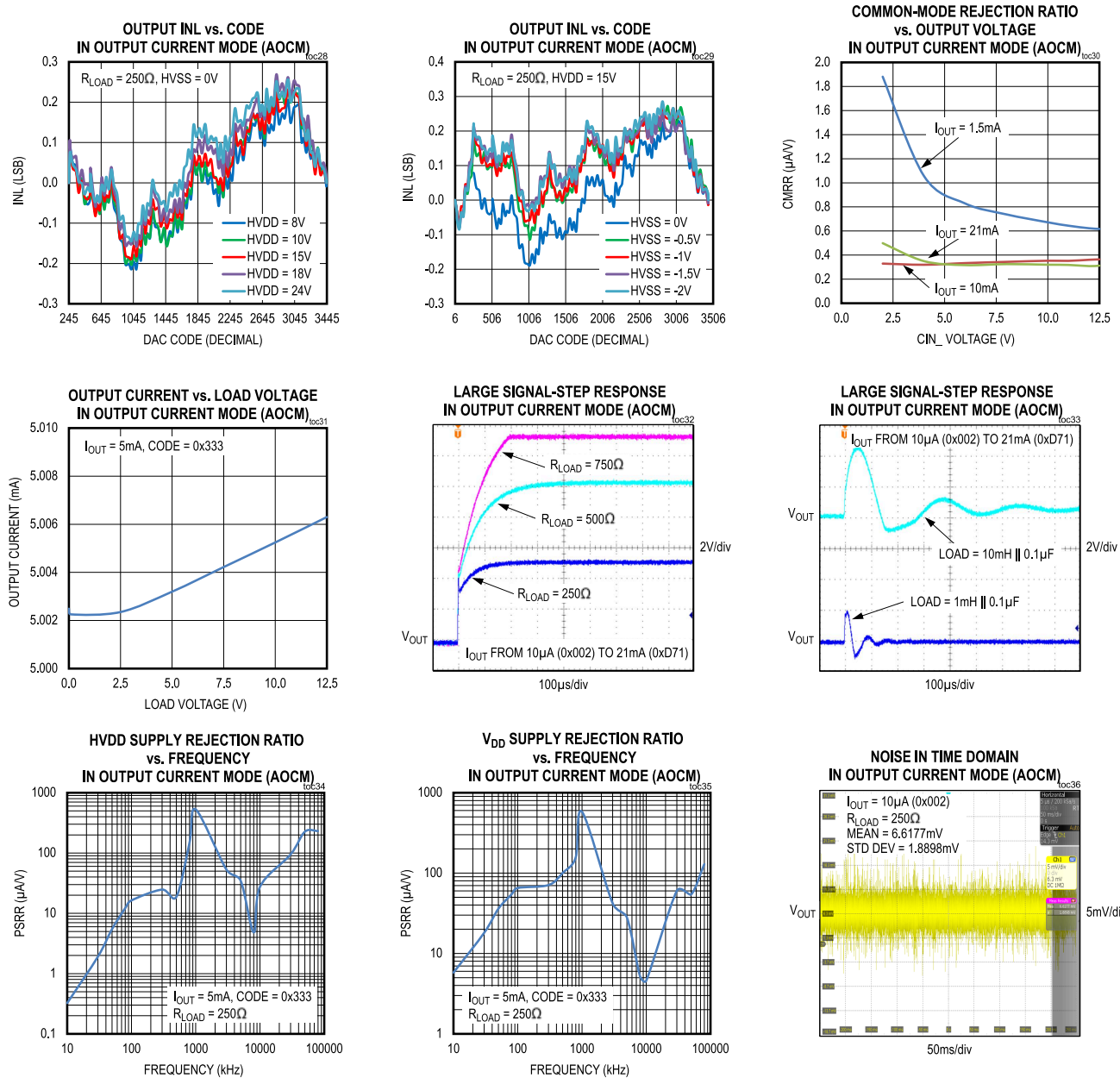
Typical Operating Characteristics (continued)

( $V_{DD} = +3.3V$ ,  $V_{HVDD} = +15V$ ,  $V_{HVSS} = 0V$ , Internal Reference,  $T_A = 25^\circ C$ , unless otherwise noted)



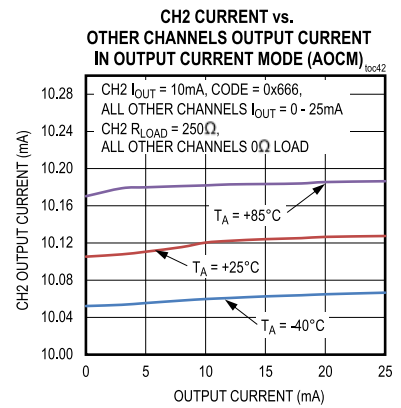
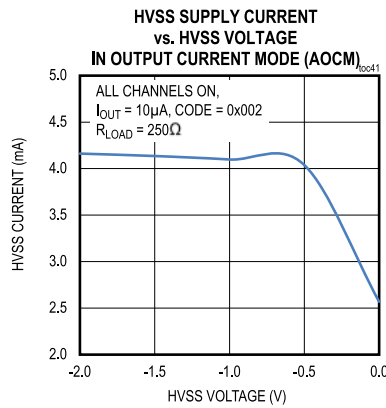
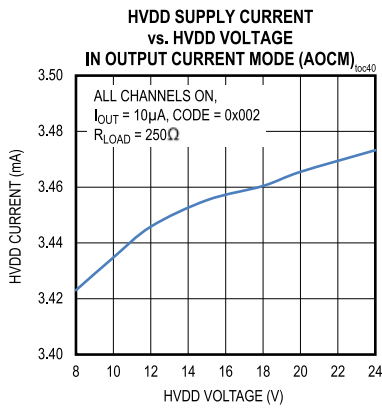
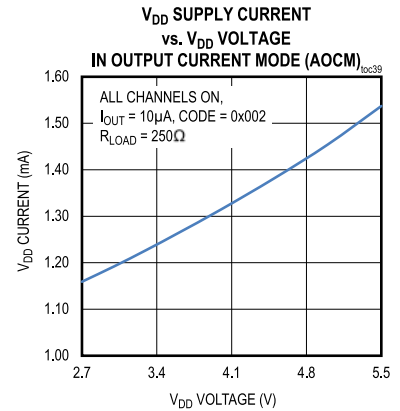
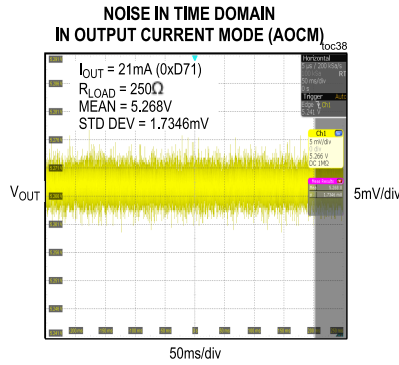
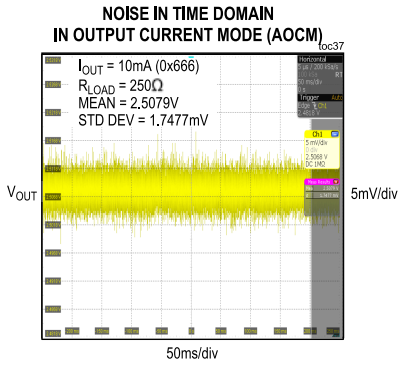
Typical Operating Characteristics (continued)

( $V_{DD} = +3.3V$ ,  $V_{HVDD} = +15V$ ,  $V_{HVSS} = 0V$ , Internal Reference,  $T_A = 25^\circ C$ , unless otherwise noted)



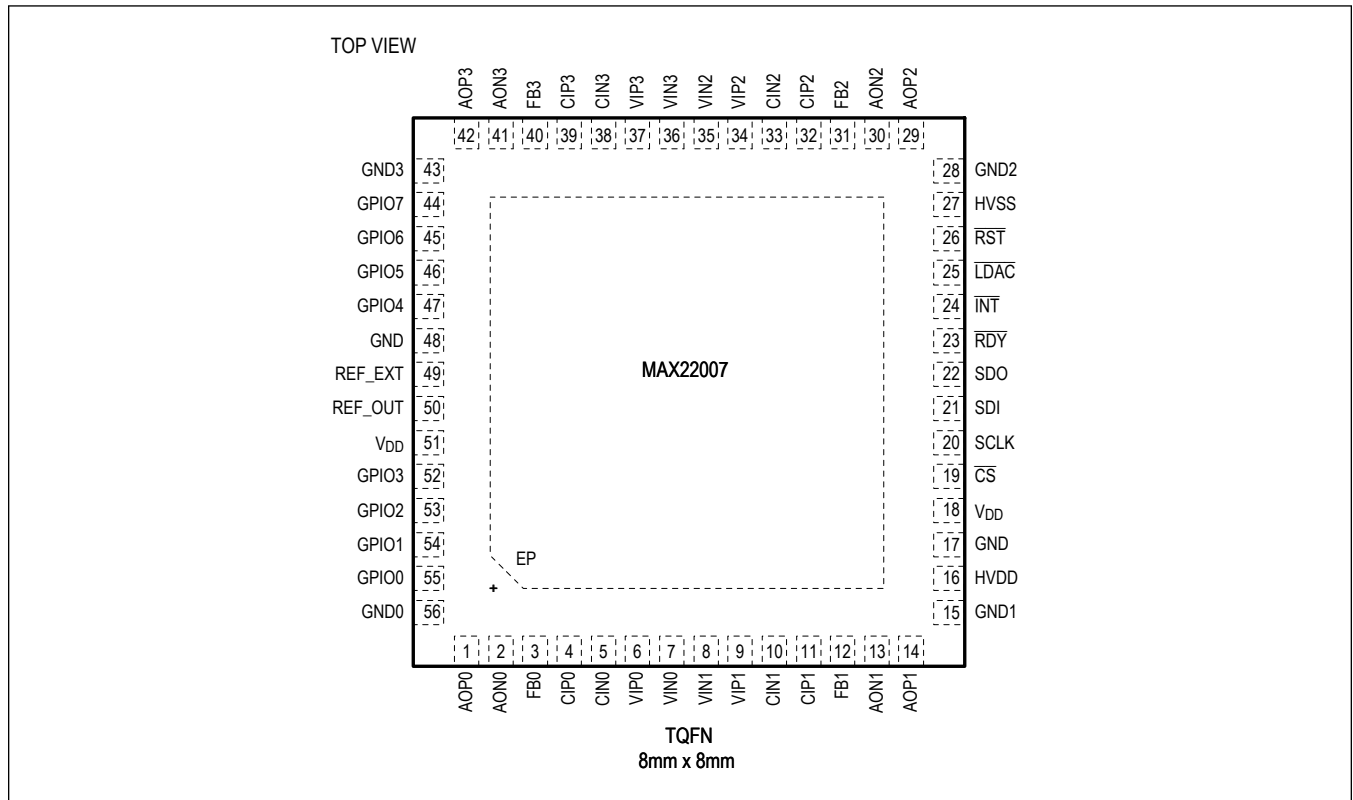
Typical Operating Characteristics (continued)

( $V_{DD} = +3.3V$ ,  $V_{HVDD} = +15V$ ,  $V_{HVSS} = 0V$ , Internal Reference,  $T_A = 25^\circ C$ , unless otherwise noted)



Pin Configuration

MAX22007



## Pin Description

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
<b>POWER SUPPLY</b>				
16	HVDD	Positive High-Voltage Power Supply from +8V to (HVSS +24V) for the Output Channels. Bypass HVDD to GND with a minimum 1 $\mu$ F ceramic capacitor as close to the device pin as possible.	HVDD	Power
17, 48	GND	Logic/Analog Ground	V <sub>DD</sub>	Ground
18, 51	V <sub>DD</sub>	Low-Voltage Power Supply from +2.7V to +5.5V. Connect both V <sub>DD</sub> pins together and bypass each pin to GND with a minimum 1 $\mu$ F ceramic capacitor as close to the device pin as possible.	V <sub>DD</sub>	Power
27	HVSS	Negative High-Voltage Power Supply from -2V to 0V for the Output Channels. For most applications connect HVSS to GND (0V), but in cases where the output must be down to 0V (or 0mA), connect HVSS to a -2V supply and in this case, bypass HVSS to GND with a minimum 1 $\mu$ F ceramic capacitor as close to the device pin as possible.	HVDD	Power
EP	EP	Exposed Pad. Connect the exposed pad on the bottom of the package to HVSS. Refer to the <a href="#">PCB Layout Recommendations</a> section for layout recommendations.	HVDD	Power
<b>VOLTAGE REFERENCE</b>				
49	REF_EXT	External Reference Voltage Input. Instead of the internal voltage reference, an external precision 2.500V reference can be connected between REF_EXT and GND. The REF_SEL bit in the <a href="#">Configuration</a> register must be set appropriately. If an external reference is connected to the REF_EXT pin, bypass it to GND with a minimum 1 $\mu$ F ceramic capacitor as close to the device pin as possible. If the internal reference is selected, tie this pin to GND.	V <sub>DD</sub>	Input
50	REF_OUT	Voltage Reference Output. The REF_OUT pin can be used to supply multiple devices from the same reference source. If not in use, leave REF_OUT unconnected.	V <sub>DD</sub>	Output
<b>ANALOG OUTPUT CHANNEL 0</b>				
1	AOP0	Channel 0 Positive Amplifier Output. Connect to the anode of an external diode.	HVDD	Output
2	AON0	Channel 0 Negative Amplifier Output. Connect to the cathode of an external diode.	HVDD	Output
3	FB0	Channel 0 Compensation Network Input. Refer to the <a href="#">Feedback (FB_) Inputs</a> section for details.	HVDD	Input
4	CIP0	Channel 0 Positive Current-Sense Input	HVDD	Input
5	CIN0	Channel 0 Negative Current-Sense Input	HVDD	Input
6	VIP0	Channel 0 Positive Voltage-Sense Input	HVDD	Input
7	VIN0	Channel 0 Negative Voltage-Sense Input	HVDD	Input
56	GND0	Channel 0 Ground. Connect GND0 to GND.	HVDD	Ground
<b>ANALOG OUTPUT CHANNEL 1</b>				
14	AOP1	Channel 1 Positive Amplifier Output. Connect to the anode of an external diode.	HVDD	Output



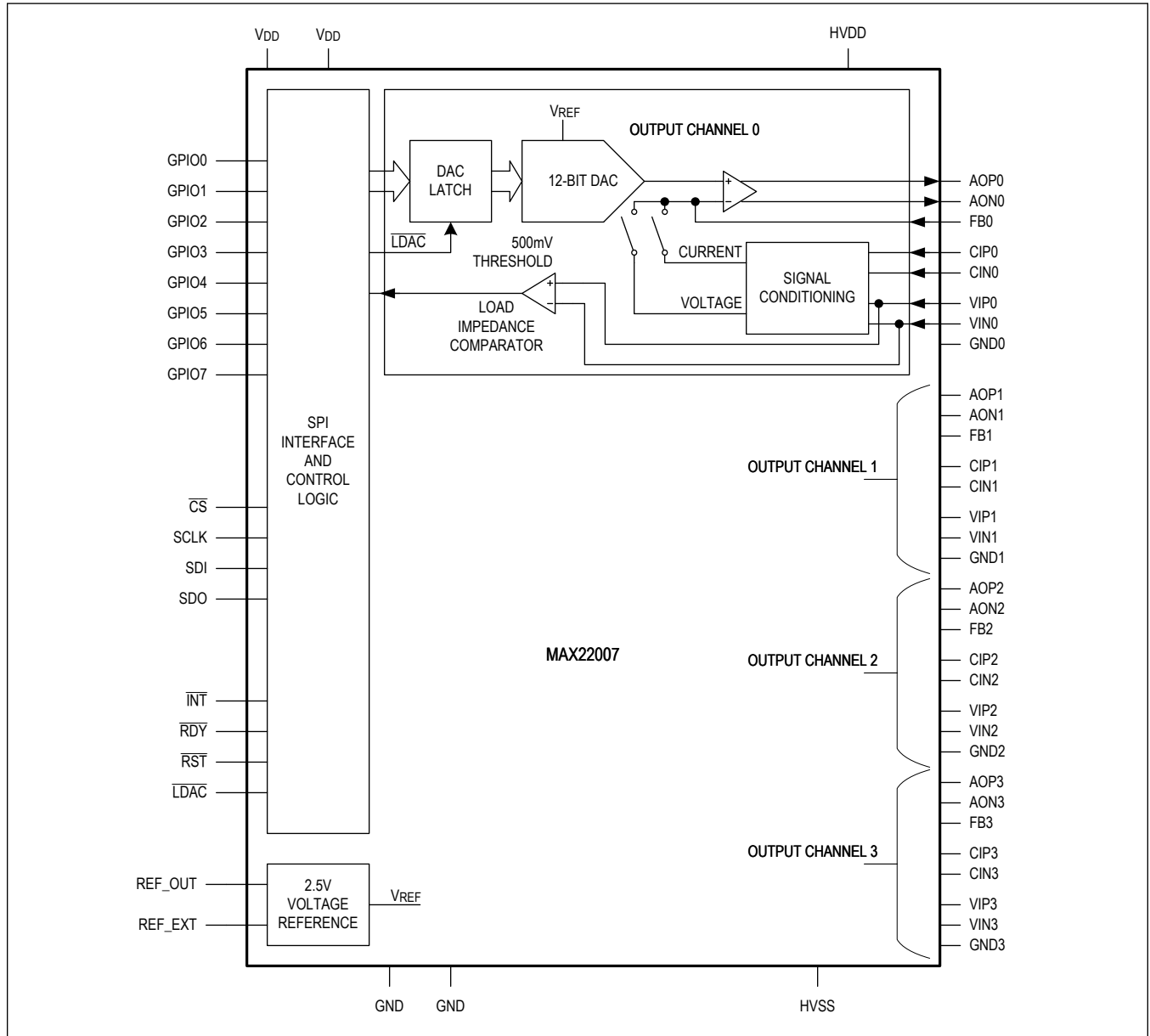
## Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
13	AON1	Channel 1 Negative Amplifier Output. Connect to the cathode of an external diode.	HVDD	Output
12	FB1	Channel 1 Compensation Network Input. Refer to the <a href="#">Feedback (FB<sub>n</sub>) Inputs</a> section for details.	HVDD	Input
11	CIP1	Channel 1 Positive Current-Sense Input	HVDD	Input
10	CIN1	Channel 1 Negative Current-Sense Input	HVDD	Input
9	VIP1	Channel 1 Positive Voltage-Sense Input	HVDD	Input
8	VIN1	Channel 1 Negative Voltage-Sense Input	HVDD	Input
15	GND1	Channel 1 Ground. Connect GND1 to GND.	HVDD	Ground
<b>ANALOG OUTPUT CHANNEL 2</b>				
29	AOP2	Channel 2 Positive Amplifier Output. Connect to the anode of an external diode.	HVDD	Output
30	AON2	Channel 2 Negative Amplifier Output. Connect to the cathode of an external diode.	HVDD	Output
31	FB2	Channel 2 Compensation Network Input. Refer to the <a href="#">Feedback (FB<sub>n</sub>) Inputs</a> section for details.	HVDD	Input
32	CIP2	Channel 2 Positive Current-Sense Input	HVDD	Input
33	CIN2	Channel 2 Negative Current-Sense Input	HVDD	Input
34	VIP2	Channel 2 Positive Voltage-Sense Input	HVDD	Input
35	VIN2	Channel 2 Negative Voltage-Sense Input	HVDD	Input
28	GND2	Channel 2 Ground. Connect GND2 to GND.	HVDD	Ground
<b>ANALOG OUTPUT CHANNEL 3</b>				
42	AOP3	Channel 3 Positive Amplifier Output. Connect to the anode of an external diode.	HVDD	Output
41	AON3	Channel 3 Negative Amplifier Output. Connect to the cathode of an external diode.	HVDD	Output
40	FB3	Channel 3 Compensation Network Input. Refer to the <a href="#">Feedback (FB<sub>n</sub>) Inputs</a> section for details.	HVDD	Input
39	CIP3	Channel 3 Positive Current-Sense Input	HVDD	Input
38	CIN3	Channel 3 Negative Current-Sense Input	HVDD	Input
37	VIP3	Channel 3 Positive Voltage-Sense Input	HVDD	Input
36	VIN3	Channel 3 Negative Voltage-Sense Input	HVDD	Input
43	GND3	Channel 3 Ground. Connect GND3 to GND.	HVDD	Ground
<b>LOGIC INTERFACE</b>				
19	$\overline{CS}$	Active-Low Chip Select Input from Controller. The SPI interface responds only when $\overline{CS}$ is low.	V <sub>DD</sub>	Input
20	SCLK	Serial Clock Input from Controller	V <sub>DD</sub>	Input
21	SDI	Serial Data Input. SPI MOSI data input from controller.	V <sub>DD</sub>	Input
22	SDO	Serial Data Output. SPI MISO data output to controller.	V <sub>DD</sub>	Output

## Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
23	$\overline{\text{RDY}}$	Active-Low Ready Output. $\overline{\text{RDY}}$ is asserted low after the last SCLK falling edge of an SPI transaction and is used to drive the $\overline{\text{CS}}$ input of the next MAX22007 when used for daisy-chain applications. If the MAX22007 is not used in daisy-chain mode, or is the last device in the daisy chain, $\overline{\text{RDY}}$ can be left unconnected.	$V_{\text{DD}}$	Output
24	$\overline{\text{INT}}$	Active-Low Open-Drain Interrupt Output. $\overline{\text{INT}}$ is asserted low when any interrupt source is detected and flagged in the <a href="#">Status &amp; Interrupts</a> register, provided that interrupt source has been enabled by setting the corresponding bit in the <a href="#">Interrupt Enable</a> register. Connect a pullup resistor from INT to $V_{\text{DD}}$ .	$V_{\text{DD}}$	Output
25	$\overline{\text{LDAC}}$	Active-Low DAC Load Input. When asserted low, transfers the contents of the DAC Channel Data registers and updates all the DAC outputs simultaneously. $\overline{\text{LDAC}}$ is ignored whilst $\overline{\text{RST}}$ is low. Connect to $V_{\text{DD}}$ if not used.	$V_{\text{DD}}$	Input
26	$\overline{\text{RST}}$	Active-Low Reset Input. When asserted low, reconfigures all registers to their power-on default states, analog outputs go high impedance, and DAC conversions stop.	$V_{\text{DD}}$	Input
55	GPIO0	General Purpose Digital Input/Output 0	$V_{\text{DD}}$	I/O
54	GPIO1	General Purpose Digital Input/Output 1	$V_{\text{DD}}$	I/O
53	GPIO2	General Purpose Digital Input/Output 2	$V_{\text{DD}}$	I/O
52	GPIO3	General Purpose Digital Input/Output 3	$V_{\text{DD}}$	I/O
47	GPIO4	General Purpose Digital Input/Output 4	$V_{\text{DD}}$	I/O
46	GPIO5	General Purpose Digital Input/Output 5	$V_{\text{DD}}$	I/O
45	GPIO6	General Purpose Digital Input/Output 6	$V_{\text{DD}}$	I/O
44	GPIO7	General Purpose Digital Input/Output 7	$V_{\text{DD}}$	I/O

Functional Diagrams



Note: Only one channel is shown for clarity.

## Detailed Description

The MAX22007 is a software-configurable four-channel analog output device that drives a voltage or current output on each channel. All outputs are protected to  $\pm 42V_{P-P}$  for high-voltage supply of  $HVDD = 8V$  to  $20V$  and  $HVSS = -2V$  to  $0V$ . Each output channel of the MAX22007 features a 12-bit DAC with fast settling time using a shared internal voltage reference.

The MAX22007 offers low-offset high-voltage amplifiers to condition the signal from low-voltage DAC outputs to high-voltage or current outputs. If one output is miswired, all other outputs remain unaffected and function normally. An internal comparator can be used to determine the load impedance and allows the microcontroller to intelligently select for voltage- or current-output mode. All outputs are kept safe by integrated current protection for functional and thermal robustness. The MAX22007 also includes a thermal shutdown circuit that protects the device when the junction temperature exceeds  $165^{\circ}C$  (typ).

The MAX22007 communicates to a microcontroller using an SPI interface at clock rates up to  $30MHz$  with an optional eight-bit CRC for improved data integrity. Eight GPIOs can be used to interface and control other resources on the circuit board. The MAX22007 operates from a  $2.7V$  to  $5.5V$  low-voltage supply, a  $+8V$  to  $+24V$  high-voltage positive supply, and a  $-2V$  to  $0V$  high-voltage negative supply. The MAX22007 is available in an  $8mm \times 8mm$  56-pin TQFN package and operates over the  $-40^{\circ}C$  to  $+85^{\circ}C$  temperature range with  $\pm 2.5kV$  HBM ESD protection on all pins.

## DAC

Each output channel features a separate low-power 12-bit DAC. The input value for each DAC is held in the corresponding Channel Data register. Each output channel uses a DAC latch between the Channel Data register and the DAC that contains the digital representation of the value that is currently presented at the channel output. The default configuration is to use the latch but it can be configured for transparent mode by setting the bits  $LD\_CNFG[3:0]$  in the [Configuration](#) register to 1. When  $LD\_CNFG[3:0]$  bits are set to 0, the operation of the latch is controlled by making the hardware pin  $\overline{LDAC}$  active low, or by setting  $LD\_CTRL[3:0]$  bits in the [Control](#) register using a SPI write operation. The  $LD\_CTRL[3:0]$  bits are self-clearing.

The MAX22007 offers several options to update the DAC output to accommodate different application requirements as shown in [Figure 4](#). In order for any of the analog outputs to change value, the values contained in the Channel Data registers need to be transferred to the DAC latch output. In transparent latch mode ( $LD\_CNFG[3:0]$  bits = 1), a write to the Channel Data register automatically updates the channel output value. In latch mode, a write transaction to one or all of the Channel Data registers does not necessarily change the channel output value. The options of controlling the  $\overline{LDAC}$  pin or setting the  $LD\_CTRL[3:0]$  bits allow for individual or simultaneous update of the channel output values, and to be able to control the exact timing of the update. Using the  $\overline{LDAC}$  pin over an SPI transaction to update the DAC latches has the advantage that the exact timing of the update can be controlled.

If no tight control of the output update timing is required, the step of loading the DAC latch can be eliminated by setting bits  $LD\_CNFG[3:0]$  in the [Configuration](#) register to 1 (transparent mode) and if one of the  $LD\_CNFG[x]$  bits is set for a certain channel, then writing to the Channel x Data register immediately updates the analog output value, bypassing the DAC latch altogether. Alternatively, if the  $\overline{LDAC}$  pin is tied to ground, the DAC latch automatically updates the DAC with the Channel Data register values.

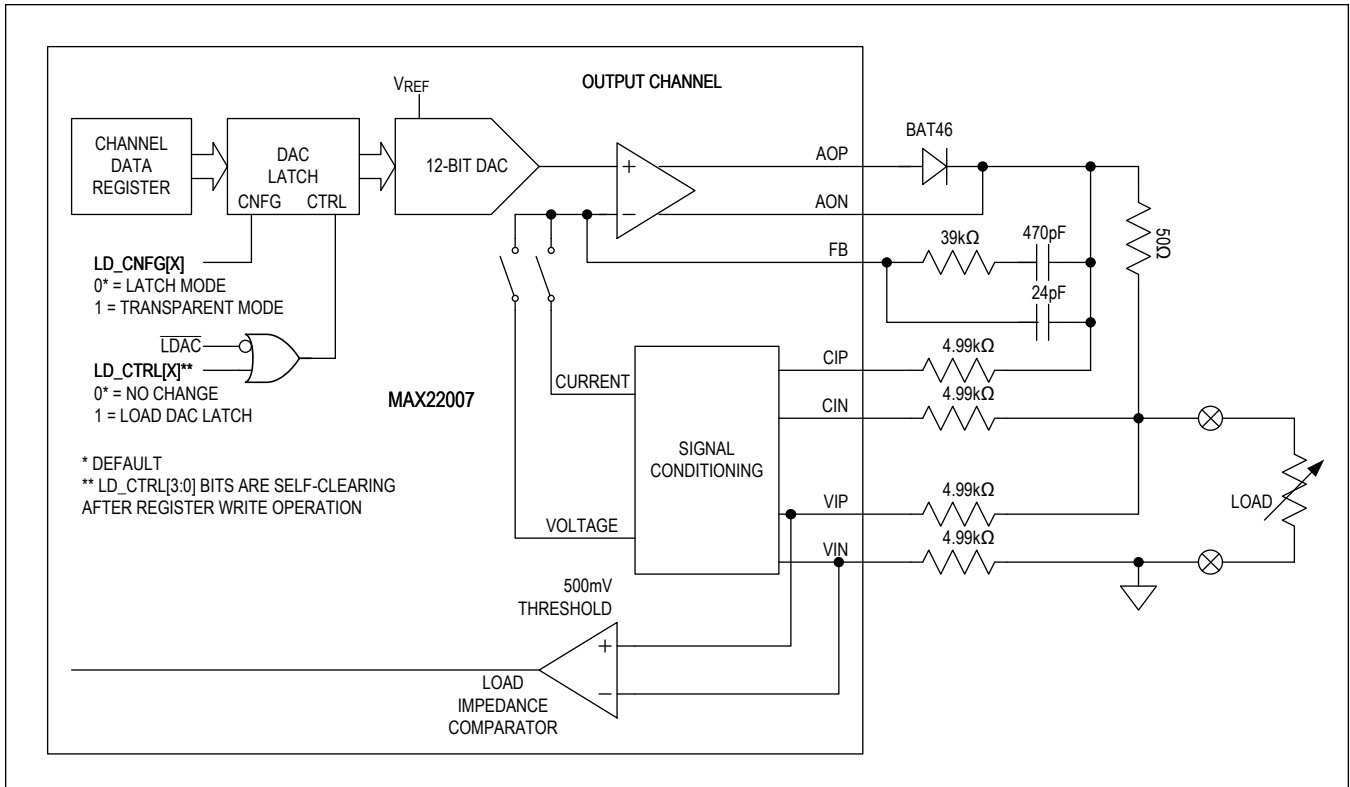


Figure 4. MAX22007 Output Channel

### High-Voltage Analog Output

The MAX22007 offers the following modes of operation:

- Analog Output-Voltage Mode (AOVM)
- Analog Output-Current Mode (AOCM)

The nominal output voltage range in AOVM is 0V to +10V, while linearity is guaranteed up to +10.5V. The DAC full-scale range is 0V to +12.5V to offer 25% overrange of the nominal output voltage range. In AOVM, the load voltage is sensed through the VIP\_ and VIN\_ inputs.

The ideal output voltage is given as:

$$V_{OUT} = 5 \times V_{REF} \times \frac{D}{2^N}$$

where,

D = Input code in the Channel x Data register

V<sub>REF</sub> = Reference voltage

N = Resolution of the DAC (N = 12)

The MAX22007 is factory calibrated using the internal reference. The full-scale range in AOVM is calibrated to 12.5V based on the internal reference; thus,  $V_{OUT} = 12.5 \times \frac{D}{2^N}$ . When using the external reference, V<sub>REF</sub> in the equation is the external reference voltage.

The nominal output current range in AOCM is 0mA to +20mA, while linearity is guaranteed up to +21mA. The DAC full-scale range is 0mA to +25mA to offer 25% overrange of the nominal output current range. In AOCM, the load current is sensed through the CIP\_ and CIN\_ inputs using an external 50Ω resistor. A value of 50Ω is required to produce the correct output-current range.

The ideal output current is given as:

$$I_{OUT} = \frac{V_{REF}}{2 \times R_{SENSE}} \times \frac{D}{2^N}$$

where,

D = Input code in the Channel x Data register

V<sub>REF</sub> = Reference voltage

R<sub>SENSE</sub> = External 50Ω sense resistor

N = Resolution of the DAC (N = 12)

The MAX22007 is factory calibrated using the internal reference and an ideal 50Ω sense resistor. The full-scale range in AOCM is calibrated to 25mA based on the external sense resistor; thus,  $I_{OUT} = \frac{1.25}{R_{SENSE}} \times \frac{D}{2^N}$ . The accuracy and temperature coefficient of the sense resistor contributes to the output accuracy. When using the external reference, V<sub>REF</sub> in the equation is the external reference voltage.

### Two-, Three-, and Four-Wire Operation

The MAX22007 can operate in two-wire, three-wire, or four-wire configurations, depending on the external connection of the CIN\_, VIP\_, and VIN\_ pins. Refer to the [Typical Application Circuits](#) section for examples of two-wire and four-wire applications.

### Feedback (FB\_) Inputs

The MAX22007 offers a feedback input pin (FB\_) per channel that allows access to the inverting input of the output amplifier to add an external compensation network as shown in the [Typical Application Circuits](#). The type of network and component values depend on the output load requirements. A recommended compensation network that offers stable amplifier performance over a wide range of resistive and capacitive loads for output voltage mode and a wide range of resistive and inductive loads for output current mode is shown in the [Typical Application Circuits](#).

### Comparator

The MAX22007 offers a comparator that monitors the output voltage through VIP\_ and VIN\_ per channel and sets a bit in the [Status & Interrupts](#) register if the output voltage exceeds a threshold of 500mV (typical). This comparator can be used to determine the load impedance to automatically detect whether a connected load requires output current mode or output voltage mode.

In order to determine the load impedance, set the output in question to output current mode. Increase the output current until the comparator trips, and the COMP\_INT[x] bit is set in the [Status & Interrupts](#) register. The load impedance is then simply the comparator threshold voltage of 500mV divided by the programmed output current.

The two bits COMP\_EDGE\_CNFG[1:0] in the [Configuration](#) register can be programmed to select different operating modes for the comparators, which in turn trigger the COMP\_INT[3:0] bits and assert the INT pin if enabled. This setting applies to all output channels. Programming COMP\_EDGE\_CNFG[1:0] to be 0b01 detects a rising edge at the comparator output, 0b10 detects a falling edge at the comparator output, and 0b11 shows the comparator output level, either a 0 or a 1, using the COMP\_INT[3:0] bits.

### Input and Output Protection

The AOP\_ and AON\_ outputs feature devices with a maximum operating voltage of 65V. The outputs can therefore tolerate ±42V<sub>P-P</sub> for a high-voltage supply HVDD up to +20V. The AOP\_ output uses an external small-signal diode. This series protection limits the current flowing into the MAX22007 to very small amounts in the μA-range in case the output

voltage is pulled above HVDD. A suitable external diode is BAT46. If the output is pulled below HVSS, an internal diode prevents any large current from flowing.

The protection of the FB\_, CIP\_, CIN\_, VIP\_, and VIN\_ inputs includes an external series resistor with a recommended value of 4.99k $\Omega$ . As long as the HVDD and HVSS supply voltages are actively driven, the voltages at these inputs remain within approximately 0.7V of HVDD or HVSS, irrespective of the actual external input voltage.

If an external DC-DC converter supplying HVDD malfunctions and is no longer capable of sinking or sourcing current, then the resistive feedback network around the DC-DC converter can be used to effectively protect the input pins of the MAX22007 as shown in [Figure 5](#). To protect the MAX22007 in this failure mode, the total resistance  $R_{PATH}$  of the feedback network of the DC-DC converter should be chosen as 30k $\Omega$  to limit the voltage at the input pins to a safe value of 36V.

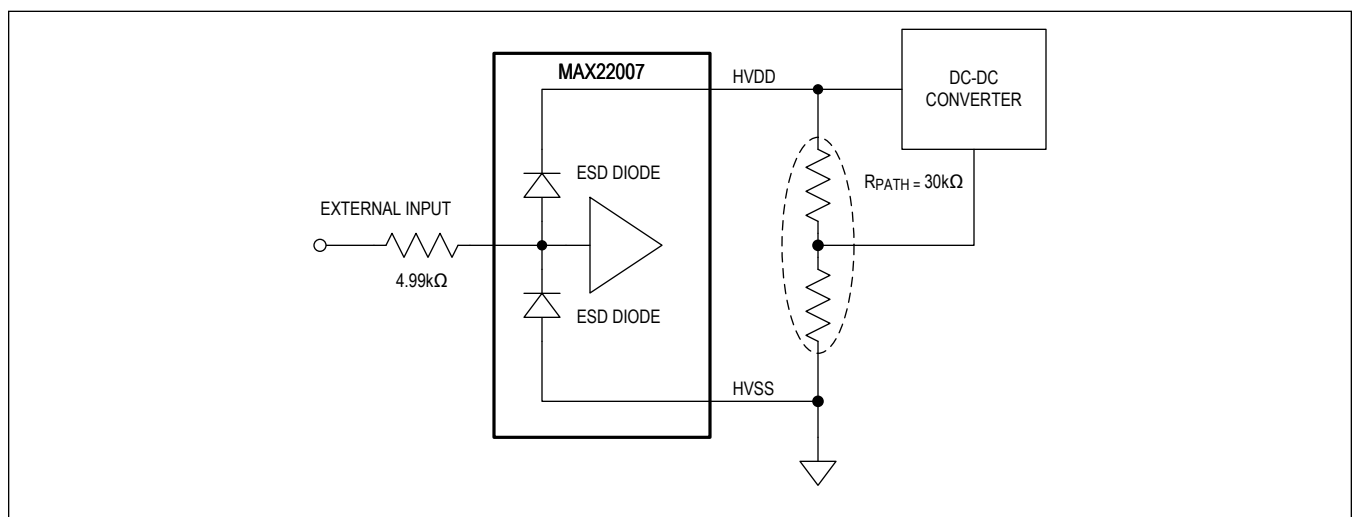


Figure 5. Input Protection of the MAX22007 In Case of External DC-DC Converter Failure

## Output Correction

To ease system calibration, reduce system test cost, and improve long-term system accuracy, all MAX22007 ICs are factory calibrated during final test for gain and offset adjustment. This output correction is applicable when operating in analog output-voltage mode (AOVM) or analog output-current mode (AOCM). The analog output is accurate to  $\pm 0.2\%$  at room temperature and to  $\pm 1\%$  over the full operating temperature range.

## Internal and External Reference

The MAX22007 includes an internal precision 2.500V reference with  $\pm 10\text{ppm}/^\circ\text{C}$  (typ) performance. Instead of the internal reference, an external 2.500V reference can be connected between REF\_EXT and GND. The typical input impedance of the REF\_EXT input is 100k $\Omega$ .

The REF\_SEL bit in the [Configuration](#) register is used to select between the internal reference and an external reference. At power-up, the internal reference is selected. The output voltage of the internal reference is available at the REF\_OUT pin, independent of the value of the REF\_SEL bit. The REF\_OUT pin is not designed to drive large capacitive loads and is provided to allow sharing of one internal voltage reference among multiple devices. REF\_OUT should be left unconnected if not used. If an external reference is selected and connected to the REF\_EXT pin, bypass it with a 1 $\mu\text{F}$  capacitor as close to the pin as possible. Otherwise, if the internal reference is selected, tie the REF\_EXT pin to GND. The MAX22007 is factory calibrated using the internal reference. The Electrical Characteristics are tested and guaranteed to the internal reference (see the [Electrical Characteristics](#) section). An external reference can provide better thermal performance; however, the factory calibration cannot be guaranteed.

### Short-Circuit Protection

When operating in analog output-voltage mode (AOVM), the analog output is constantly monitored for overcurrent conditions. Two modes of operation can be selected by the OVC\_CNFG bit in the [Configuration](#) register. In automatic mode, the output amplifier is powered down after an excessive output current is detected, and powers up approximately every 8ms for 400 $\mu$ s while the overcurrent condition exists. Once the overcurrent condition is resolved, the output amplifier remains in power-up mode. In host-controlled mode, the output amplifier is powered down after an excessive output current is detected, and the corresponding CHNL\_PWR[x] bit in the [Channel Mode](#) register is reset. The host is then responsible to rewrite the CHNL\_PWR[x] bit to enable the corresponding output channel.

In both cases, the interrupt bit OVC\_INT[x] in the [Status & Interrupts](#) register is set to logic high to indicate the overcurrent condition. In automatic mode, bit OVC\_INT[x] is automatically cleared once the overcurrent condition is resolved.

To allow capacitive loads to be charged up quickly, once an overcurrent condition is detected, the MAX22007 waits for approximately 400 $\mu$ s before the output amplifiers are powered down. This time window is sufficient to charge a completely discharged capacitive load of 1 $\mu$ F from 0V to +10V or vice versa without interrupting normal operation.

When the MAX22007 operates in analog output-current mode (AOCM), the short-circuit protection is disabled.

### Thermal Monitoring and Shutdown

The die temperature of the MAX22007 is constantly monitored. If the die temperature reaches 145°C (typical), the THWRNG\_INT bit in the [Status & Interrupts](#) register is set to logic high, and an interrupt is issued if bit THWRNG\_INTEN in the [Interrupt Enable](#) register is set to logic high. If the die temperature falls below 135°C (typical), bit THWRNG\_INT in the [Status & Interrupts](#) register is automatically cleared.

If the die temperature exceeds 165°C (typical), the THSHDN\_INT bit in the [Status & Interrupts](#) register is set to logic high, and the MAX22007 is shut down by powering down all amplifiers. The CHNL\_PWR[3:0] settings in the [Channel Mode](#) register are reset to their power-up values. Under this condition, an interrupt is always issued, i.e., the INT pin is pulled low.

In order to allow the voltage reference to power up and not produce false thermal shutdown and thermal warning interrupts, the thermal monitoring system is blocked from operation for the first 100ms after a power-on reset.

### SPI Interface

The MAX22007 features an SPI interface with clock speed up to 30MHz. An eight-bit cyclic redundancy check (CRC) is offered to improve the SPI data integrity in harsh environments. CRC checking can be enabled and disabled by setting the CRC\_EN bit in the [Configuration](#) register. The default condition for CRC\_EN bit is 1, meaning the CRC is enabled by default. The SPI transactions are 32-bits long if CRC is enabled as shown in [Table 1](#).

**Table 1. SPI Transaction with CRC Enabled**

BITS 31:25	BIT 24	BITS 23:8	BITS 7:0
Register Address	R/W	16-bit Payload	CRC

If CRC is disabled, the SPI transactions are 24-bits long as shown in [Table 2](#).

**Table 2. SPI Transaction with CRC Disabled**

BITS 23:17	BIT 16	BITS 15:0
Register Address	R/W	16-bit Payload



The MAX22007 implements the CRC-8/MAXIM algorithm with a  $0x31$  polynomial ( $x^8 + x^5 + x^4 + x^0$ ), the same polynomial that is used in Maxim's 1-wire® products. This CRC algorithm uses reflected input and output bytes (i.e., LSB first instead of MSB first on a byte basis; the byte order of the input sequence is not changed). The initial value is  $0x00$ , and the output is reported as is without any XOR operation. This CRC can detect the following types of errors:

- Any odd number of errors anywhere within the 32-bit number
- All double-bit errors anywhere within the 32-bit number
- Any cluster of errors that can be contained within an 8-bit window (1-8 bits incorrect)
- Most large clusters of errors

For write transactions, the CRC is calculated on the 24 bits that precede it, namely the 7-bit register address, the 1-bit read or write control, and the 16-bit payload. Here are two examples of write operations:

- Write  $0xF000$  to the [Interrupt Enable](#) register:  $0x04F0\_0007$
- Write  $0x53FA$  to the [Channel 1 Data](#) register:  $0x1053\_FA62$

For read transactions, the CRC sent back to the host by the MAX22007 is calculated on the 24 bits comprised of the 8-bit header received from the host (register address and read control) and the 16 bits of payload. Here are two examples of read operations:

- Read the default value from the [Configuration](#) register:  $0x0700\_007A$
- Read the default value from the [Channel Mode](#) register:  $0x0B00\_00C1$

Refer to AN27 for more details at: <https://www.maximintegrated.com/en/app-notes/index.mvp/id/27>.

### SPI Timeout

The MAX22007 offers timeout detection that monitors the SPI interface for transactions. In particular, the MAX22007 expects to see a properly formatted SPI transaction during the timeout interval. A properly formatted SPI transaction requires a falling edge of  $\overline{CS}$ , at least 24 SCLK cycles if CRC is disabled, or at least 32 SCLK cycles if CRC is enabled, and a rising edge of  $\overline{CS}$ . A valid CRC code is not required for an SPI transaction to be considered properly formatted. The timeout interval starts with the completion of every properly formatted SPI transaction and can be selected to last from 100ms to 1.6s (typical values) using the `TMOUT_SEL[3:0]` bits in the [Configuration](#) register. If no additional completion of a properly formatted SPI transaction is detected during the timeout interval, the `TMOUT_INT` bit in the [Status & Interrupts](#) register is set. If the `TMOUT_CNFG` bit in the [Configuration](#) register is set, in addition to setting the `TMOUT_INT` bit, all registers are reset to their power-on default values, except for the `TMOUT_INT` interrupt bit, the `TMOUT_INTEN` bit of the [Interrupt Enable](#) register, and the `CRC_EN` and `REF_SEL` bit settings in the [Configuration](#) register.

Timeout detection is disabled by default and must be enabled by setting the `TMOUT_EN` bit in the [Configuration](#) register. The first timeout interval starts at the completion of the SPI transaction that enables `TMOUT_EN`.

The timeout interval accuracy is  $\pm 50\%$  with respect to the nominal value that is selected using the `TMOUT_SEL[3:0]` bits in the [Configuration](#) register.

### SPI Daisy-Chain Operation

The MAX22007 offers an elongated programming operation that is typically used for devices in daisy-chain applications. The  $\overline{RDY}$  output of the MAX22007 feeds the  $\overline{CS}$  input of the next device in the daisy-chain as shown in [Figure 6](#).

The MAX22007 pulls the  $\overline{RDY}$  output low on the 24<sup>th</sup> or 32<sup>nd</sup> SCLK falling edge, depending on whether CRC is enabled or not, allowing the next device in the chain to begin its SPI operation, commencing with the 25<sup>th</sup> or 33<sup>rd</sup> SCLK falling edge, respectively. The timing for the SPI signals and the three chip select signals is shown in [Figure 7](#).

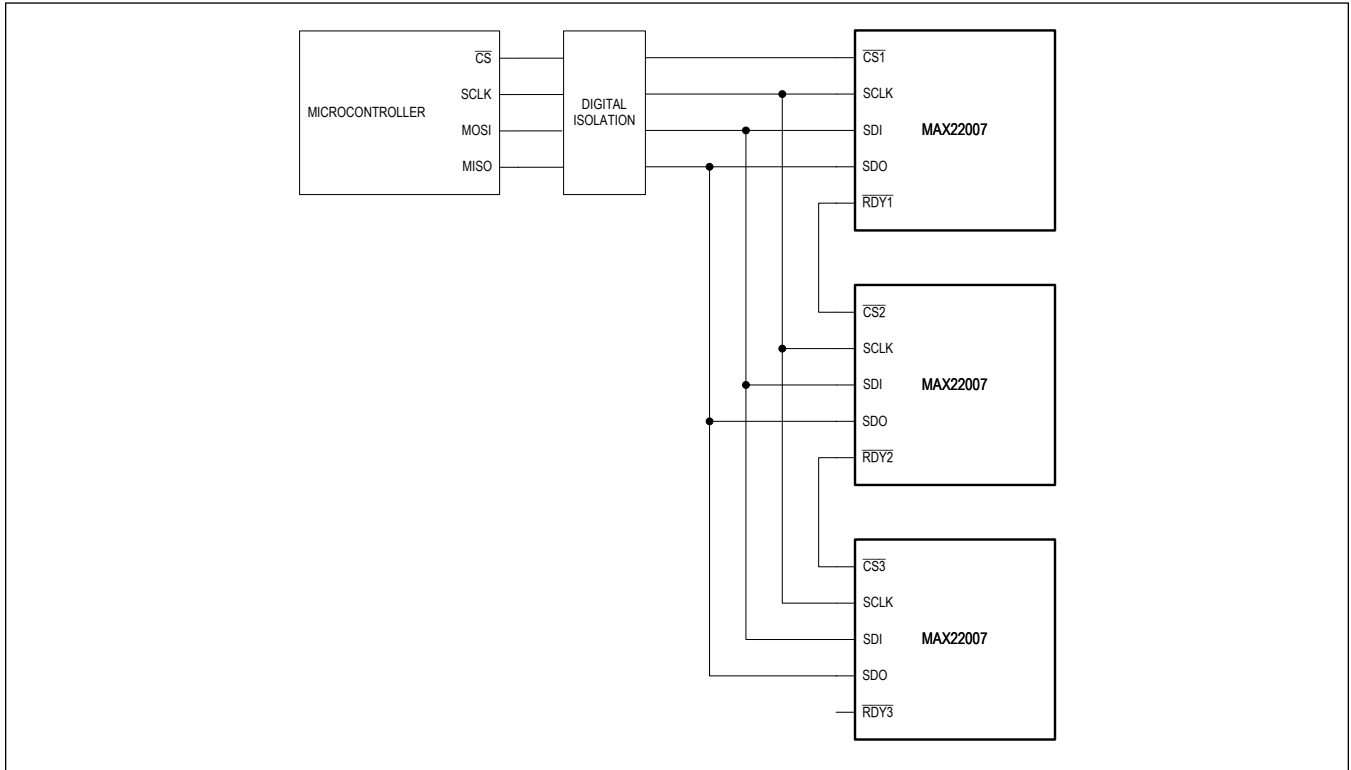


Figure 6. Daisy-Chain Operation

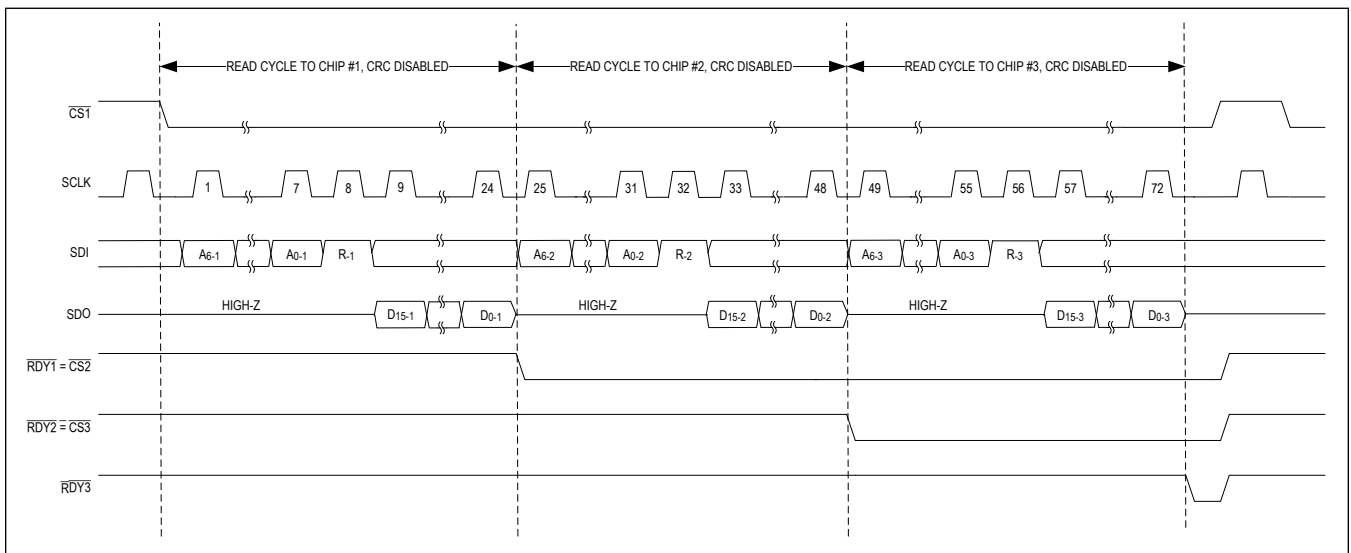


Figure 7. Daisy-Chain SPI Write Diagram

### Load DAC ( $\overline{\text{LDAC}}$ ) Input

The MAX22007 features an active-low  $\overline{\text{LDAC}}$  logic input that allows the channels to update asynchronously.  $\overline{\text{LDAC}}$  should be kept high or connected to  $V_{\text{DD}}$  when the device is controlled only through the SPI interface. A high-to-low transition of  $\overline{\text{LDAC}}$  simultaneously updates the channel outputs with data from the Channel x Data registers. If  $\overline{\text{LDAC}}$  is held low, the contents of the Channel x Data registers are passed through to the DAC immediately, updating the channel outputs.

The LD\_CNFG[3:0] bits in the [Configuration](#) register are used to configure the  $\overline{\text{LDAC}}$  operation for each channel, independently. When LD\_CNFG[x] is set to 1 (transparent mode), writing to the Channel x Data register immediately updates the DAC output value, regardless of the  $\overline{\text{LDAC}}$  logic level. When LD\_CNFG[x] is set to 0, the DAC output is updated at the  $\overline{\text{LDAC}}$  falling edge with the current content of the Channel x Data register.

### Power-On Reset

The low-voltage  $V_{\text{DD}}$  supply is monitored by power-on reset circuitry. The MAX22007 is held in a reset state until the  $V_{\text{DD}}$  supply has reached a certain threshold that allows safe operation without loss of data. Once this threshold is exceeded, the SPI interface and low-voltage circuitry is fully functional. The high-voltage supplies (HVDD and HVSS) are also constantly monitored. The loss of the high-voltage supply is indicated by the HVDD\_INT bit in the [Status & Interrupts](#) register. The HVDD\_INT bit is set when the voltage difference between HVDD and HVSS is approximately 1.5V.

### Software Reset

A software reset can be accomplished by writing to the SW\_CLR or SW\_RST bit in the [Soft Reset](#) register. Both bits have a default state of 0 for normal operating condition. Writing a 1 to the SW\_RST bit resets all registers except the CRC\_EN and REF\_SEL bits in the [Configuration](#) register. Writing a 1 to SW\_CLR bit resets only the Channel x Data registers and the DAC latches. Both bits are self-clearing.

### Hardware Reset ( $\overline{\text{RST}}$ )

The MAX22007 features an asynchronous active-low  $\overline{\text{RST}}$  logic input that resets the MAX22007 to power-on reset conditions. Driving  $\overline{\text{RST}}$  low also aborts any on-going SPI transaction. To allow a new SPI transaction,  $\overline{\text{RST}}$  must be driven high.

### Product Tracking

The MAX22007 includes a 16-bit device tracking number, unique to each device revision manufactured, accessible through the SPI interface. This feature enables tracking individual IC revisions. Refer to the [Revision ID](#) register for details.

Register Map

Registers

ADDRESS	RESET	NAME	MSB							LSB
<b>Revision</b>										
0x00	0xBB47	<a href="#">Revision ID[15:8]</a>	PART_ID[7:0]							
		<a href="#">Revision ID[7:0]</a>	REV_ID[7:0]							
<b>Interrupts</b>										
0x01	0x0000	<a href="#">Status &amp; Interrupts[15:8]</a>	COMP_INT[3:0]			OVC_INT[3:0]				
		<a href="#">Status &amp; Interrupts[7:0]</a>	Reserved[1:0]	THSHDN_INT	THWRN_G_INT	HVDD_INT	TMOUT_INT	GPI_INT	CRC_INT	
0x02	0x0000	<a href="#">Interrupt Enable[15:8]</a>	COMP_INTEN[3:0]			OVC_INTEN[3:0]				
		<a href="#">Interrupt Enable[7:0]</a>	Reserved[2:0]		THWRN_G_INTEN	HVDD_INTEN	TMOUT_INTEN	GPI_INTEN	CRC_INTEN	
<b>General Controls</b>										
0x03	0x0001	<a href="#">Configuration[15:8]</a>	LD_CNFG[3:0]			COMP_EDGE_CNFG[1:0]		Reserved	REF_SEL	
		<a href="#">Configuration[7:0]</a>	TMOUT_SEL[3:0]			TMOUT_CNFG	TMOUT_EN	OVC_CNFG	CRC_EN	
0x04	0x0000	<a href="#">Control[15:8]</a>	LD_CTRL[3:0]			Reserved[3:0]				
		<a href="#">Control[7:0]</a>	Reserved[7:0]							
0x05	0x0000	<a href="#">Channel Mode[15:8]</a>	CHNL_MODE[3:0]			CHNL_PWR[3:0]				
		<a href="#">Channel Mode[7:0]</a>	Reserved[7:0]							
0x06	0x0000	<a href="#">Soft Reset[15:8]</a>	Reserved[2:0]		SW_CLR	Reserved[2:0]			SW_RST	
		<a href="#">Soft Reset[7:0]</a>	Reserved[7:0]							
<b>DAC Data</b>										
0x07	0x0000	<a href="#">Channel 0 Data[15:8]</a>	DATA_CH_0[11:4]							
		<a href="#">Channel 0 Data[7:0]</a>	DATA_CH_0[3:0]			Reserved[3:0]				
0x08	0x0000	<a href="#">Channel 1 Data[15:8]</a>	DATA_CH_1[11:4]							
		<a href="#">Channel 1 Data[7:0]</a>	DATA_CH_1[3:0]			Reserved[3:0]				
0x09	0x0000	<a href="#">Channel 2 Data[15:8]</a>	DATA_CH_2[11:4]							

ADDRESS	RESET	NAME	MSB						LSB
		<a href="#">Channel 2 Data[7:0]</a>		DATA_CH_2[3:0]			Reserved[3:0]		
0x0A	0x0000	<a href="#">Channel 3 Data[15:8]</a>		DATA_CH_3[11:4]					
		<a href="#">Channel 3 Data[7:0]</a>		DATA_CH_3[3:0]			Reserved[3:0]		
<b>GPIO Ports</b>									
0x0B	0x0000	<a href="#">GPIO Control[15:8]</a>		GPIO_EN[7:0]					
		<a href="#">GPIO Control[7:0]</a>		GPIO_DIR[7:0]					
0x0C	0x0000	<a href="#">GPIO Data[15:8]</a>		GPO_DATA[7:0]					
		<a href="#">GPIO Data[7:0]</a>		GPI_DATA[7:0]					
0x0D	0x0000	<a href="#">GPI Edge Detection Control[15:8]</a>		GPI_POS_EDGE_INT[7:0]					
		<a href="#">GPI Edge Detection Control[7:0]</a>		GPI_NEG_EDGE_INT[7:0]					
0x0E	0x0000	<a href="#">GPI Edge Detection Status[15:8]</a>		GPI_POS_EDGE_INT_STA[7:0]					
		<a href="#">GPI Edge Detection Status[7:0]</a>		GPI_NEG_EDGE_INT_STA[7:0]					

**Register Details**

Revision ID (0x0)

BIT	15	14	13	12	11	10	9	8
Field	PART_ID[7:0]							
Reset	0xBB							
Access Type	Read Only							
BIT	7	6	5	4	3	2	1	0
Field	REV_ID[7:0]							
Reset	0x47							
Access Type	Read Only							
BITFIELD	BITS		DESCRIPTION					
PART_ID	15:8		Part Identification Code: 0xBB					
REV_ID	7:0		Revision Identification Code: REV_ID[7:4]: 0x4 REV_ID[3:0]: silicon revision (starting at 0x7)					

**Status & Interrupts (0x1)**

<b>BIT</b>	<b>15</b>	<b>14</b>	<b>13</b>	<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>
<b>Field</b>	COMP_INT[3:0]				OVC_INT[3:0]			
<b>Reset</b>	0x0				0x0			
<b>Access Type</b>	Read Clears All				Read Only			
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>Field</b>	Reserved[1:0]		THSHDN_I NT	THWRNG_I NT	HVDD_INT	TMOUT_IN T	GPI_INT	CRC_INT
<b>Reset</b>	0b00		0b0	0b0	0b0	0b0	0b0	0b0
<b>Access Type</b>	Read Only		Read Clears All	Read Only	Read Only	Read Clears All	Read Clears All	Read Clears All

<b>BITFIELD</b>	<b>BITS</b>	<b>DESCRIPTION</b>	<b>DECODE</b>
COMP_INT	15:12	<p>Comparator interrupt for output channels.</p> <p>Bit 15 = Channel 3 Bit 14 = Channel 2 Bit 13 = Channel 1 Bit 12 = Channel 0</p> <p>The event reported by the interrupt depends on the setting of COMP_EDGE_CNFG[1:0], which defines global configuration for all channel comparators:</p> <p>COMP_EDGE_CNFG = 0x1, the interrupt reports a rising edge was detected at the output of the corresponding comparator. The interrupt is cleared on read.</p> <p>COMP_EDGE_CNFG = 0x2, the interrupt reports a falling edge was detected at the output of the corresponding comparator. The interrupt is cleared on read.</p> <p>COMP_EDGE_CNFG = 0x3, the interrupt reports the output level of the corresponding comparator. Reading the interrupt register has no impact on this interrupt.</p>	<p>0: No rising or falling edge detected (COMP_EDGE_CNFG = 0x1 or 0x2) or output level is low (COMP_EDGE_CNFG = 0x3).</p> <p>1: Rising or falling edge detected (COMP_EDGE_CNFG = 0x1 or 0x2) or output level is high (COMP_EDGE_CNFG = 0x3).</p>

BITFIELD	BITS	DESCRIPTION	DECODE
OVC_INT	11:8	<p>Overcurrent interrupt per output channel.</p> <p>Bit 11 = Channel 3 Bit 10 = Channel 2 Bit 9 = Channel 1 Bit 8 = Channel 0</p> <p>Asserted when the channel is in output-voltage mode and the output current exceeds 50mA (typical).</p> <p>The clearing behavior of this bit depends on the setting of OVC_CNFG in the Configuration register.</p> <p>OVC_CNFG = 0, automatic mode. OVC_INT is cleared once the overcurrent condition is resolved, and the corresponding output amplifier is powered up.</p> <p>OVC_CNFG = 1, host-controlled mode. The corresponding output channel is powered down. OVC_INT is only cleared when read.</p>	<p>0: AOVM current below 50mA 1: AOVM current above 50mA</p>
Reserved	7:6	Reserved	
THSHDN_INT	5	<p>Thermal shutdown interrupt. Asserted when the die temperature exceeds 165°C (typical). The Channel Mode register field CHNL_PWR[3:0] is reset when this interrupt is asserted.</p> <p>Cleared when read.</p>	<p>0: Internal temperature below 165°C 1: Internal temperature above 165°C</p>
THWRNG_INT	4	<p>Thermal warning interrupt. Asserted when the die temperature exceeds 145°C (typical). Cleared when the device internal temperature falls below 135°C (typical).</p>	<p>0: Internal temperature below 145°C (rising), or 135°C (falling) 1: Internal temperature above 145°C</p>
HVDD_INT	3	<p>Asserted when the high-voltage supply HVDD falls below a preset threshold, indicating that the functionality of the amplifiers is not guaranteed.</p> <p>Cleared when the high-voltage supply exceeds the threshold again.</p>	<p>0: HVDD supply is above preset threshold 1: HVDD supply is below preset threshold</p>
TMOUT_INT	2	<p>SPI time-out interrupt. Asserted when no properly formatted SPI transaction has been detected for a duration exceeding the selected time-out period. A properly formatted transaction is a transaction that has a minimum of 24 bits (if CRC is disabled) or 32 bits (if CRC is enabled). A properly formatted transaction is always accounted for at the end of the transaction.</p> <p>Cleared when read.</p>	<p>0: No SPI time-out detected 1: SPI time-out detected</p>

BITFIELD	BITS	DESCRIPTION	DECODE
GPI_INT	1	Asserted when at least one positive or negative edge was detected at the input of at least one input-configured GPIOs, and the GPI edge detection is enabled in the GPI Edge Detection Control register. Cleared when read.	0: No edge detected on any input-configured GPIO 1: At least one edge detected on at least one input-configured GPIO
CRC_INT	0	Asserted when a CRC error is detected when the CRC mode is enabled. Cleared when read.	0: No CRC error detected 1: At least one CRC error detected

**Interrupt Enable (0x2)**

BIT	15	14	13	12	11	10	9	8
Field	COMP_INTEN[3:0]				OVC_INTEN[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			
BIT	7	6	5	4	3	2	1	0
Field	Reserved[2:0]			THWRNG_INTEN	HVDD_INTEN	TMOUT_INTEN	GPI_INTEN	CRC_INTEN
Reset	0b000			0b0	0b0	0b0	0b0	0b0
Access Type	Read Only			Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
COMP_INTEN	15:12	Comparator interrupt enables for COMP_INT[3:0].  Bit 15 = Channel 3 interrupt enable Bit 14 = Channel 2 interrupt enable Bit 13 = Channel 1 interrupt enable Bit 12 = Channel 0 interrupt enable  When set, the $\overline{INT}$ pin is asserted low when the corresponding COMP_INT interrupt bit is asserted.	0: COMP_INT does not assert the $\overline{INT}$ pin 1: COMP_INT asserts the $\overline{INT}$ pin
OVC_INTEN	11:8	Overcurrent interrupt enables for OVC_INT[3:0].  Bit 11 = Channel 3 interrupt enable Bit 10 = Channel 2 interrupt enable Bit 9 = Channel 1 interrupt enable Bit 8 = Channel 0 interrupt enable  OVC_INT[3:0] interrupt enable. When set, the $\overline{INT}$ pin is asserted low when the corresponding OVC_INT[3:0] interrupt bit is asserted.	0: OVC_INT does not assert $\overline{INT}$ pin 1: OVC_INT asserts $\overline{INT}$ pin
Reserved	7:5	Reserved	
THWRNG_INTEN	4	THWRNG_INT interrupt enable. When set, the $\overline{INT}$ pin is asserted low when the THWRNG_INT interrupt bit is asserted.	0: THWRNG_INT does not assert the $\overline{INT}$ pin 1: THWRNG_INT asserts the $\overline{INT}$ pin



BITFIELD	BITS	DESCRIPTION	DECODE
HVDD_INTEN	3	HVDD_INT interrupt enable. When set, the $\overline{\text{INT}}$ pin is asserted low when the HVDD_INT interrupt bit is asserted.	0: HVDD_INT does not assert the $\overline{\text{INT}}$ pin 1: HVDD_INT asserts the $\overline{\text{INT}}$ pin
TMOUT_INTEN	2	TMOUT_INT interrupt enable. When set, the $\overline{\text{INT}}$ pin is asserted low when the TMOUT_INT interrupt bit is asserted.	0: TMOUT_INT does not assert the $\overline{\text{INT}}$ pin 1: TMOUT_INT asserts the $\overline{\text{INT}}$ pin
GPI_INTEN	1	GPI_INT interrupt enable. When set, the $\overline{\text{INT}}$ pin is asserted low when the GPI_INT interrupt bit is asserted.	0: GPI_INT does not assert the $\overline{\text{INT}}$ pin 1: GPI_INT asserts the $\overline{\text{INT}}$ pin
CRC_INTEN	0	CRC_INT interrupt enable. When set, the $\overline{\text{INT}}$ pin is asserted low when the CRC_INT interrupt bit is asserted.	0: CRC_INT does not assert the $\overline{\text{INT}}$ pin 1: CRC_INT asserts the $\overline{\text{INT}}$ pin

**Configuration (0x03)**

BIT	15	14	13	12	11	10	9	8
Field	LD_CNFG[3:0]				COMP_EDGE_CNFG[1:0]		Reserved	REF_SEL
Reset	0x0				0b00		0b0	0b0
Access Type	Write, Read				Write, Read		Read Only	Write, Read
BIT	7	6	5	4	3	2	1	0
Field	TMOUT_SEL[3:0]				TMOUT_CNFG	TMOUT_EN	OVC_CNFG	CRC_EN
Reset	0x0				0b0	0b0	0b0	0b1
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LD_CNFG	15:12	DAC latch mode control per output channel. Bit 15 = Channel 3 Bit 14 = Channel 2 Bit 13 = Channel 1 Bit 12 = Channel 0	0: The DAC latch is operational and is controlled by the corresponding LD_CTRL bit in the Control register or the LDAC pin.  1: The DAC latch is transparent, and any value written to the Channel x Data register is directly applied to the DAC.
COMP_EDGE_CNFG	11:10	Comparator edge detection configuration for all channel comparators	0b00: Powers down the comparators 0b01: Detects rising edges at the comparator outputs 0b10: Detects falling edges at the comparator outputs 0b11: Shows the comparator outputs
Reserved	9	Reserved	
REF_SEL	8	Voltage reference selection	0: Internal voltage reference 1: External voltage reference

BITFIELD	BITS	DESCRIPTION	DECODE
TMOUT_SEL	7:4	Time-out expiration time selection, for typical values.	0x0: 100ms (default) 0x1: 200ms 0x2: 300ms 0x3: 400ms 0x4: 500ms 0x5: 600ms 0x6: 700ms 0x7: 800ms 0x8: 900ms 0x9: 1.0s 0xA: 1.1s 0xB: 1.2s 0xC: 1.3s 0xD: 1.4s 0xE: 1.5s 0xF: 1.6s
TMOUT_CNFG	3	SPI time-out configuration	0: By default, only TMOUT_INT is asserted in case of a time-out event.  1: TMOUT_INT is asserted in case of a time-out event, and the device is reset, except for the TMOUT_INT interrupt bit, the TMOUT_INTEN bit of the Interrupt Enable register, and the CRC_EN bit and REF_SEL bit of the Configuration register.
TMOUT_EN	2	SPI time-out enable	0: SPI time-out function is disabled 1: SPI time-out function is enabled
OVC_CNFG	1	Overcurrent response control	0: Automatic mode In case of overcurrent detection, the device powers down the corresponding output amplifier, indicated by OVC_INT[x], and powers it up every 8ms for 400µs while the overcurrent condition exists. Once the overcurrent condition is resolved, the output amplifier remains in power-up mode.  1: Host-controlled mode In case of overcurrent detection, the device powers down the corresponding output amplifier, indicated by OVC_INT[x], and the corresponding bit in the CHNL_PWR[3:0] register field is reset. The host is then responsible to rewrite the corresponding bit in the CHNL_PWR[3:0] register field to restart the channel.
CRC_EN	0	When set, enables the CRC verification for incoming and outgoing SPI frames. When CRC is enabled, the SPI frame is 32-bits long. When CRC is disabled, the SPI frame is 24-bits long.	0: CRC disabled 1: CRC enabled (default)

**Control (0x4)**

<b>BIT</b>	<b>15</b>	<b>14</b>	<b>13</b>	<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>
<b>Field</b>	LD_CTRL[3:0]				Reserved[3:0]			
<b>Reset</b>	0x0				0x0			
<b>Access Type</b>	Write Only Clears All				Read Only			
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>Field</b>	Reserved[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Only							

<b>BITFIELD</b>	<b>BITS</b>	<b>DESCRIPTION</b>	<b>DECODE</b>
LD_CTRL	15:12	DAC latch load control. When set, loads the contents of the corresponding channel data register to the DAC output if the corresponding LD_CNFG[3:0] configuration bit is logic low. These bits are self-clearing upon the completion of the SPI transaction.  Bit 15 = Channel 3 Bit 14 = Channel 2 Bit 13 = Channel 1 Bit 12 = Channel 0	0: No action 1: Loads the contents of the corresponding channel data register to the DAC output
Reserved	11:8	Reserved	
Reserved	7:0	Reserved	

**Channel Mode (0x5)**

<b>BIT</b>	<b>15</b>	<b>14</b>	<b>13</b>	<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>
<b>Field</b>	CHNL_MODE[3:0]				CHNL_PWR[3:0]			
<b>Reset</b>	0x0				0x0			
<b>Access Type</b>	Write, Read				Write, Read			
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>Field</b>	Reserved[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Only							

<b>BITFIELD</b>	<b>BITS</b>	<b>DESCRIPTION</b>	<b>DECODE</b>
CHNL_MODE	15:12	Channel mode selection per channel.  Bit 15 = Channel 3 Bit 14 = Channel 2 Bit 13 = Channel 1 Bit 12 = Channel 0	0: Voltage mode 1: Current mode

BITFIELD	BITS	DESCRIPTION	DECODE
CHNL_PWR	11:8	Channel power control per channel. Bit 11 = Channel 3 Bit 10 = Channel 2 Bit 9 = Channel 1 Bit 8 = Channel 0	0: Channel powered off 1: Channel powered on
Reserved	7:0	Reserved	

**Soft Reset (0x6)**

BIT	15	14	13	12	11	10	9	8
Field	Reserved[2:0]			SW_CLR	Reserved[2:0]			SW_RST
Reset	0b000			0b0	0b000			0b0
Access Type	Read Only			Write Only Clears All	Read Only			Write Only Clears All
BIT	7	6	5	4	3	2	1	0
Field	Reserved[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
Reserved	15:13	Reserved	
SW_CLR	12	Data register reset control. Resets only the Channel Data registers and DAC latch control bits. This bit is self-clearing upon the completion of the SPI transaction.	0: Normal operation 1: Resets all Channel Data registers and DAC latch control bits
Reserved	11:9	Reserved	
SW_RST	8	Software reset control. Resets all registers except CRC_EN and REF_SEL bits in the Configuration register. This bit is self-clearing upon the completion of the SPI transaction.	0: Normal operation 1: Resets all registers except CRC_EN and REF_SEL bits in the Configuration register
Reserved	7:0	Reserved	

**Channel 0 Data (0x07)**

BIT	15	14	13	12	11	10	9	8
Field	DATA_CH_0[11:4]							
Reset	0x000							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	DATA_CH_0[3:0]				Reserved[3:0]			
Reset	0x000				0x0			
Access Type	Write, Read				Read Only			

BITFIELD	BITS	DESCRIPTION
DATA_CH_0	15:4	Channel 0 data
Reserved	3:0	Reserved

**Channel 1 Data (0x8)**

BIT	15	14	13	12	11	10	9	8
Field	DATA_CH_1[11:4]							
Reset	0x000							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	DATA_CH_1[3:0]				Reserved[3:0]			
Reset	0x000				0x0			
Access Type	Write, Read				Read Only			

BITFIELD	BITS	DESCRIPTION
DATA_CH_1	15:4	Channel 1 data
Reserved	3:0	Reserved

**Channel 2 Data (0x9)**

BIT	15	14	13	12	11	10	9	8
Field	DATA_CH_2[11:4]							
Reset	0x000							
Access Type	Write, Read							
BIT	7	6	5	4	3	2	1	0
Field	DATA_CH_2[3:0]				Reserved[3:0]			
Reset	0x000				0x0			
Access Type	Write, Read				Read Only			

BITFIELD	BITS	DESCRIPTION
DATA_CH_2	15:4	Channel 2 data
Reserved	3:0	Reserved

**Channel 3 Data (0xA)**

BIT	15	14	13	12	11	10	9	8
Field	DATA_CH_3[11:4]							
Reset	0x000							
Access Type	Write, Read							

<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>Field</b>	DATA_CH_3[3:0]				Reserved[3:0]			
<b>Reset</b>	0x000				0x0			
<b>Access Type</b>	Write, Read				Read Only			

<b>BITFIELD</b>	<b>BITS</b>	<b>DESCRIPTION</b>
DATA_CH_3	15:4	Channel 3 data
Reserved	3:0	Reserved

**GPIO Control (0x0B)**

<b>BIT</b>	<b>15</b>	<b>14</b>	<b>13</b>	<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>
<b>Field</b>	GPIO_EN[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>Field</b>	GPIO_DIR[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

<b>BITFIELD</b>	<b>BITS</b>	<b>DESCRIPTION</b>	<b>DECODE</b>
GPIO_EN	15:8	GPIO port enable control.  Bit 15 = GPIO 7 Bit 14 = GPIO 6 Bit 13 = GPIO 5 Bit 12 = GPIO 4 Bit 11 = GPIO 3 Bit 10 = GPIO 2 Bit 9 = GPIO 1 Bit 8 = GPIO 0	0: GPIO port disabled 1: GPIO port enabled
GPIO_DIR	7:0	GPIO port direction control.  Bit 7 = GPIO 7 Bit 6 = GPIO 6 Bit 5 = GPIO 5 Bit 4 = GPIO 4 Bit 3 = GPIO 3 Bit 2 = GPIO 2 Bit 1 = GPIO 1 Bit 0 = GPIO 0	0: Input mode 1: Output mode

**GPIO Data (0xC)**

<b>BIT</b>	<b>15</b>	<b>14</b>	<b>13</b>	<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>
<b>Field</b>	GPO_DATA[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>Field</b>	GPI_DATA[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Read Only							

BITFIELD	BITS	DESCRIPTION
GPO_DATA	15:8	Data to be driven by output-configured GPIO ports.  Bit 15 = GPIO 7 Bit 14 = GPIO 6 Bit 13 = GPIO 5 Bit 12 = GPIO 4 Bit 11 = GPIO 3 Bit 10 = GPIO 2 Bit 9 = GPIO 1 Bit 8 = GPIO 0
GPI_DATA	7:0	Data detected at the input-configured GPIO ports.  Bit 7 = GPIO 7 Bit 6 = GPIO 6 Bit 5 = GPIO 5 Bit 4 = GPIO 4 Bit 3 = GPIO 3 Bit 2 = GPIO 2 Bit 1 = GPIO 1 Bit 0 = GPIO 0

**GPI Edge Detection Control (0xD)**

<b>BIT</b>	<b>15</b>	<b>14</b>	<b>13</b>	<b>12</b>	<b>11</b>	<b>10</b>	<b>9</b>	<b>8</b>
<b>Field</b>	GPI_POS_EDGE_INT[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							
<b>BIT</b>	<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>Field</b>	GPI_NEG_EDGE_INT[7:0]							
<b>Reset</b>	0x00							
<b>Access Type</b>	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
GPI_POS_E DGE_INT	15:8	Positive edge detection control. When set, enables the detection of rising edges on the corresponding input-configured GPIO port.  Bit 15 = GPIO 7 Bit 14 = GPIO 6 Bit 13 = GPIO 5 Bit 12 = GPIO 4 Bit 11 = GPIO 3 Bit 10 = GPIO 2 Bit 9 = GPIO 1 Bit 8 = GPIO 0	0: Positive edge detection disabled 1: Positive edge detection enabled
GPI_NEG_E DGE_INT	7:0	Negative edge detection control. When set, enables the detection of falling edges on the corresponding input-configured GPIO port.  Bit 7 = GPIO 7 Bit 6 = GPIO 6 Bit 5 = GPIO 5 Bit 4 = GPIO 4 Bit 3 = GPIO 3 Bit 2 = GPIO 2 Bit 1 = GPIO 1 Bit 0 = GPIO 0	0: Negative edge detection disabled 1: Negative edge detection enabled

**GPI Edge Detection Status (0xE)**

BIT	15	14	13	12	11	10	9	8
Field	GPI_POS_EDGE_INT_STA[7:0]							
Reset	0x00							
Access Type	Read Clears All							
BIT	7	6	5	4	3	2	1	0
Field	GPI_NEG_EDGE_INT_STA[7:0]							
Reset	0x00							
Access Type	Read Clears All							



BITFIELD	BITS	DESCRIPTION	DECODE
GPI_POS_E DGE_INT_S TA	15:8	<p>Positive edge detection status. When asserted, indicates that at least one rising edge was detected on the corresponding input-configured GPIO port.</p> <p>Cleared when read.</p> <p>Bit 15 = GPIO 7                      Bit 14 = GPIO 6                      Bit 13 = GPIO 5                      Bit 12 = GPIO 4                      Bit 11 = GPIO 3                      Bit 10 = GPIO 2                      Bit 9 = GPIO 1                      Bit 8 = GPIO 0</p>	<p>0: No positive edge was detected                      1: At least one positive edge was detected</p>
GPI_NEG_E DGE_INT_S TA	7:0	<p>Negative edge detection status. When asserted, indicates that at least one falling edge was detected on the corresponding input-configured GPIO port.</p> <p>Cleared when read.</p> <p>Bit 7 = GPIO 7                      Bit 6 = GPIO 6                      Bit 5 = GPIO 5                      Bit 4 = GPIO 4                      Bit 3 = GPIO 3                      Bit 2 = GPIO 2                      Bit 1 = GPIO 1                      Bit 0 = GPIO 0</p>	<p>0: No negative edge was detected                      1: At least one negative edge was detected</p>

## Applications Information

### Single High-Voltage Supply

The MAX22007 is designed to operate with a single positive high-voltage supply (i.e., HVSS is connected to GND). In this case, the linear output-voltage range starts at 300mV above GND\_ and the linear output-current range starts at 1.5mA. If performance to all specifications including an output voltage down to 20mV or output current down to 40 $\mu$ A is required, then a negative high-voltage supply  $V_{HVSS}$  of -2V must be applied.

### Power-Supply Sequencing

The two power supply pairs of the MAX22007 ( $V_{DD}/GND$  and  $HVDD/HVSS$ ) can be powered up in any sequence. Likewise, the positive and negative high-voltage supplies HVDD and HVSS (if HVSS is chosen not to be at the same potential as GND) can be powered up in any sequence.

### Power-Supply Decoupling

To reduce ripple and the chance of introducing signal or data errors, bypass  $V_{DD}$  and  $HVDD$  with a 1 $\mu$ F low-ESR ceramic capacitor to GND respectively, and place the bypass capacitor as close to the  $V_{DD}$  and  $HVDD$  pins as possible. If a negative high-voltage supply is required, bypass HVSS with a 1 $\mu$ F low-ESR ceramic capacitor to GND and place the bypass capacitor as close to the HVSS pin as possible.

### PCB Layout Recommendations

The PCB designer should follow some critical recommendations in order to get the best performance from the MAX22007.

- Use proper grounding techniques such as a multilayer board with low-inductance ground planes.
- Connect all GND and GND\_ pins to the GND plane on the PCB.
- Use ground plane shielding to improve noise immunity.
- Keep analog signal traces away from digital signal traces, especially clock traces.
- Connect the exposed pad on the bottom of the MAX22007 to HVSS.
- Maximize the metal coverage for all layers, especially for top and bottom layer to optimize the heat dissipation.
- Maximize the number of vias under the package for thermal purposes. If possible, fill the via with copper, which further enhances the vertical heat transfer through the PCB.
- Package stress needs to be minimized to ensure the output accuracy.

For a detailed recommended layout, refer to the MAX22007 EV kit data sheet.

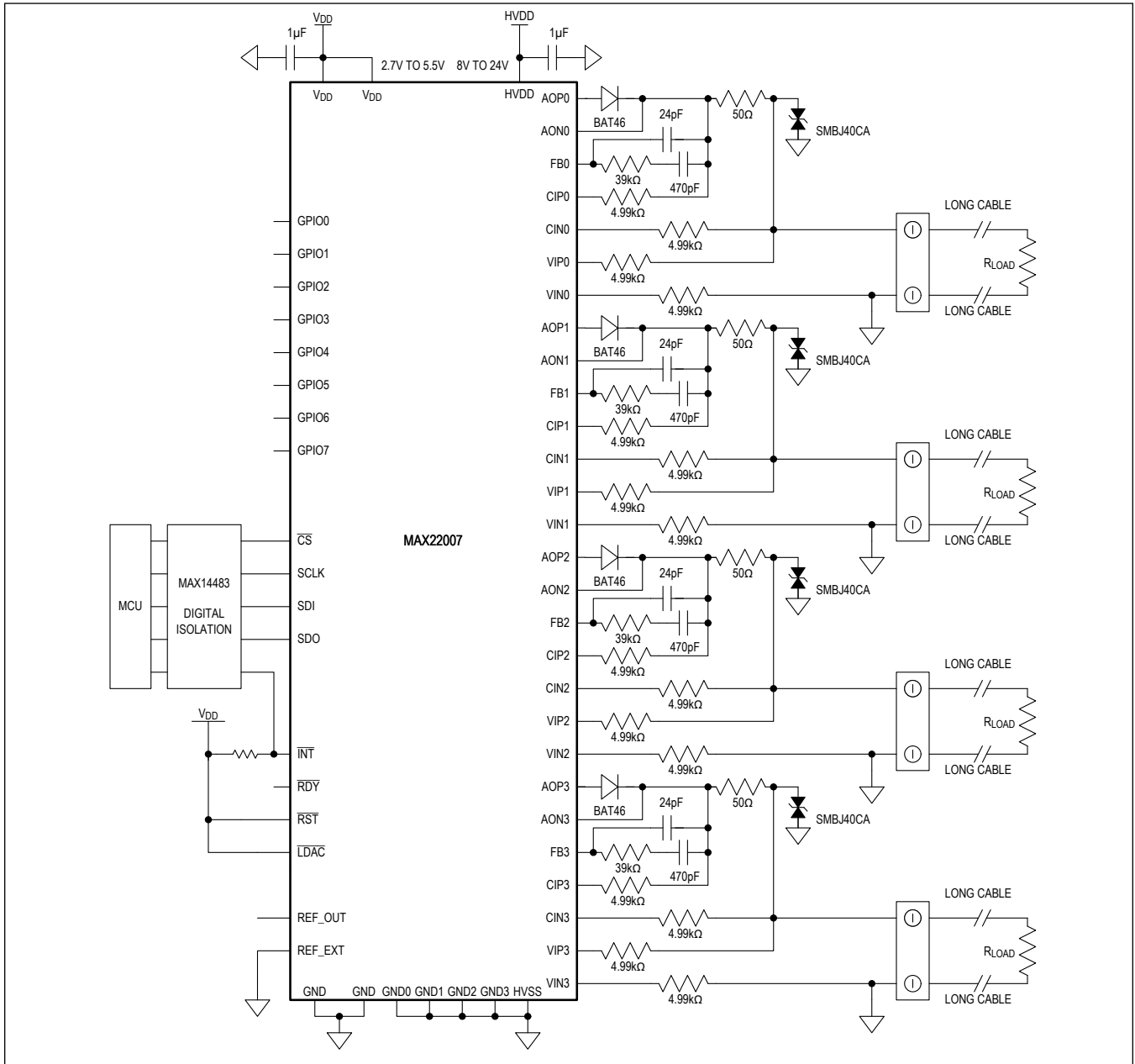
### Surge Protection

With external circuitry, the input and output pins are protected against  $\pm 1\text{kV}/42\Omega$  line-to-line or line-to-ground surge pulses as per IEC 61000-4-5. Place a 40V bidirectional TVS between the outputs and GND, after the AOP\_ diode and after the 50 $\Omega$  current-sense resistor. Place a minimum 4.99k $\Omega$  resistor in series with each input pin (CIN\_, CIP\_, VIN\_, and VIP\_) at risk.

All other MAX22007 pins are rated for  $\pm 2.5\text{kV}$  Human Body Model (HBM) ESD. If surge voltages can couple to the supply rails (HVDD or HVSS), a unidirectional TVS is recommended to be placed on the HVDD or HVSS pins, respectively.

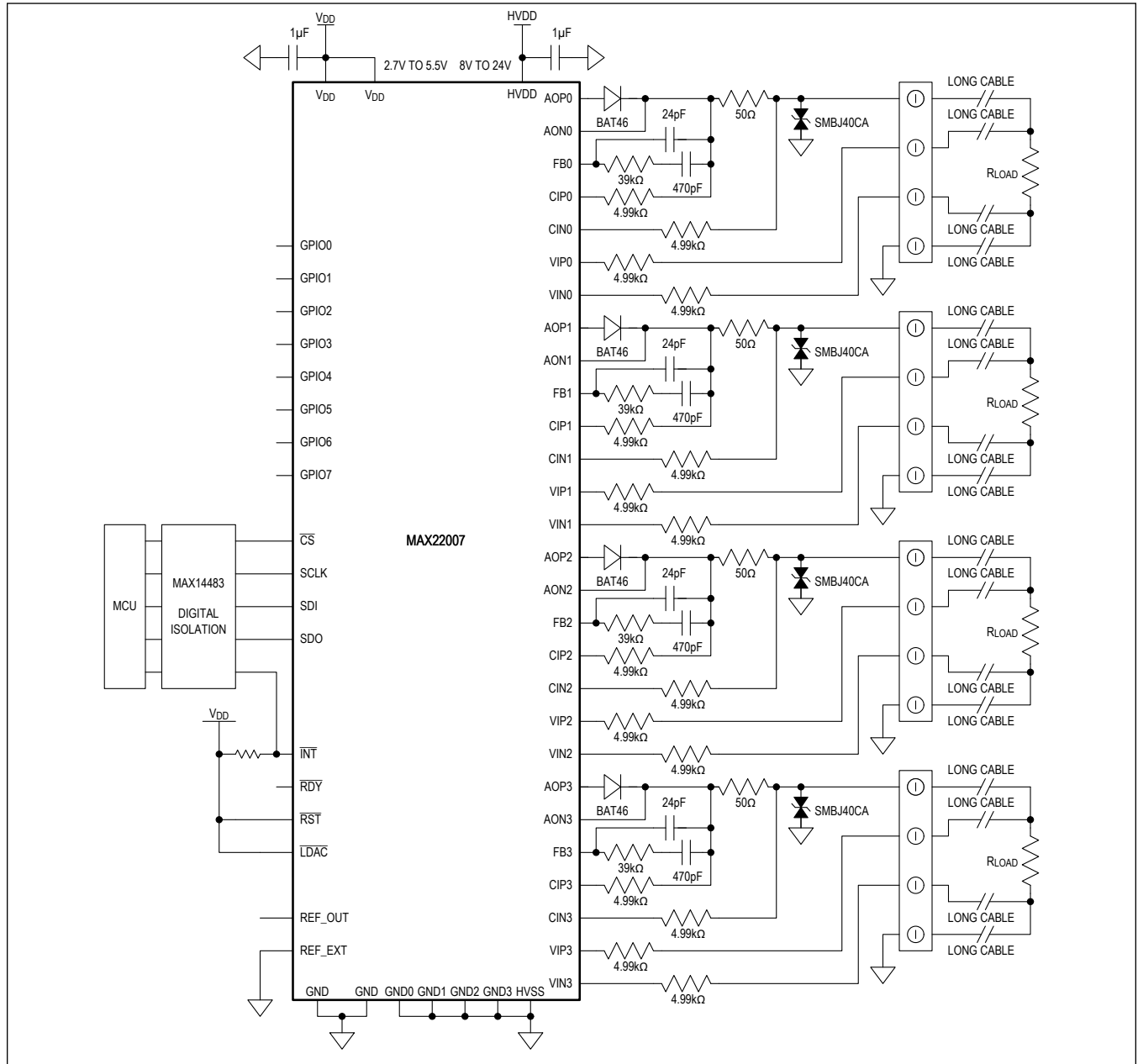
Typical Application Circuits

Two-Wire Application Circuit



Typical Application Circuits (continued)

Four-Wire Application Circuit



MAX22007

Four-Channel 12-Bit  
Configurable Analog Output with  
Integrated Voltage Reference

Ordering Information

PART	TEMP RANGE	PIN PACKAGE
MAX22007ETN+	-40°C to +85°C	56 TQFN-EP*
MAX22007ETN+T	-40°C to +85°C	56 TQFN-EP*

+ Denotes lead(Pb)-free/RoHS-compliance.

T = Tape-and-reel.

\*EP = Exposed pad.

**Revision History**

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/20	Release for Market Intro	—
1	11/20	Added TOC17 and TOC39, and renumbered subsequent TOCs; updated the Revision ID (0x00) register	11, 14, 28–29

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at <https://www.maximintegrated.com/en/storefront/storefront.html>.

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