MAX5854 Dual, 10-Bit, 165Msps, Current-Output DAC

General Description

The MAX5854 dual, 10-bit, 165Msps digital-to-analog converter (DAC) provides superior dynamic performance in wideband communication systems. The device integrates two 10-bit DAC cores, and a 1.24V reference. The MAX5854 supports single-ended and differential modes of operation. The dynamic performance is maintained over the entire 2.7V to 3.6V power-supply operating range. The analog outputs support a -1.0V to +1.25V compliance voltage.

The MAX5854 can operate in interleaved data mode to reduce the I/O pin count. This allows the converter to be updated on a single, 10-bit bus.

The MAX5854 features digital control of channel gain matching to within ±0.4dB in sixteen 0.05dB steps. Channel matching improves sideband suppression in analog quadrature modulation applications. The on-chip 1.24V bandgap reference includes a control amplifier that allows external full-scale adjustments of both channels through a single resistor. The internal reference can be disabled and an external reference can be applied for high-accuracy applications.

The MAX5854 features full-scale current outputs of 2mA to 20mA and operates from a 2.7V to 3.6V single supply. The DAC supports three modes of power-control operation: normal, low-power standby, and complete power-down. In power-down mode, the operating current is reduced to 1µA.

The MAX5854 is packaged in a 40-pin TQFN with exposed paddle (EP) and is specified for the extended (-40°C to +85°C) temperature range.

Pin-compatible, lower speed, and lower resolution versions are also available. Refer to the MAX5853 (10-bit, 80Msps), the MAX5852 (8-bit, 165Msps), and the MAX5851 (8-bit, 80Msps) data sheets for more information. See Table 4 at the end of the data sheet.

Applications

- Communications
  SatCom, LMDS, MMDS, HFC, DSL, WLAN, Point-to-Point Microwave Links
- Wireless Base Stations
- Quadrature Modulation
- Direct Digital Synthesis (DDS)
- Instrumentation/ATE

Features

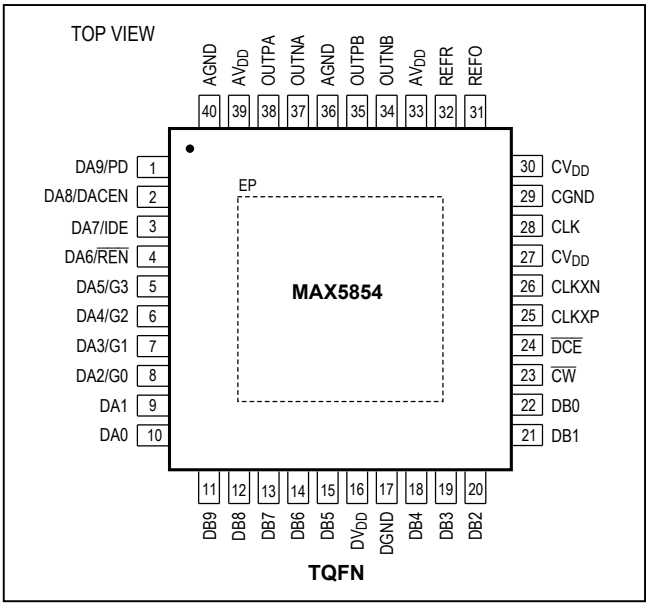
- 10-Bit, 165Msps Dual DAC
- Low Power
  - 190mW with I_{FS} = 20mA at f_{CLK} = 165MHz
- 2.7V to 3.6V Single Supply
- Full Output Swing and Dynamic Performance at 2.7V Supply
- Superior Dynamic Performance
  - 73dBc SFDR at f_{OUT} = 40MHz
  - UMTS ACLR = 65.5dB at f_{OUT} = 30.7MHz
- Programmable Channel Gain Matching
- Integrated 1.24V Low-Noise Bandgap Reference
- Single-Resistor Gain Control
- Interleaved Data Mode
- Single-Ended and Differential Clock Input Modes
- Miniature 40-Pin TQFN Package, 6mm x 6mm
- EV Kit Available—MAX5854 EV Kit

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5854ETL	-40°C to +85°C	40 Thin QFN-EP*

**EP = Exposed paddle.*

Pin Configuration



Absolute Maximum Ratings

AV_{DD}, DV_{DD}, CV_{DD} to AGND, DGND, CGND .....-0.3V to +4V
DA9–DA0, DB9–DB0, $\overline{CW}$, $\overline{DCE}$ to AGND,
DGND, CGND .....-0.3V to +4V
CLKXN, CLKXP to CGND.....-0.3V to +4V
OUTP_, OUTN_ to AGND.....-1.25V to (AV_{DD} + 0.3V)
CLK to DGND.....-0.3V to (DV_{DD} + 0.3V)
REFR, REFO to AGND .....-0.3V to (AV_{DD} + 0.3V)
AGND to DGND, DGND to CGND,
AGND to CGND.....-0.3V to +0.3V
Maximum Current into Any Pin
(excluding power supplies).....±50mA
Continuous Power Dissipation (T_A = +70°C)
40-Pin TQFN-EP (derate 23.3mW/°C
above +70°C) 1.860W
Operating Temperature Range..... -40°C to +85°C
Storage Temperature Range..... -65°C to +150°C
Junction Temperature.....+150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(AV_{DD} = DV_{DD} = CV_{DD} = 3V, AGND = DGND = CGND = 0, f_{DAC} = 165Msps, differential clock, external reference, V_{REF} = 1.2V, I_{FS} = 20mA, output amplitude = 0dB FS, differential output, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A ≥ +25°C guaranteed by production test. T_A < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			10			Bits
Integral Nonlinearity	INL	R_L = 0		-1.0	±0.25	+1.0	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic, R_L = 0		-0.5	±0.2	+0.5	LSB
Offset Error	V_{OS}			-0.5	±0.1	+0.5	LSB
Gain Error (See Also *Gain Error Definition* Section)	GE	Internal reference (Note1)		-11.0	±1.5	+6.8	%FSR
		External reference		-6.25	±0.7	+4.10	
Gain-Error Temperature Drift		Internal reference			±150		ppm/°C
		External reference			±100		
DYNAMIC PERFORMANCE							
Spurious-Free Dynamic Range to Nyquist	SFDR	f_{CLK} = 165MHz, A_{OUT} = -1dBFS	f_{OUT} = 10MHz	69.4	78		dBc
			f_{OUT} = 20MHz		77		
			f_{OUT} = 40MHz		73		
		f_{CLK} = 100MHz, A_{OUT} = -1dBFS	f_{OUT} = 10MHz		77		
			f_{OUT} = 20MHz		77		
			f_{OUT} = 30MHz		76		
		f_{CLK} = 25MHz, A_{OUT} = -1dBFS	f_{OUT} = 1MHz		79		
Spurious-Free Dynamic Range Within a Window	SFDR	f_{CLK} = 165MHz, f_{OUT} = 10MHz, A_{OUT} = -1dBFS, span = 10MHz			83		dBc
		f_{CLK} = 100MHz, f_{OUT} = 5MHz, A_{OUT} = -1dBFS, span = 4MHz			84		
		f_{CLK} = 25MHz, f_{OUT} = 1MHz, A_{OUT} = -1dBFS, span = 2MHz			82		
Multitone Power Ratio to Nyquist	MTPR	8 tones at 400kHz spacing, f_{CLK} = 78MHz, f_{OUT} = 15MHz to 18.2MHz			74		dBc

Electrical Characteristics (continued)

(AV_{DD} = DV_{DD} = CV_{DD} = 3V, AGND = DGND = CGND = 0, f_{DAC} = 165Msps, differential clock, external reference, V_{REF} = 1.2V, I_{FS} = 20mA, output amplitude = 0dB FS, differential output, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A ≥ +25°C guaranteed by production test. T_A < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Multitone Spurious-Free Dynamic Range Within a Window		8 tones at 2.1MHz spacing, f_{CLK} = 165MHz, f_{OUT} = 28.3MHz to 45.2MHz, span = 50MHz			70		dBc
Adjacent Channel Power Ratio with UMTS	ACLR	f_{OUT} = 30.72MHz, RBW = 30kHz, f_{CLK} = 122.88MHz			65.5		dB
Total Harmonic Distortion to Nyquist (2nd- Through 8th-Order Harmonics Included)	THD	f_{CLK} = 165MHz, A_{OUT} = -1dBFS	f_{OUT} = 10MHz		-76		dBc
			f_{OUT} = 20MHz		-74		
			f_{OUT} = 40MHz		-71		
		f_{CLK} = 100MHz, A_{OUT} = -1dBFS	f_{OUT} = 10MHz		-75		
			f_{OUT} = 20MHz		-74		
			f_{OUT} = 30MHz		-73		
		f_{CLK} = 25MHz, A_{OUT} = -1dBFS	f_{OUT} = 1MHz		-76		
Output Channel-to-Channel Isolation		f_{OUT} = 10MHz			90		dB
Channel-to-Channel Gain Mismatch		f_{OUT} = 10MHz, G[3:0] = 1000			0.025		dB
Channel-to-Channel Phase Mismatch		f_{OUT} = 10MHz			0.05		Degrees
Signal-to-Noise Ratio to Nyquist	SNR	f_{CLK} = 165MHz, f_{OUT} = 10MHz, I_{FS} = 20mA			60.5		dB
		f_{CLK} = 165MHz, f_{OUT} = 10MHz, I_{FS} = 5mA			61		
		f_{CLK} = 65MHz, f_{OUT} = 10MHz, I_{FS} = 20mA			62		
		f_{CLK} = 65MHz, f_{OUT} = 10MHz, I_{FS} = 5mA			62		
Maximum DAC Conversion Rate	f_{DAC}	Interleaved mode disabled, IDE = 0		165	200		Msps
		Interleaved mode enabled, IDE = 1		82.5	100		
Glitch Impulse					5		pV-s
Output Settling Time	t_S	To ±0.1% error band (Note 3)			12		ns
Output Rise Time		10% to 90% (Note 3)			2.2		ns
Output Fall Time		90% to 10% (Note 3)			2.2		ns
ANALOG OUTPUT							
Full-Scale Output Current Range	I_{FS}			2		20	mA
Output Voltage Compliance Range				-1.00		+1.25	V
Output Leakage Current		Shutdown or standby mode		-5		+5	µA
REFERENCE							
Internal-Reference Output Voltage	V_{REFO}	$\overline{REN}$ = 0		1.13	1.24	1.32	V

Electrical Characteristics (continued)

(AV_{DD} = DV_{DD} = CV_{DD} = 3V, AGND = DGND = CGND = 0, f_{DAC} = 165Msps, differential clock, external reference, V_{REF} = 1.2V, I_{FS} = 20mA, output amplitude = 0dB FS, differential output, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A ≥ +25°C guaranteed by production test. T_A < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Internal-Reference Supply Rejection		AV_{DD} varied from 2.7V to 3.6V		0.5		mV/V
Internal-Reference Output-Voltage Temperature Drift	TCV_{REFO}	$\overline{REN}$ = 0		±50		ppm/°C
Internal-Reference Output Drive Capability		$\overline{REN}$ = 0		50		µA
External-Reference Input Voltage Range		$\overline{REN}$ = 1	0.10	1.2	1.32	V
Current Gain	I_{FS}/I_{REF}			32		mA/mA
LOGIC INPUTS (DA9–DA0, DB9–DB0, $\overline{CW}$)						
Digital Input-Voltage High	V_{IH}		0.65 x DV_{DD}			V
Digital Input-Voltage Low	V_{IL}				0.3 x DV_{DD}	V
Digital Input Current	I_{IN}		-1		+1	µA
Digital Input Capacitance	C_{IN}			3		pF
SINGLE-ENDED CLOCK INPUT/OUTPUT AND $\overline{DCE}$ INPUT (CLK, $\overline{DCE}$)						
Digital Input-Voltage High	V_{IH}	$\overline{DCE}$ = 1	0.65 x CV_{DD}			V
Digital Input-Voltage Low	V_{IL}	$\overline{DCE}$ = 1			0.3 x CV_{DD}	V
Digital Input Current	I_{IN}	$\overline{DCE}$ = 1	-1		+1	µA
Digital Input Capacitance	C_{IN}	$\overline{DCE}$ = 1		3		pF
Digital Output-Voltage High	V_{OH}	$\overline{DCE}$ = 0, I_{SOURCE} = 0.5mA, Figure 1	0.9 x CV_{DD}			V
Digital Output-Voltage Low	V_{OL}	$\overline{DCE}$ = 0, I_{SINK} = 0.5mA, Figure 1			0.1 x CV_{DD}	V
DIFFERENTIAL CLOCK INPUTS (CLKXP/CLKXN)						
Differential Clock Input Internal Bias				$CV_{DD}/2$		V
Differential Clock Input Swing			0.5			V
Clock Input Impedance		Measured single ended		5		kΩ
POWER REQUIREMENTS						
Analog Power-Supply Voltage	AV_{DD}		2.7	3	3.6	V
Digital Power-Supply Voltage	DV_{DD}		2.7	3	3.6	V
Clock Power-Supply Voltage	CV_{DD}		2.7	3	3.6	V

Electrical Characteristics (continued)

(AV_{DD} = DV_{DD} = CV_{DD} = 3V, AGND = DGND = CGND = 0, f_{DAC} = 165Msps, differential clock, external reference, V_{REF} = 1.2V, I_{FS} = 20mA, output amplitude = 0dB FS, differential output, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A ≥ +25°C guaranteed by production test. T_A < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Supply Current	I_{AVDD}	I_{FS} = 20mA (Note 2), single-ended clock mode			43.2	46	mA
		I_{FS} = 20mA (Note 2), differential clock mode			43.2		
		I_{FS} = 2mA (Note 2), single-ended clock mode			5		
		I_{FS} = 2mA (Note 2), differential clock mode			5		
Digital Supply Current	I_{DVDD}	I_{FS} = 20mA (Note 2), single-ended clock mode			6.2	7.5	mA
		I_{FS} = 20mA (Note 2), differential clock mode			6.2		
Clock Supply Current	I_{CVDD}	Single-ended clock mode ($\overline{DCE}$ = 1) (Note 2)			13.7	16.5	mA
		Differential clock mode ($\overline{DCE}$ = 0) (Note 2)			24		
Total Standby Current	$I_{STANDBY}$	I_{AVDD} + I_{DVDD}+ I_{CVDD}			3.1	3.7	mA
Total Shutdown Current	I_{SHDN}	I_{AVDD} + I_{DVDD} + I_{CVDD}			1		µA
Total Power Dissipation	P_{TOT}	Single-ended clock mode ($\overline{DCE}$ = 1)	I_{FS} = 20mA (Note 2)		190	210	mW
			I_{FS} = 2mA (Note 2)		75		
		Differential clock mode ($\overline{DCE}$ = 0)	I_{FS} = 20mA (Note 2)		220		
			I_{FS} = 2mA (Note 2)		106		
		Standby			9.3	11.1	
		Shutdown			0.003		
TIMING CHARACTERISTICS (Figure 5, Figure 6)							
Propagation Delay					1		Clock cycles
DAC Data to CLK Rise/Fall Setup Time	t_{DCS}	Single-ended clock mode ($\overline{DCE}$ = 1) (Note 4)		1.2			ns
		Differential clock mode ($\overline{DCE}$ = 0) (Note 4)		2.7			
DAC Data to CLK Rise/Fall Hold Time	t_{DCH}	Single-ended clock mode ($\overline{DCE}$ = 1) (Note 4)		0.8			ns
		Differential clock mode ($\overline{DCE}$ = 0) (Note 4)		-0.5			
Control Word to $\overline{CW}$ Rise Setup Time	t_{CS}			2.5			ns
Control Word to $\overline{CW}$ Rise Hold Time	t_{CW}			2.5			ns
$\overline{CW}$ High Time	t_{CWH}			5			ns
$\overline{CW}$ Low Time	t_{CWL}			5			ns
DACEN = 1 to V_{OUT} Stable Time (Coming Out of Standby)	t_{STB}				3		µs

Electrical Characteristics (continued)

(AV_{DD} = DV_{DD} = CV_{DD} = 3V, AGND = DGND = CGND = 0, f_{DAC} = 165Msps, differential clock, external reference, V_{REF} = 1.2V, I_{FS} = 20mA, output amplitude = 0dB FS, differential output, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. T_A ≥ +25°C guaranteed by production test. T_A < +25°C guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PD = 0 to V_{OUT} Stable Time (Coming Out of Power-Down)	t_{SHDN}			500		µs
Maximum Clock Frequency at CLKXP/CLKXN Input	f_{CLK}		165	200		MHz
Clock High Time	t_{CXH}	CLKXP or CLKXN input		1.5		ns
Clock Low Time	t_{CXL}	CLKXP or CLKXN input		1.5		ns
CLKXP Rise to CLK Output Rise Delay	t_{CDH}	$\overline{DCE}$ = 0		2.7		ns
CLKXP Fall to CLK Output Fall Delay	t_{CDL}	$\overline{DCE}$ = 0		2.7		ns

Note 1: Including the internal reference voltage tolerance and reference amplifier offset.
Note 2: f_{DAC} = 165Msps, f_{OUT} = 10MHz.
Note 3: Measured single-ended with 50Ω load and complementary output connected to AGND.
Note 4: Guaranteed by design, not production tested.

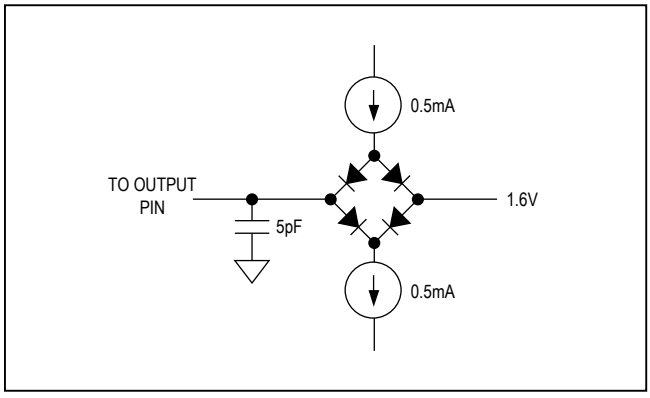
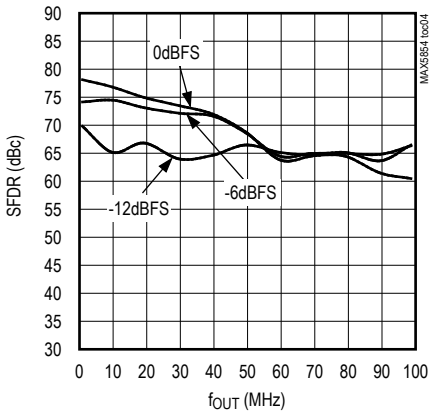


Figure 1. Load Test Circuit for CLK Outputs

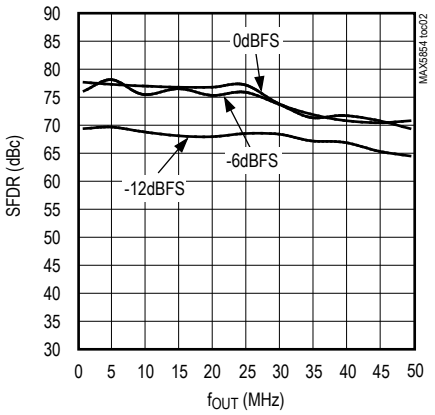
Typical Operating Characteristics

(AV_{DD} = DV_{DD} = CV_{DD} = 3V, AGND = DGND = CGND = 0, external reference, differential clock, I_{FS} = 20mA, differential output, T_A = +25°C, unless otherwise noted.)

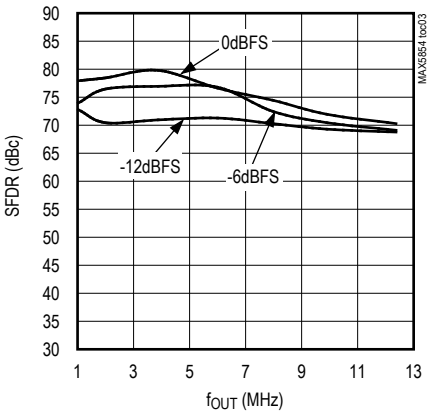
SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY (f_{CLK} = 200MHz)



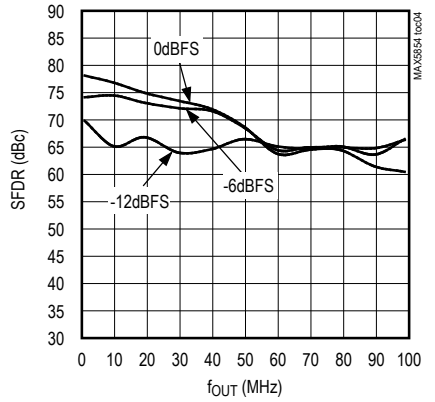
SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY (f_{CLK} = 100MHz)



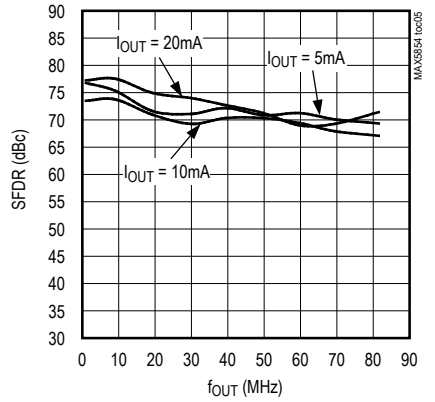
SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY (f_{CLK} = 25MHz)



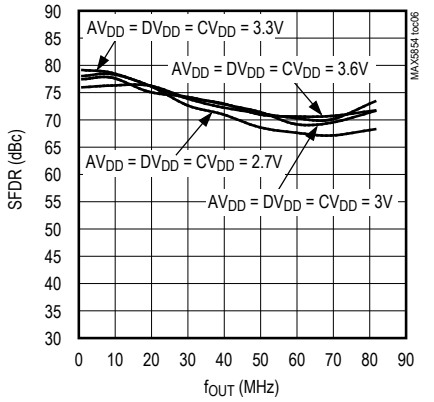
SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY (f_{CLK} = 200MHz)



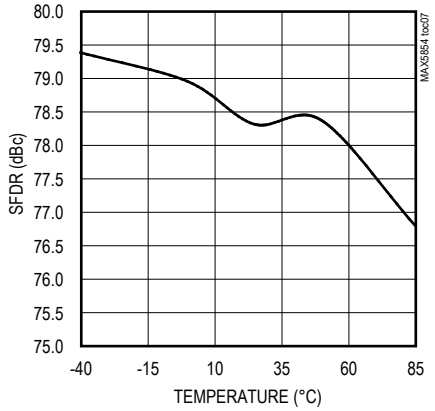
SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY (f_{CLK} = 165MHz)



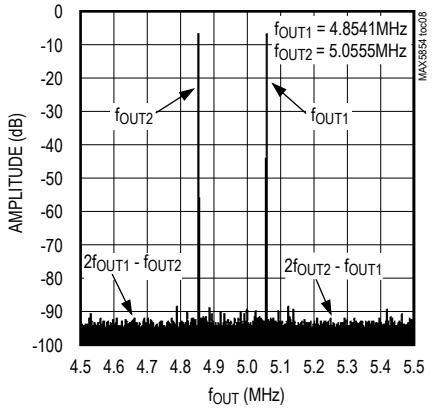
SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY (f_{CLK} = 165MHz)



SFDR vs. TEMPERATURE (f_{CLK} = 165MHz, f_{OUT} = 10MHz, A_{OUT} = 0dBFS)



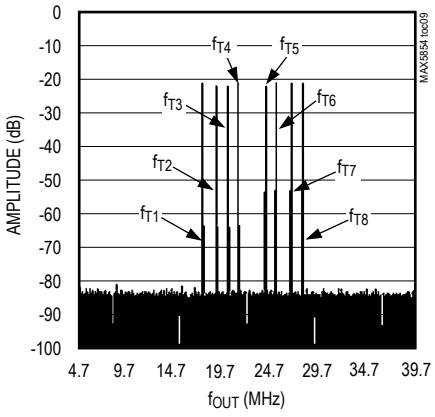
TWO-TONE INTERMODULATION DISTORTION (f_{CLK} = 165MHz, 1MHz WINDOW)



Typical Operating Characteristics (continued)

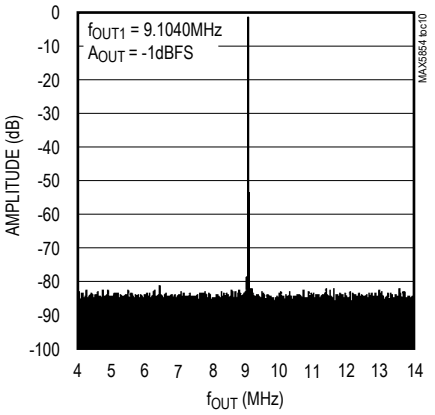
(AV_{DD} = DV_{DD} = CV_{DD} = 3V, AGND = DGND = CGND = 0, external reference, differential clock, I_{FS} = 20mA, differential output, T_A = +25°C, unless otherwise noted.)

8-TONE SFDR PLOT (f_{CLK} = 165MHz, 35MHz WINDOW)

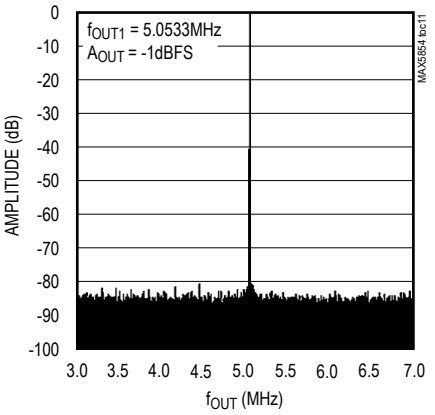


f_{T1} = 17.493MHz
f_{T2} = 18.997MHz
f_{T3} = 20.200MHz
f_{T4} = 21.253MHz
f_{T5} = 24.035MHz
f_{T6} = 25.087MHz
f_{T7} = 26.741MHz
f_{T8} = 27.869MHz

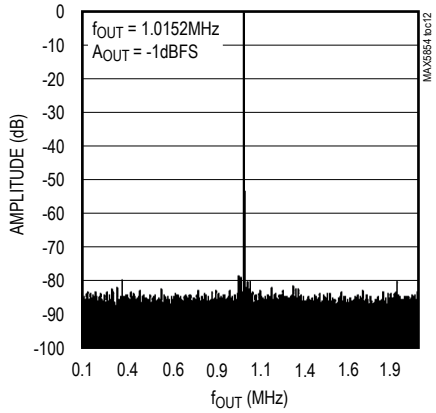
SINGLE-TONE SFDR (f_{CLK} = 165MHz, 10MHz WINDOW)



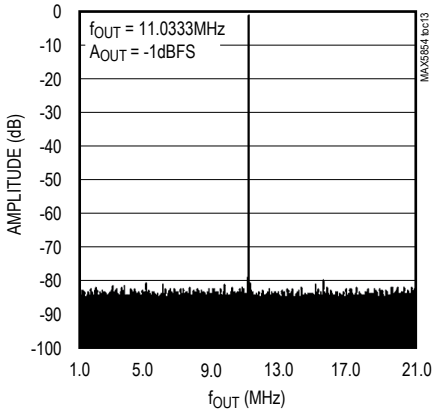
SINGLE-TONE SFDR (f_{CLK} = 100MHz, 4MHz WINDOW)



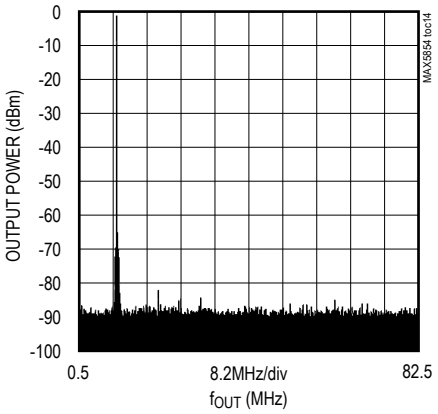
SINGLE-TONE SFDR (f_{CLK} = 25MHz, 2MHz WINDOW)



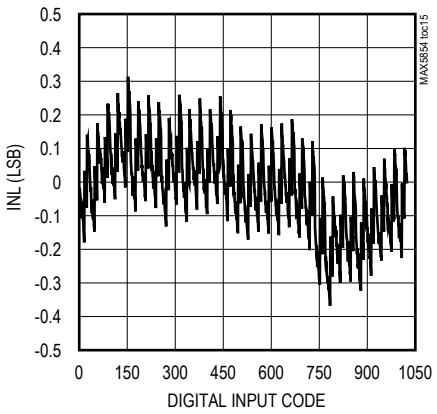
SINGLE-TONE SFDR (f_{CLK} = 78MHz, 20MHz WINDOW)



SINGLE-TONE FFT PLOT (f_{CLK} = 165MHz, f_{OUT} = 10MHz, A_{OUT} = 0dBFS, NYQUIST WINDOW)



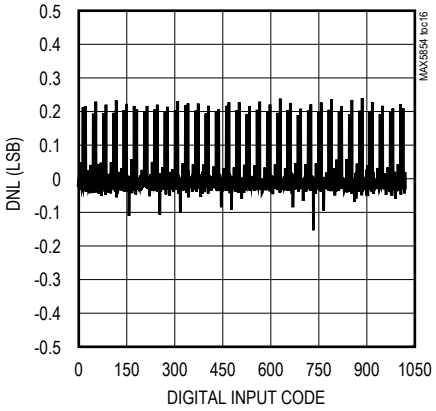
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



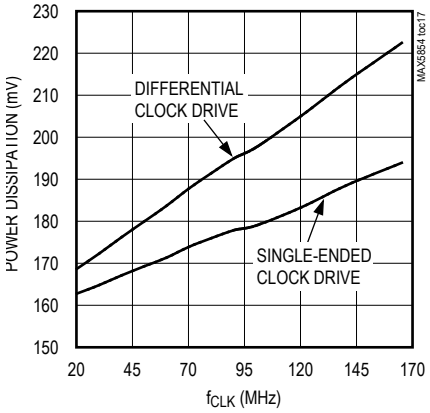
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = CV_{DD} = 3V, AGND = DGND = CGND = 0, external reference, differential clock, I_{FS} = 20mA, differential output, T_A = +25°C, unless otherwise noted.)

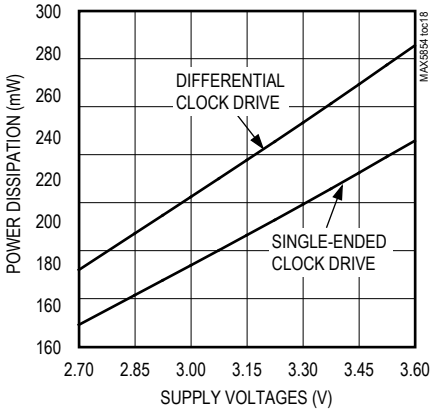
DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



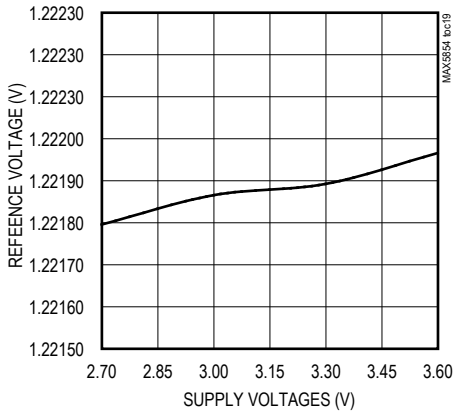
POWER DISSIPATION vs. CLOCK FREQUENCY (f_{OUT} = 10MHz, A_{OUT} = 0dBFS)



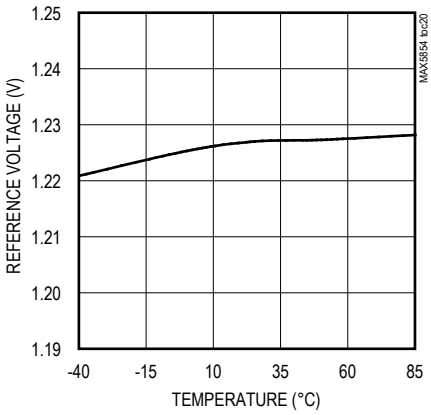
POWER DISSIPATION vs. SUPPLY VOLTAGES (f_{CLK} = 165MHz, f_{OUT} = 10MHz)



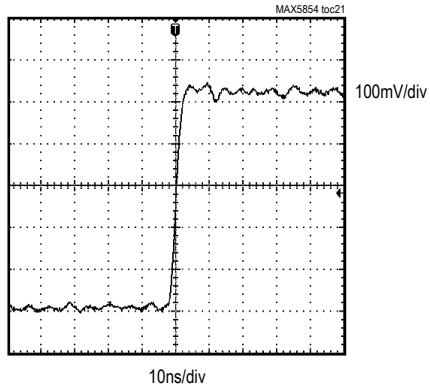
REFERENCE VOLTAGE vs. SUPPLY VOLTAGES (f_{CLK} = 165MHz, f_{OUT} = 10MHz)



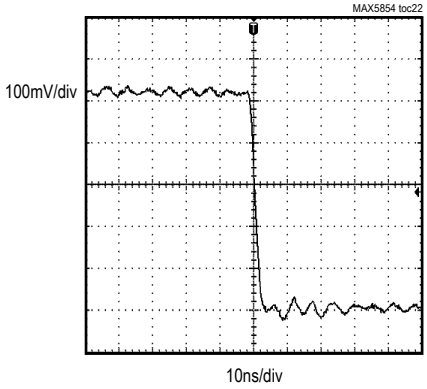
REFERENCE VOLTAGE vs. TEMPERATURE



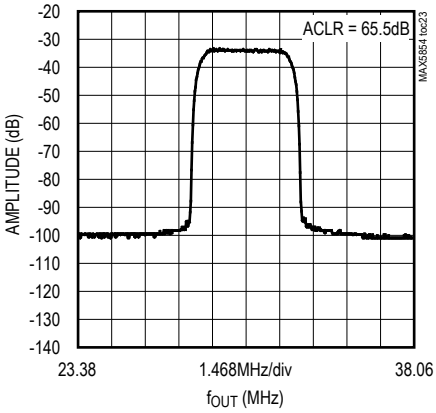
DYNAMIC RESPONSE RISE TIME



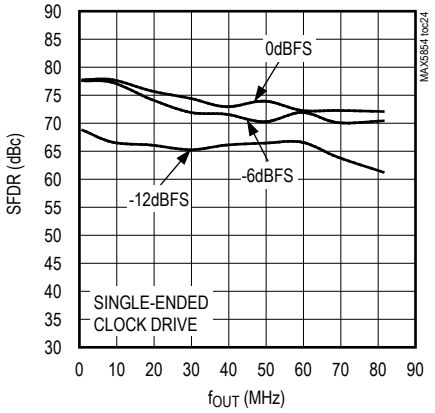
DYNAMIC RESPONSE FALL TIME



ACLR PLOT (f_{CLK} = 122.88MHz, f_{OUT} = 30.72MHz)



SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY (f_{CLK} = 165MHz)



Pin Description

PIN	NAME	FUNCTION
1	DA9/PD	Channel A Input Data Bit 9 (MSB)/Power-Down
2	DA8/DACEN	Channel A Input Data Bit 8/DAC Enable Control
3	DA7/IDE	Channel A Input Data Bit 7/Interleaved Data Enable
4	DA6/$\overline{REN}$	Channel A Input Data Bit 6/Reference Enable. Setting $\overline{REN}$ = 0 enables the internal reference. Setting $\overline{REN}$ = 1 disables the internal reference.
5	DA5/G3	Channel A Input Data Bit 5/Channel A Gain Adjustment Bit 3
6	DA4/G2	Channel A Input Data Bit 4/Channel A Gain Adjustment Bit 2
7	DA3/G1	Channel A Input Data Bit 3/Channel A Gain Adjustment Bit 1
8	DA2/G0	Channel A Input Data Bit 2/Channel A Gain Adjustment Bit 0
9	DA1	Channel A Input Data Bit 1
10	DA0	Channel A Input Data Bit 0 (LSB)
11	DB9	Channel B Input Data Bit 9 (MSB)
12	DB8	Channel B Input Data Bit 8
13	DB7	Channel B Input Data Bit 7
14	DB6	Channel B Input Data Bit 6
15	DB5	Channel B Input Data Bit 5
16	DV_{DD}	Digital Power Input. See the *Power Supplies, Bypassing, Decoupling, and Layout* section for more details.
17	DGND	Digital Ground
18	DB4	Channel B Input Data Bit 4
19	DB3	Channel B Input Data Bit 3
20	DB2	Channel B Input Data Bit 2
21	DB1	Channel B Input Data Bit 1
22	DB0	Channel B Input Data Bit 0 (LSB)
23	$\overline{CW}$	Active-Low Control Word Write Pulse. The control word is latched on the rising edge of $\overline{CW}$.
24	$\overline{DCE}$	Active-Low Differential Clock Enable Input. Drive $\overline{DCE}$ low to enable the differential clock inputs CLKXP and CLKXN. Drive $\overline{DCE}$ high to disable the differential clock inputs and enable the single-ended CLK input.
25	CLKXP	Positive Differential Clock Input. With $\overline{DCE}$ = 0, CLKXP and CLKXN are enabled. With $\overline{DCE}$ = 1, CLKXP and CLKXN are disabled. Connect CLKXP to CGND when the differential clock is disabled.
26	CLKXN	Negative Differential Clock Input. With $\overline{DCE}$ = 0, CLKXP and CLKXN are enabled. With $\overline{DCE}$ = 1, CLKXP and CLKXN are disabled. Connect CLKXN to CV_{DD} when the differential clock is disabled.
27, 30	CV_{DD}	Clock Power Input. See the *Power Supplies, Bypassing, Decoupling, and Layout* section for more details.
28	CLK	Single-Ended Clock Input/Output. With the differential clock disabled ($\overline{DCE}$ = 1), CLK becomes a single-ended conversion clock input. With the differential clock enabled ($\overline{DCE}$ = 0), CLK is a single-ended output that mirrors the differential clock inputs CLKXP and CLKXN. See the *Clock Modes* section for more information on CLK.
29	CGND	Clock Ground
31	REFO	Reference Input/Output. REFO serves as a reference input when the internal reference is disabled. If the internal 1.24V reference is enabled, REFO serves as an output for the internal reference. When the internal reference is enabled, bypass REFO to AGND with a 0.1µF capacitor

Pin Description (continued)

PIN	NAME	FUNCTION
32	REFR	Full-Scale Current Adjustment. To set the output full-scale current, connect an external resistor RSET between REFR and AGND. The output full-scale current is equal to 32 x V_{REFO}/R_{SET}.
33, 39	AV_{DD}	Analog Power Input. See the *Power Supplies, Bypassing, Decoupling, and Layout* section for more details.
34	OUTNB	Channel B Negative Analog Current Output
35	OUTPB	Channel B Positive Analog Current Output
36, 40	AGND	Analog Ground
37	OUTNA	Channel A Negative Analog Current Output
38	OUTPA	Channel A Positive Analog Current Output
—	EP	Exposed Paddle. Connect EP to the common point of all ground planes.

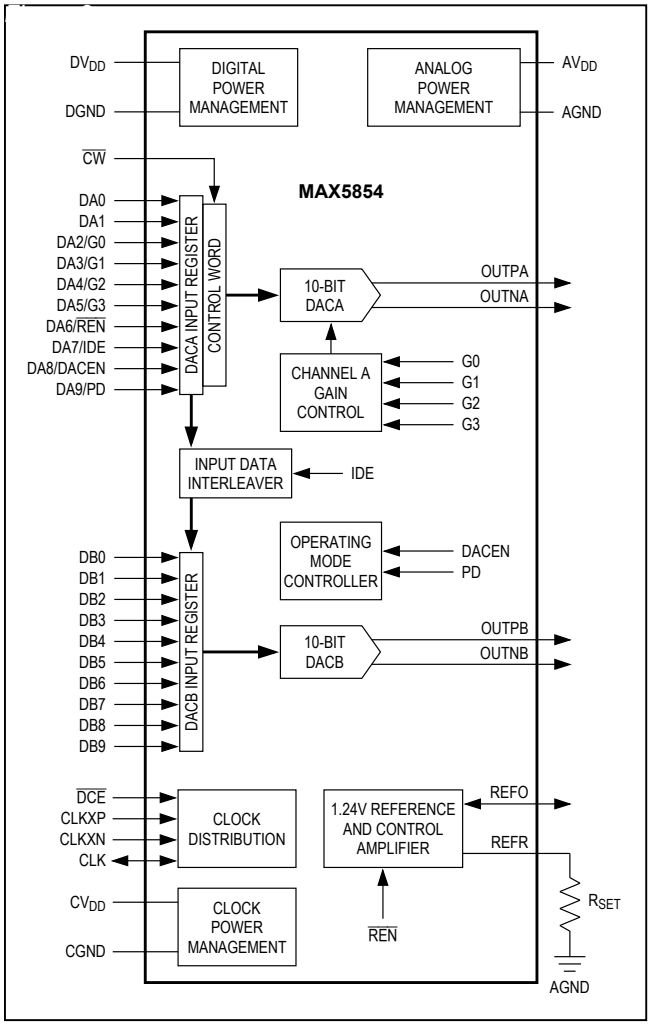


Figure 2. Simplified Diagram

Detailed Description

The MAX5854 dual, high-speed, 10-bit, current-output DAC provides superior performance in communication systems requiring low-distortion analog-signal reconstruction. The MAX5854 combines two DACs and an on-chip 1.24V reference (Figure 2). The current outputs of the DACs can be configured for differential or single-ended operation. The full-scale output current range is adjustable from 2mA to 20mA to optimize power dissipation and gain control.

The MAX5854 accepts an input data and a DAC conversion rate of 165MHz. The inputs are latched on the rising edge of the clock whereas the output latches on the following rising edge.

The MAX5854 features three modes of operation: normal, standby, and power-down (Table 2). These modes allow efficient power management. In power-down, the MAX5854 consumes only 1µA of supply current. Wake-up time from standby mode to normal DAC operation is 3µs.

Programming the DAC

An 8-bit control word routed through channel A's data port programs the gain matching, reference, and the operational mode of the MAX5854. The control word is latched on the rising edge of $\overline{CW}$. $\overline{CW}$ is independent of the DAC clock. The DAC clock can always remain running, when the control word is written to the DAC. Table 1 and Table 2 represent the control word format and function.

The gain on channel A can be adjusted to achieve gain matching between two channels in a user's system. The gain on channel A can be adjusted from -0.4dB to 0.35dB in steps of 0.05dB by using bits G3 to G0 (Table 3).

Table 1. Control Word Format and Function

MSB									LSB
PD	DACEN	IDE	$\overline{REN}$	G3	G2	G1	G0	X	X

CONTROL WORD	FUNCTION
PD	Power-Down. The part enters power-down mode if PD = 1.
DACEN	DAC Enable. When DACEN = 0 and PD = 0, the part enters standby mode.
IDE	Interleaved Data Mode. IDE = 1 enables the interleaved data mode. In this mode, digital data for both channels is applied through channel A in a multiplexed fashion. Channel B data is written on the falling edge of the clock signal and channel A data is written on the rising edge of the clock signal.
$\overline{REN}$	Reference Enable Bit. $\overline{REN}$ = 0 activates the internal reference. $\overline{REN}$ = 1 disables the internal reference and requires the user to apply an external reference between 0.1V to 1.32V.
G3	Bit 3 (MSB) of Gain Adjust Word
G2	Bit 2 of Gain Adjust Word
G1	Bit 1 of Gain Adjust Word
G0	Bit 0 (LSB) of Gain Adjust Word

Table 2. Configuration Modes

MODE	PD	DACEN	IDE	$\overline{REN}$
Normal operation; noninterleaved inputs; internal reference active	0	1	0	0
Normal operation; noninterleaved inputs; internal reference disabled	0	1	0	1
Normal operation; interleaved inputs; internal reference disabled	0	1	1	1
Standby	0	0	X	X
Power-down	1	X	X	X
Power-up	0	1	X	X

X = Don't care.

Table 3. Gain Difference Setting

GAIN ADJUSTMENT ON CHANNEL A (dB)	G3	G2	G1	G0
+0.4	0	0	0	0
0	1	0	0	0
-0.35	1	1	1	1

Device Power-Up and States of Operation

At power-up, the MAX5854's default configuration is internal reference noninterleaved input mode with a gain of 0dB and a fully operational converter. In shutdown, the MAX5854 consumes only 1µA of supply current, and in standby the current consumption is 3.1mA. Wake-up time from standby mode to normal operation is 3µs.

Clock Modes

The MAX5854 allows both single-ended CMOS and differential clock mode operation, and supports update rates of up to 165Msps. These modes are selected through an active-low control line called $\overline{DCE}$. In single-ended clock mode ($\overline{DCE}$ = 1), the CLK pin functions as an input, which accepts a user-provided single-ended clock signal. Data is written to the converter on the rising edge of the clock. The DAC outputs (previous data) are updated simultaneously on the same edge.

If the $\overline{DCE}$ pin is pulled low, the MAX5854 will operate in differential clock mode. In this mode, the clock signal has to be applied to differential clock input pins CLKXP/CLKXN. The differential input accepts an input range of ≥0.5V_{P-P} and a common-mode range of 1V to (CV_{DD} - 0.5V), making the part ideal for low-input amplitude clock drives. CLKXP/CLKXN also help to minimize the jitter, and allow the user to connect a crystal oscillator directly to MAX5854.

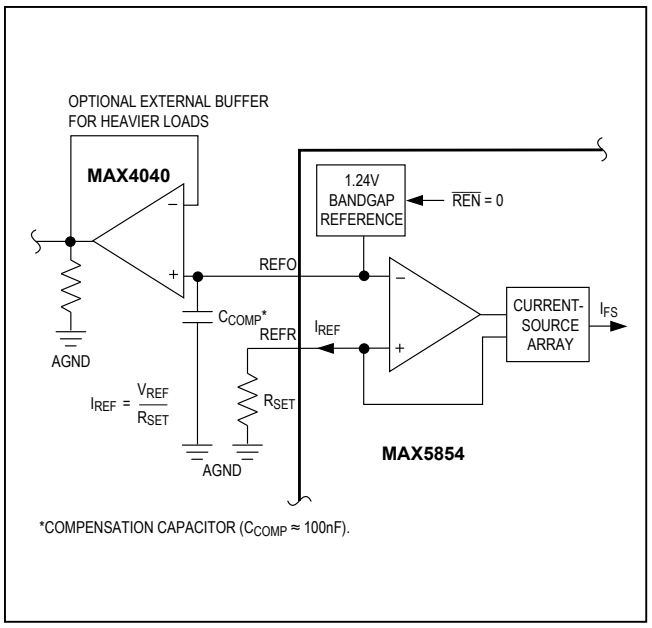


Figure 3. Setting I_{FS} with the Internal 1.24V Reference and the Control Amplifier

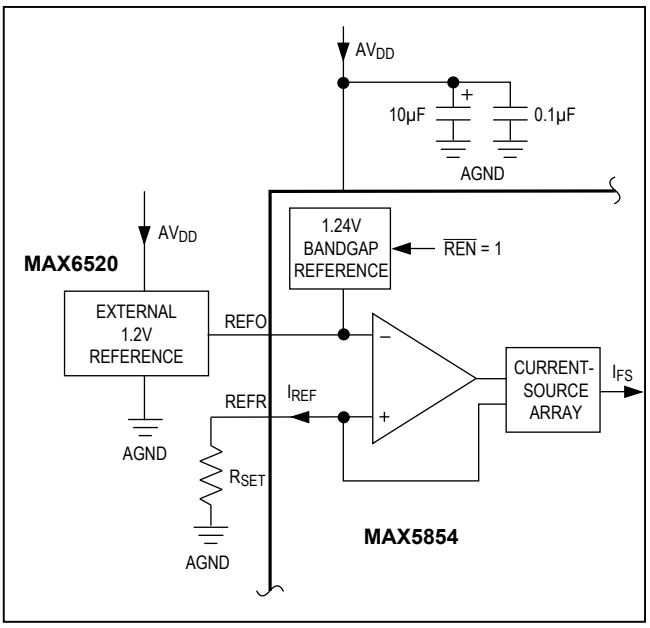


Figure 4. MAX5854 with External Reference

The CLK pin now becomes an output, and provides a single-ended replica of the differential clock signal, which can be used to synchronize the input data. Data is written to the device on the rising edge of the CLK signal.

Internal Reference and Control Amplifier

The MAX5854 provides an integrated 50ppm/°C, 1.24V, low-noise bandgap reference that can be disabled and overridden with an external reference voltage. REFO serves either as an external reference input or an integrated reference output. If $\overline{REN}$ = 0, the internal reference is selected and REFO provides a 1.24V (50µA) output. Buffer REFO with an external amplifier, when driving a heavy load.

The MAX5854 also employs a control amplifier designed to simultaneously regulate the full-scale output current (I_{FS}) for both outputs of the devices. Calculate the output current as:

$$I_{FS} = 32 \times I_{REF}$$

where I_{REF} is the reference output current ($I_{REF} = V_{REFO}/R_{SET}$) and I_{FS} is the full-scale output current. R_{SET} is the reference resistor that determines the amplifier output current of the MAX5854 (Figure 3). This current is mirrored into the current-source array where I_{FS} is equally distributed between matched current segments and summed to valid output current readings for the DACs.

External Reference

To disable the internal reference of the MAX5854, set $\overline{REN}$ = 1. Apply a temperature-stable, external reference to drive the REFO pin and set the full-scale output (Figure 4). For improved accuracy and drift performance, choose a fixed output voltage reference such as the 1.2V, 25ppm/°C MAX6520 bandgap reference.

Detailed Timing

The MAX5854 accepts an input data and the DAC conversion rate of up to 165Msps. The input latches on the rising edge of the clock, whereas the output latches on the following rising edge.

Figure 5 depicts the write cycle of the two DACs in non-interleaved mode.

The MAX5854 can also operate in an interleaved data mode. Programming the IDE bit with a high level activates this mode (Table 1 and Table 2). In interleaved mode, data for both DAC channels is written through input port A. Channel B data is written on the falling edge of the clock signal and then channel A data is written on the following rising edge of the clock signal. Both DAC outputs (channel A and B) are updated simultaneously on the next following rising edge of the clock. In interleaved data mode, the maximum input data rate per channel is half of the rate in noninterleaved mode. The interleaved data mode is attractive for applications where lower data rates are acceptable and interfacing on a single 10-bit bus is desired (Figure 6).

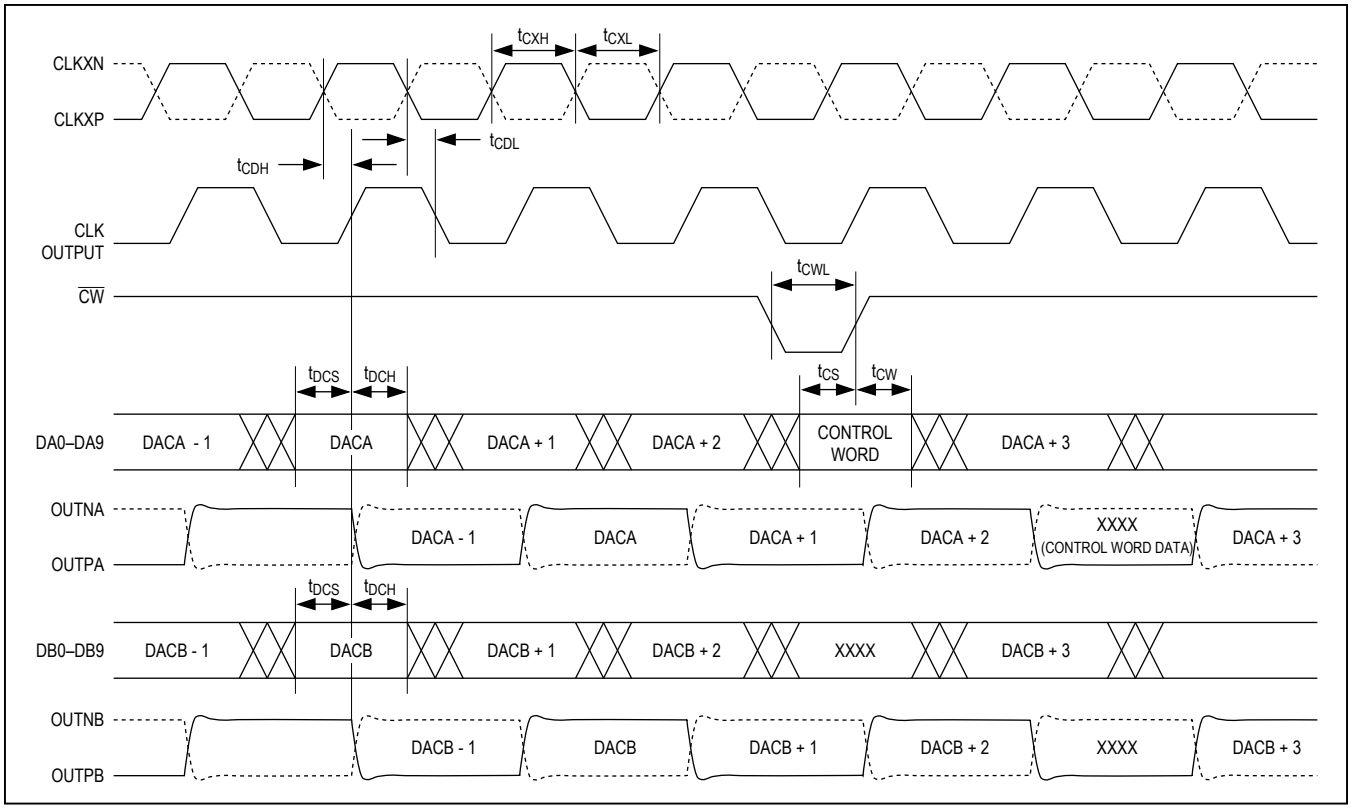


Figure 5. Timing Diagram for Noninterleaved Data Mode (IDE = 0)

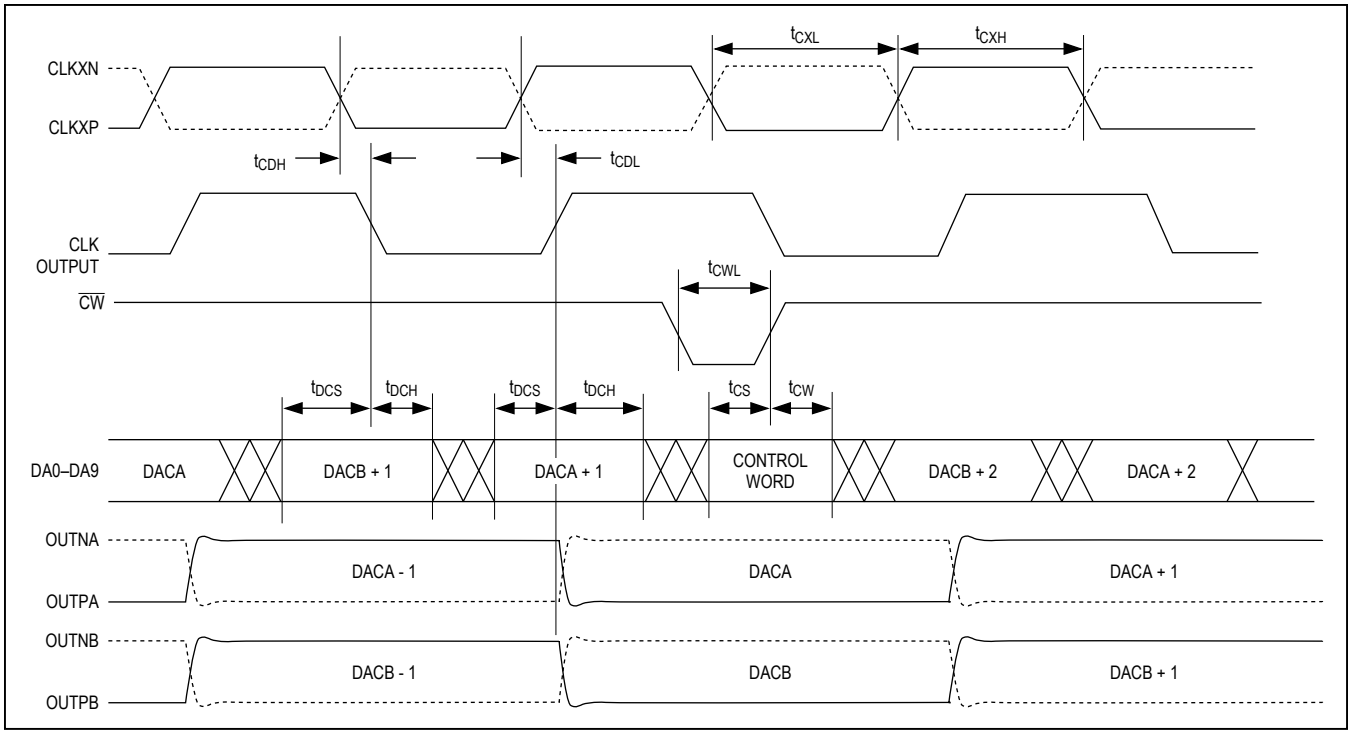


Figure 6. Timing Diagram for Interleaved Data Mode (IDE = 1)

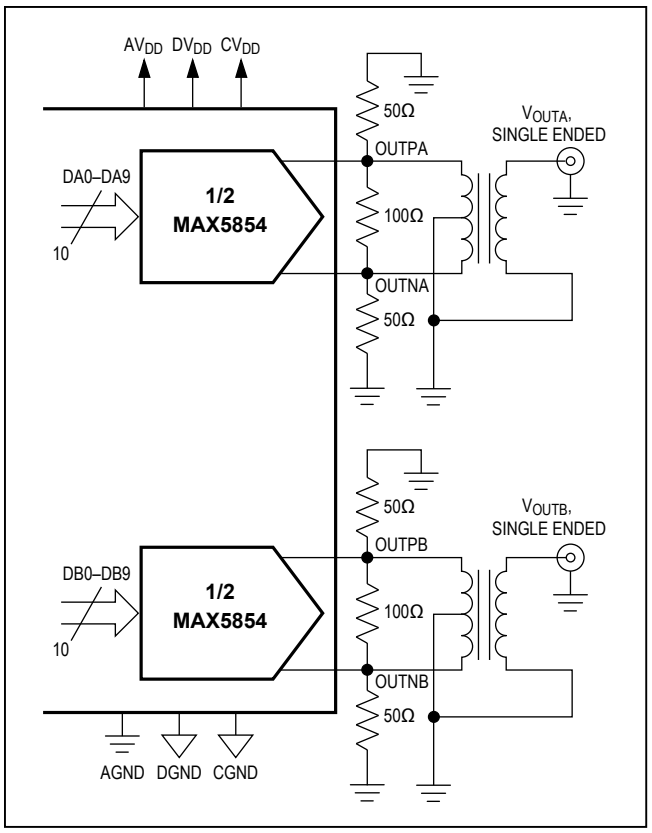


Figure 7. Application with Output Transformer Performing Differential-to-Single-Ended Conversion

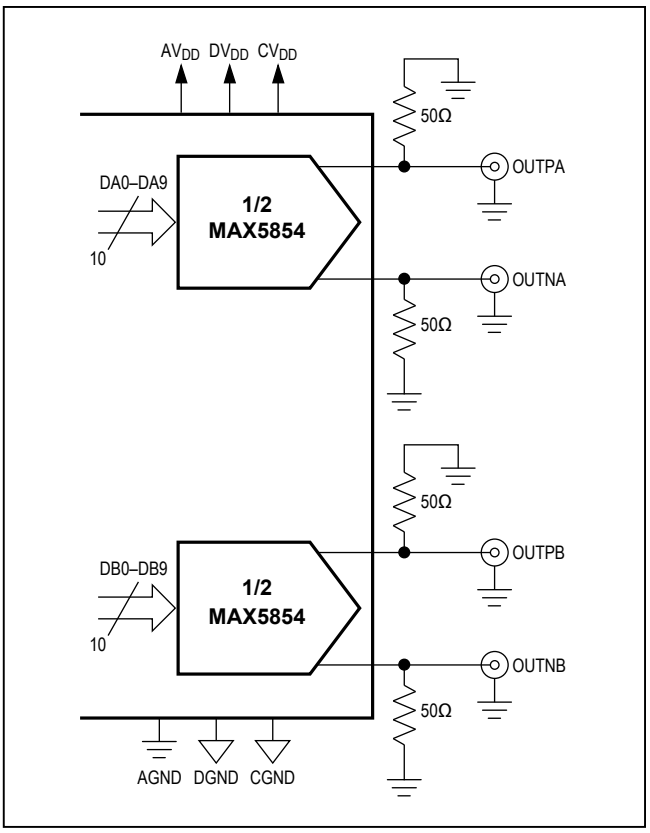


Figure 8. Application with DC-Coupled Differential Outputs

Applications Information

Differential-to-Single-Ended Conversion

The MAX5854 exhibits excellent dynamic performance to synthesize a wide variety of modulation schemes, including high-order QAM modulation with OFDM.

Figure 7 shows a typical application circuit with output transformers performing the required differential-to-single-ended signal conversion. In this configuration, the MAX5854 operates in differential mode, which reduces even-order harmonics, and increases the available output power.

Differential DC-Coupled Configuration

Figure 8 shows the MAX5854 output operating in differential, DC-coupled mode. This configuration can be used in communications systems employing analog quadrature upconverters and requiring a baseband sampling, dual-channel, high-speed DAC for I/Q synthesis. In these applications, information bandwidth can extend from 10MHz down to several hundred kilohertz. DC-coupling is desirable to eliminate long discharge time constants that are problematic with large, expensive coupling capacitors. Analog quadrature upconverters have a DC common-mode input requirement of typically 0.7V to 1.0V. The MAX5854 differential I/Q outputs can maintain the desired full-scale level at the required 0.7V to 1.0V DC common-mode level when powered from a single 2.85V (±5%) supply. The MAX5854 meets this low-power requirement with minimal reduction in dynamic range while eliminating the need for level-shifting resistor networks.

Power Supplies, Bypassing, Decoupling, and Layout

Grounding and power-supply decoupling strongly influence the MAX5854 performance. Unwanted digital crosstalk can couple through the input, reference, power-supply, and ground connections, which can affect dynamic specifications, like signal-to-noise ratio or spurious-free dynamic

range. In addition, electromagnetic interference (EMI) can either couple into or be generated by the MAX5854. Observe the grounding and power-supply decoupling guidelines for high-speed, high-frequency applications. Follow the power supply and filter configuration to realize optimum dynamic performance.

Use of a multilayer printed circuit (PC) board with separate ground and power-supply planes is recommended. Run high-speed signals on lines directly above the ground plane. The MAX5854 has separate analog and digital ground buses (AGND, CGND, and DGND, respectively). Provide separate analog, digital, and clock ground sections on the PC board with only one point connecting the three planes. The ground connection points should be located underneath the device and connected to the exposed paddle. Run digital signals above the digital ground plane and analog/clock signals above the analog/clock ground plane. Digital signals should be kept away from sensitive analog, clock, and reference inputs. Keep digital signal paths short and metal trace lengths matched to avoid propagation delay and data skew mismatch.

The MAX5854 includes three separate power-supply inputs: analog (AV_{DD}), digital (DV_{DD}), and clock (CV_{DD}). Use a single linear regulator power source to branch out to three separate power-supply lines (AV_{DD}, DV_{DD}, CV_{DD}) and returns (AGND, DGND, CGND).Filter each power-supply line to the respective return line using LC filters comprising ferrite beads and 10µF capacitors. Filter each supply input locally with 0.1µF ceramic capacitors to the respective return lines.

Note: To maintain the dynamic performance of the *Electrical Characteristics*, ensure the voltage difference between DV_{DD}, AV_{DD}, and CV_{DD} does not exceed 150mV.

Thermal Characteristics and Packaging

Thermal Resistance

40-lead thin QFN-EP:

$$\theta_{JA} = 38°C/W$$

The MAX5854 is packaged in a 40-pin thin QFN-EP package, providing greater design flexibility, increased thermal efficiency, and optimized AC performance of the DAC. The EP enables the implementation of grounding techniques, which are necessary to ensure highest performance operation.

In this package, the data converter die is attached to an EP leadframe with the back of this frame exposed at the package bottom surface, facing the PC board side of the package. This allows a solid attachment of the package to the PC board with standard infrared (IR) flow soldering techniques. A specially created land pattern on the PC board, matching the size of the EP (4.1mm x 4.1mm), ensures the proper attachment and grounding of the DAC. Designing vias* into the land area and implementing large ground planes in the PC board design allows for highest performance operation of the DAC. Use an array of 3 x 3 vias (≤ 0.3mm diameter per via hole and 1.2mm pitch between via holes) for this 40-pin thin QFN-EP package (package code: T4066-1).

Dynamic Performance Parameter Definitions

Adjacent Channel Leakage Ratio (ACLR)

Commonly used in combination with wideband code-division multiple-access (WCDMA), ACLR reflects the leakage power ratio in dB between the measured power within a channel relative to its adjacent channel. ACLR provides a quantifiable method of determining out-of-band spectral energy and its influence on an adjacent channel when a bandwidth-limited RF signal passes through a nonlinear device.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of all essential harmonics (within a Nyquist window) of the input signal to the fundamental itself. This can be expressed as:

$$THD = 20 \times \log \left[\frac{\sqrt{\left(V_2^2 + V_3^2 + V_4^2 ... + ... V_N^2\right)}}{V_1} \right]$$

where V_1 is the fundamental amplitude, and V_2 through V_N are the amplitudes of the 2nd through Nth order harmonics. The MAX5854 uses the first seven harmonics for this calculation.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of RMS amplitude of the carrier frequency (maximum signal component) to the RMS value of their next-largest spectral component. SFDR is usually measured in dBc with respect to the carrier frequency amplitude or in dBFS with respect to the DAC's full-scale range. Depending on its test condition, SFDR is observed within a predefined window or to Nyquist.

**Vias connect the land pattern to internal or external copper planes.*

Multitone Power Ratio (MTPR)

A series of equally spaced tones are applied to the DAC with one tone removed from the center of the range. MTPR is defined as the worst-case distortion (usually a 3rd-order harmonic product of the fundamental frequencies), which appears as the largest spur at the frequency of the missing tone in the sequence. This test can be performed with any number of input tones; however, four and eight tones are among the most common test conditions for CDMA- and GSM/EDGE-type applications.

Intermodulation Distortion (IMD)

The two-tone IMD is the ratio expressed in dBc of either output tone to the worst 3rd-order (or higher) IMD products.

Static Performance Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. For a DAC, the deviations are measured at every individual step.

Differential Nonlinearity (DNL)

Differential nonlinearity (DNL) is the difference between an actual step height and the ideal value of 1 LSB. A DNL error specification no more negative than -1 LSB guarantees monotonic transfer function.

Offset Error

Offset error is the current flowing from positive DAC output when the digital input code is set to zero. Offset error is expressed in LSBs.

Gain Error

A gain error is the difference between the ideal and the actual full-scale output current on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step. The ideal current is defined by reference voltage at V_{REFO}/I_{REF} x 32.

Settling Time

The settling time is the amount of time required from the start of a transition until the DAC output settles to its new output value to within the converter's specified accuracy.

Glitch Impulse

A glitch is generated when a DAC switches between two codes. The largest glitch is usually generated around the midscale transition, when the input pattern transitions from 011…111 to 100…000. This occurs due to timing variations between the bits. The glitch impulse is found by integrating the voltage of the glitch at the midscale transition over time. The glitch impulse is usually specified in pV-s.

Table 4. Part Selection Table

PART	SPEED (Msps)	RESOLUTION
MAX5851	80	8-bit, dual
MAX5852	165	8-bit, dual
MAX5853	80	10-bit, dual
MAX5854	165	10-bit, dual

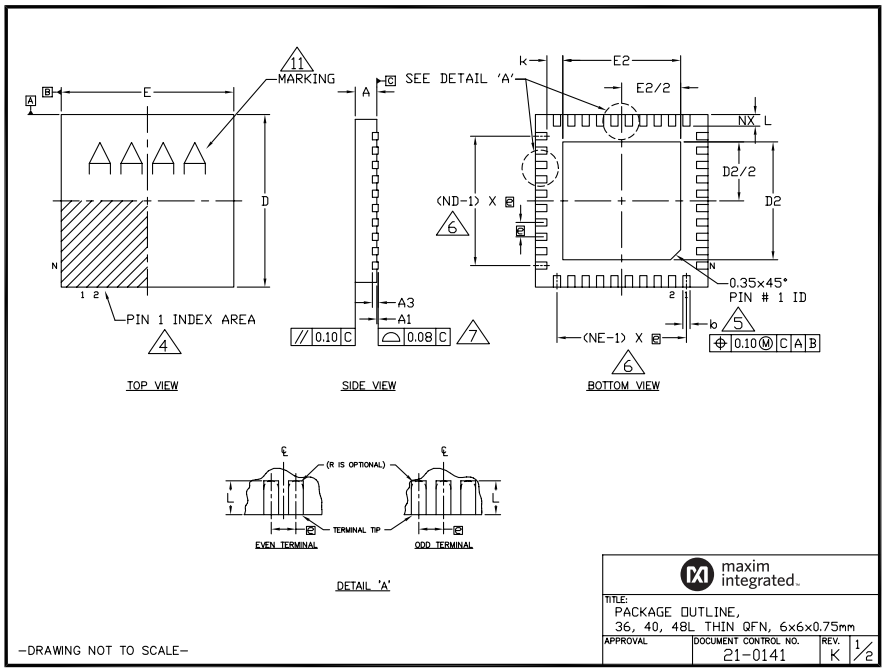
Chip Information

TRANSISTOR COUNT: 9,035

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



COMMON DIMENSIONS									
PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–
L	0.35	0.50	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80
T3666N-1	3.60	3.70	3.80	3.60	3.70	3.80
T3666MN-1	3.60	3.70	3.80	3.60	3.70	3.80
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20
T4866-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866N-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866-2	4.40	4.50	4.60	4.40	4.50	4.60
T4066MN-5	4.00	4.10	4.20	4.00	4.10	4.20

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES IN DEGREES UNLESS OTHERWISE SPECIFIED
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
3. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10–0131.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95–1 SPP–012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE, RESPECTIVELY.
7. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
8. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH: PACKAGE T4866.
9. N IS THE TOTAL NUMBER OF TERMINALS.
10. WARPAGE SHALL NOT EXCEED 0.10mm.
11. MARKING IS FOR PACKAGE ORIENTATION PURPOSE ONLY.
12. NUMBER OF LEADS SHOWN FOR REFERENCE ONLY.
13. ALL DIMENSIONS APPLY TO BOTH LEADED (–) AND PbFREE (+) PKG. CODES.

–DRAWING NOT TO SCALE–

maxim integrated
PACKAGE OUTLINE, 36, 40, 48L THIN QFN, 6x6x0.75mm
21-0141
K
2/2

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