

M62352P/FP/GP

R03DS0041EJ0400

Rev.4.00

8-bit 12ch D/A Converter with Buffer Amplifiers

Jun 03, 2011

Description

The M62352 is an integrated circuit semiconductor of CMOS structure with 12 channels of built-in D/A converters with output buffer operational amplifiers.

The 3-wire serial interface method is used for the transfer format of digital data to allow connection with microcomputer with minimum wiring.

It is able to cascading serial use with DO terminal.

The output buffer operational amplifier operates in the whole voltage range from power supply to ground for both input/output.

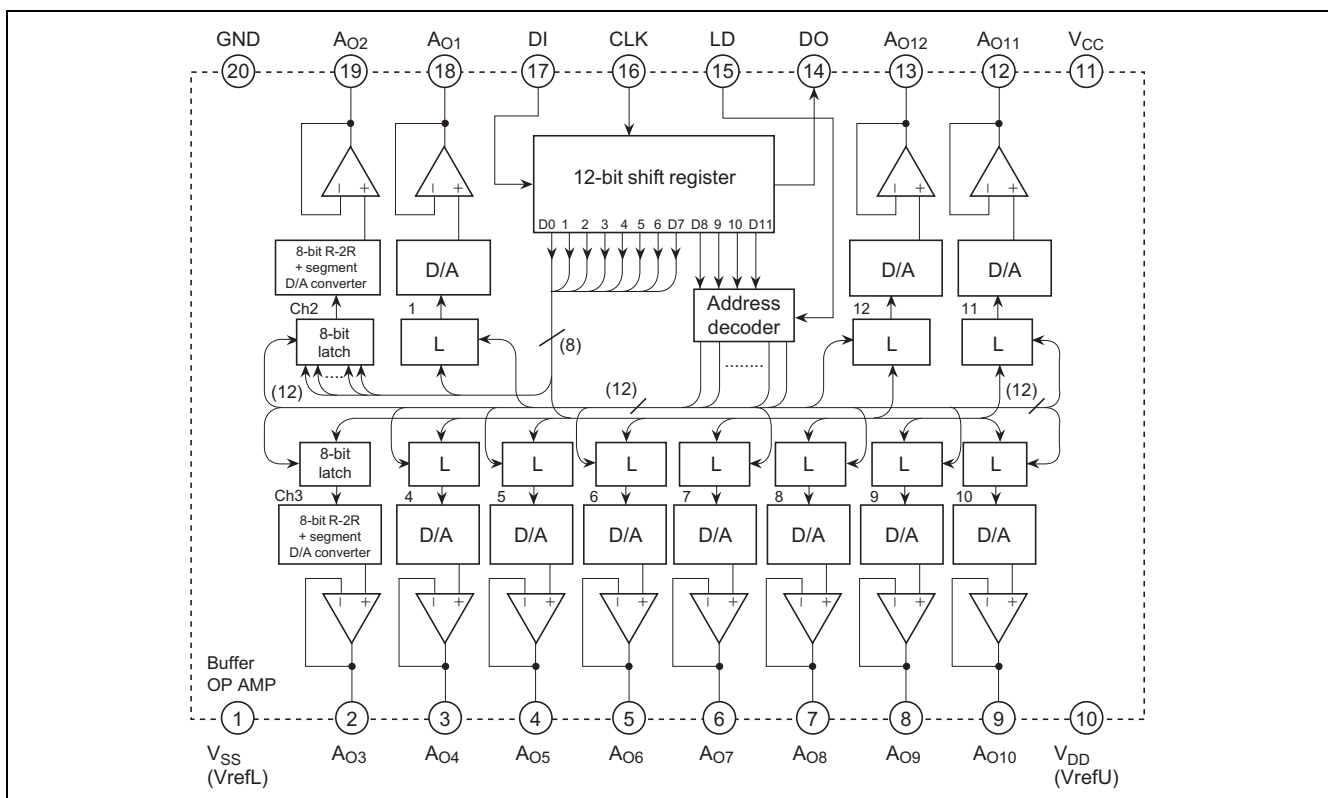
Features

- 12-bit serial data input (3-wire serial data transfer method)
- Highly stable output buffer operational amplifier allow operation in the all voltage range from power supply to ground.

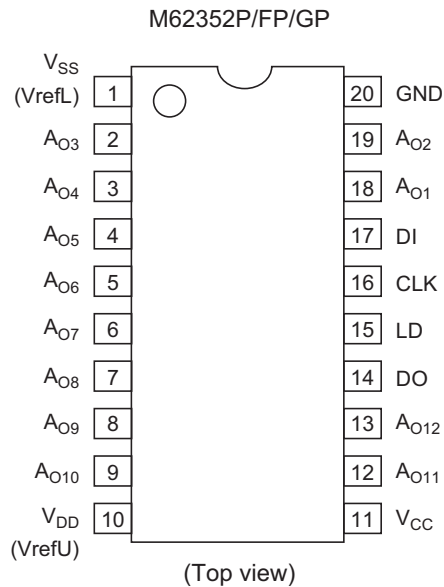
Application

Adjustment/control of industrial or home-use electronic equipment, such as VTR camera, VTR set, TV, and CRT display.

Block Diagram



Pin Arrangement

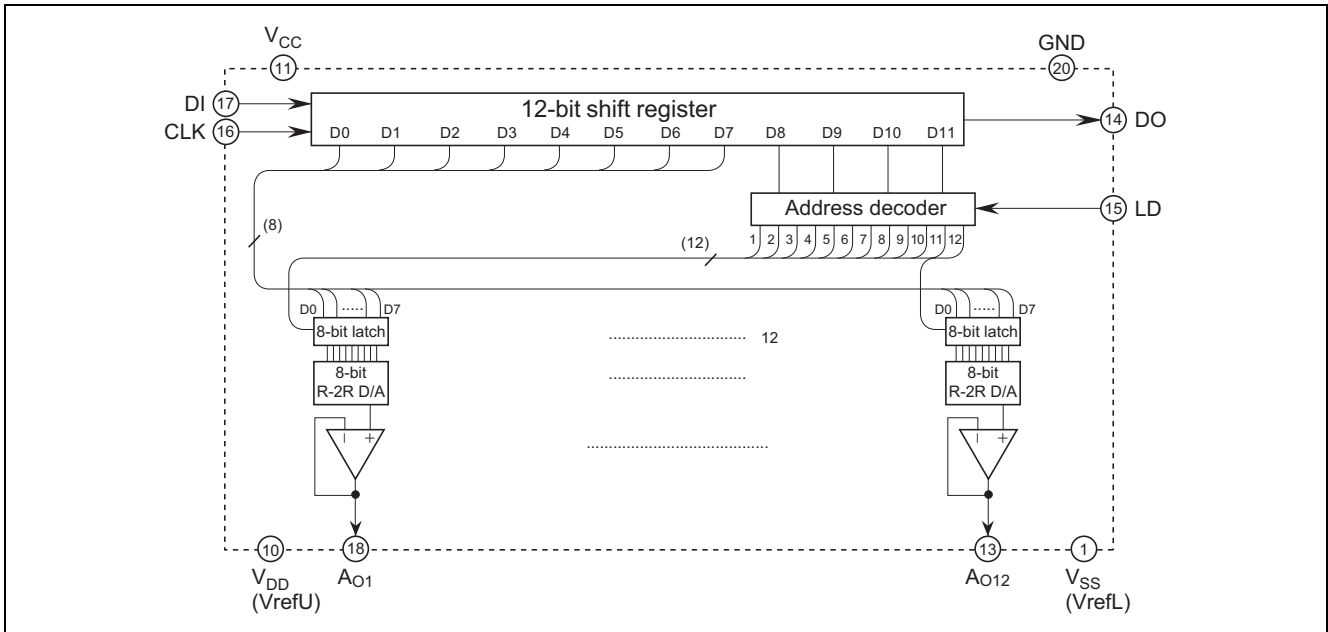


Outline: PRDP0020BA-A (20P4B) [P] (not recommend for new design)
 PRSP0020DA-A (20P2N-A) [FP]
 20P2E-A [GP]

Pin Description

Pin No.	Pin Name	Function
17	DI	Serial data input terminal
14	DO	Serial data output terminal
16	CLK	Serial clock input terminal
15	LD	LD terminal input high level then latch circuit data load
18	AO ₁	8-bit D/A converter output terminal
19	AO ₂	
2	AO ₃	
3	AO ₄	
4	AO ₅	
5	AO ₆	
6	AO ₇	
7	AO ₈	
8	AO ₉	
9	AO ₁₀	
12	AO ₁₁	
13	AO ₁₂	
11	V _{CC}	Power supply terminal
20	GND	Digital and analog common GND
10	V _{DD}	D/A converter upper reference voltage input terminal
1	V _{SS}	D/A converter lower reference voltage input terminal

Block Diagram for Explanation of Terminals



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V _{CC}	-0.3 to +7.0	V
D/A converter upper reference voltage	V _{DD}	-0.3 to +7.0	V
Input voltage	V _{IN}	-0.3 to V _{CC} + 0.3	V
Output voltage	V _O	-0.3 to V _{CC} + 0.3	V
Power dissipation	P _d	350 (P) / 300 (FP) / 150 (GP)	mW
Operating temperature	T _{opr}	-20 to +85	°C
Storage temperature	T _{stg}	-40 to +125	°C

Electrical Characteristics

Digital Part

(V_{CC} , $V_{refU} = +5\text{ V} \pm 10\%$, $V_{CC} \geq V_{refU}$, GND , $V_{refL} = 0\text{ V}$, $T_a = -20^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Circuit current	I_{CC}	—	1.6	3.2	mA	CLK = 1 MHz operation $I_{OA} = 0\ \mu\text{A}$
Input leak current	I_{ILK}	-10	—	10	μA	$V_{IN} = 0$ to V_{CC}
Input low voltage	V_{IL}	—	—	$0.2 V_{CC}$	V	
Input high voltage	V_{IH}	$0.8 V_{CC}$	—	—	V	
Output low voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 2.5\text{ mA}$
Output high voltage	V_{OH}	$V_{CC} - 0.4$	—	—	V	$I_{OH} = -400\ \mu\text{A}$

Analog Part

(V_{CC} , $V_{refU} = +5\text{ V} \pm 10\%$, $V_{CC} \geq V_{refU}$, $T_a = -20^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted)

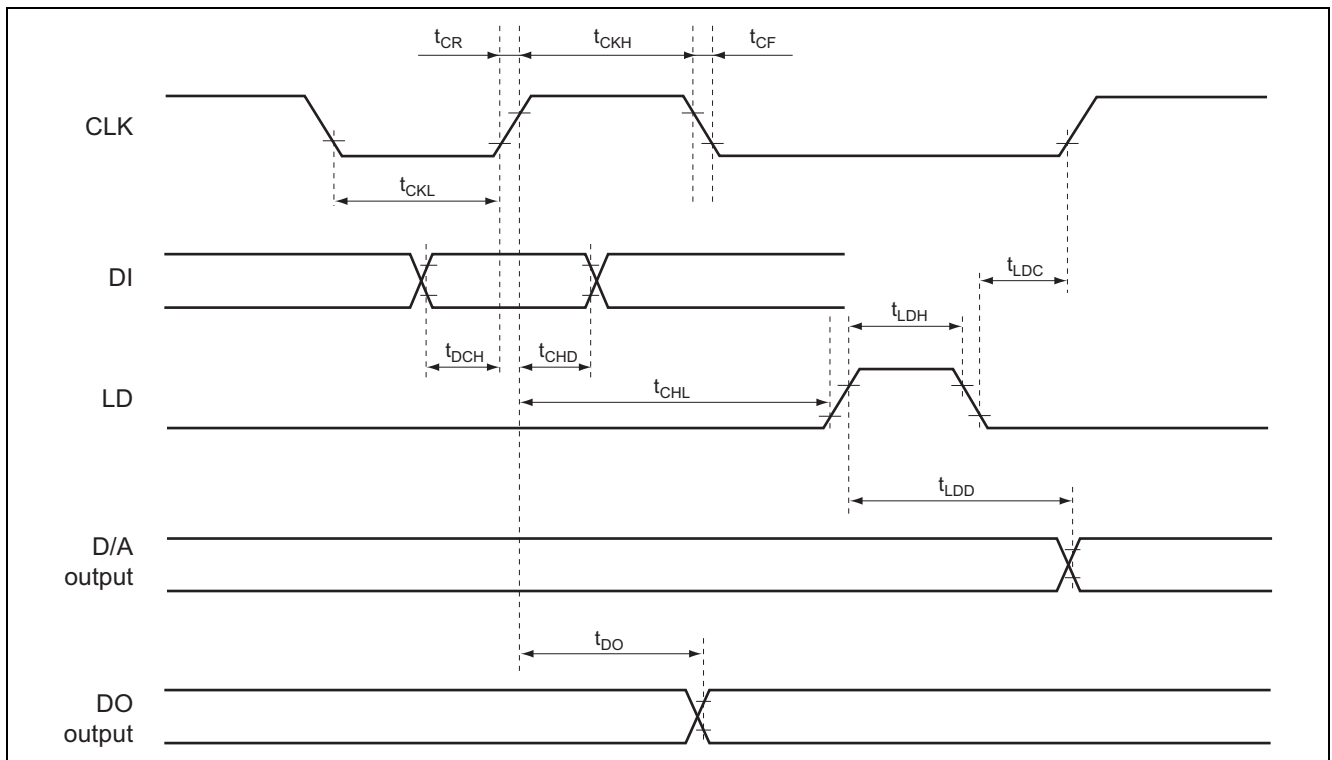
Item	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Current dissipation	I_{DD}	—	1.5	3.5	mA	$V_{refU} = 5\text{ V}$, $V_{refL} = 0\text{ V}$, $I_{AO} = 0\ \mu\text{A}$ Data condition; at maximum current
D/A converter upper reference voltage range	V_{DD}	3.5	—	V_{CC}	V	The output dose not necessarily be the value within the reference voltage setting range. The output value is determined by the buffer amplifier output voltage range (V_{AO})
D/A converter lower reference voltage range	V_{SS}	GND	—	$V_{CC} - 3.5$	V	
Buffer amplifier output voltage range	V_{AO}	0.1	—	$V_{CC} - 0.1$	V	$I_{OA} = \pm 100\ \mu\text{A}$
		0.2	—	$V_{CC} - 0.2$		$I_{OA} = \pm 500\ \mu\text{A}$
Buffer amplifier output drive range	I_{AO}	-1	—	1	mA	Upper side saturation voltage = 0.3 V Lower side saturation voltage = 0.2 V
Differential nonlinearity error	S_{DL}	-1.0	—	1.0	LSB	$V_{refU} = 4.79\text{ V}$ $V_{refL} = 0.95\text{ V}$
Nonlinearity error	S_L	-1.5	—	1.5	LSB	$V_{CC} = 5.5\text{ V}$ (15 mV/LSB)
Zero code error	S_{ZERO}	-2	—	2	LSB	Without load ($I_{OA} = \pm 0\ \mu\text{A}$)
Full scale error	S_{FULL}	-2	—	2	LSB	
Output capacitive load	C_O	—	—	0.1	μF	
Buffer amplifier output impedance	R_O	—	5	—	Ω	

AC Characteristics

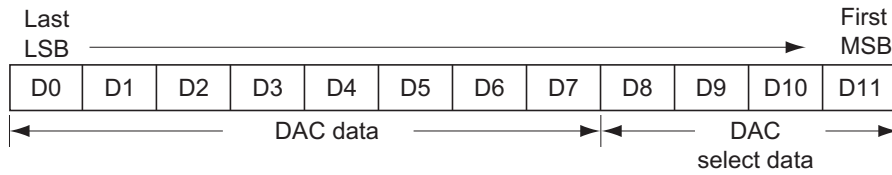
(V_{CC} , $V_{refU} = +5\text{ V} \pm 10\%$, $V_{CC} \geq V_{refU}$, GND , $V_{refL} = 0\text{ V}$, $T_a = -20$ to $+85^\circ\text{C}$, unless otherwise noted)

Item	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Clock "L" pulse width	t_{CKL}	200	—	—	ns	
Clock "H" pulse width	t_{CKH}	200	—	—	ns	
Clock rise time	t_{CR}	—	—	200	ns	
Clock fall time	t_{CF}	—	—	200	ns	
Data setup time	t_{DCH}	30	—	—	ns	
Data hold time	t_{CHD}	60	—	—	ns	
LD setup time	t_{CHL}	200	—	—	ns	
LD hold time	t_{LDC}	100	—	—	ns	
LD "H" pulse width	t_{LDH}	100	—	—	ns	
Data output delay time	t_{DO}	70	—	350	ns	$C_L \leq 100\text{ pF}$
D/A output setting time	t_{LDD}	—	—	300	μs	$C_L \leq 100\text{ pF}$ $V_{AO}: 0.5 \leftrightarrow 4.5\text{ V}$ The time until the output becomes the final value of 1/2 LSB

Timing Chart



Digital Data Format



DAC Data

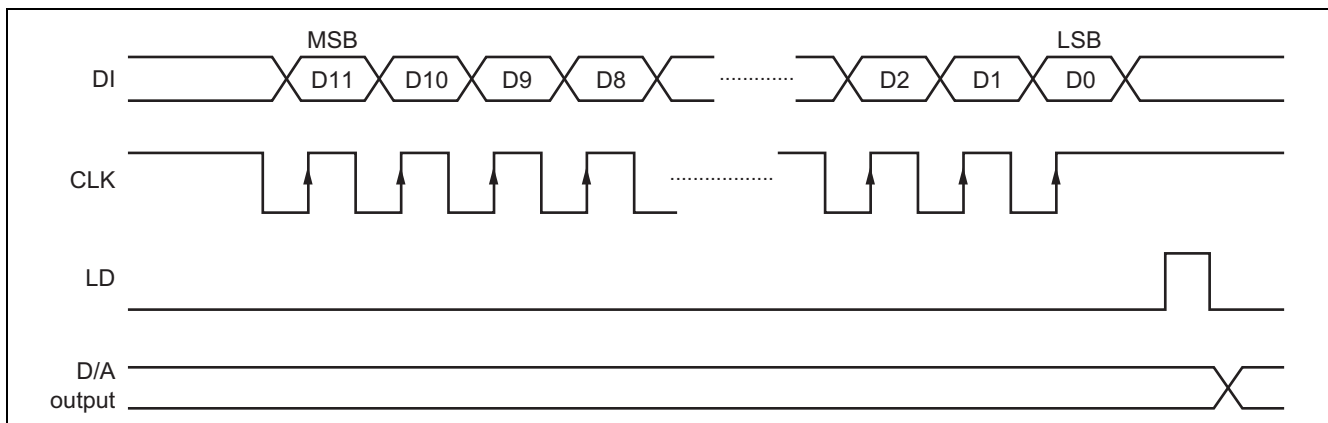
D0	D1	D2	D3	D4	D5	D6	D7	D/A Output
0	0	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 1 + V_{refL}$
1	0	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 2 + V_{refL}$
0	1	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 3 + V_{refL}$
1	1	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 4 + V_{refL}$
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	$(V_{refU} - V_{refL}) / 256 \times 255 + V_{refL}$
1	1	1	1	1	1	1	1	V_{refU}

Note: $V_{refU} = V_{DD}$, $V_{refL} = V_{SS}$

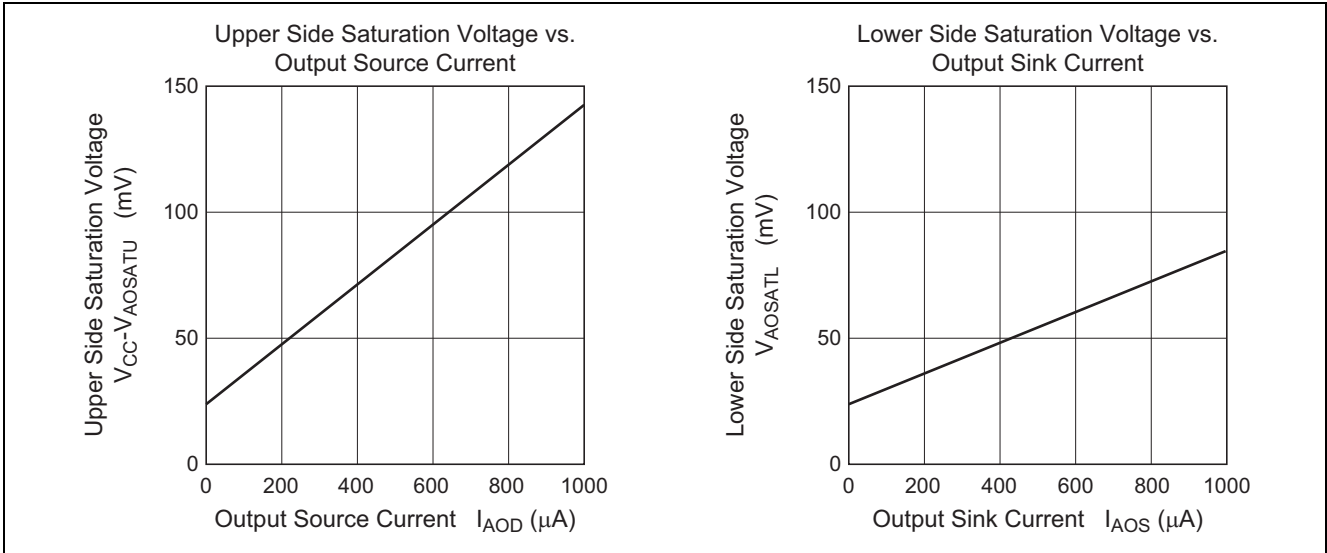
DAC Select Data

D8	D9	D10	D11	DAC Selection
0	0	0	0	Don't care
0	0	0	1	A ₀₁ select
0	0	1	0	A ₀₂ select
0	0	1	1	A ₀₃ select
0	1	0	0	A ₀₄ select
0	1	0	1	A ₀₅ select
0	1	1	0	A ₀₆ select
0	1	1	1	A ₀₇ select
1	0	0	0	A ₀₈ select
1	0	0	1	A ₀₉ select
1	0	1	0	A ₀₁₀ select
1	0	1	1	A ₀₁₁ select
1	1	0	0	A ₀₁₂ select
1	1	0	1	Don't care
1	1	1	0	Don't care
1	1	1	1	Don't care

Timing Chart (Model)

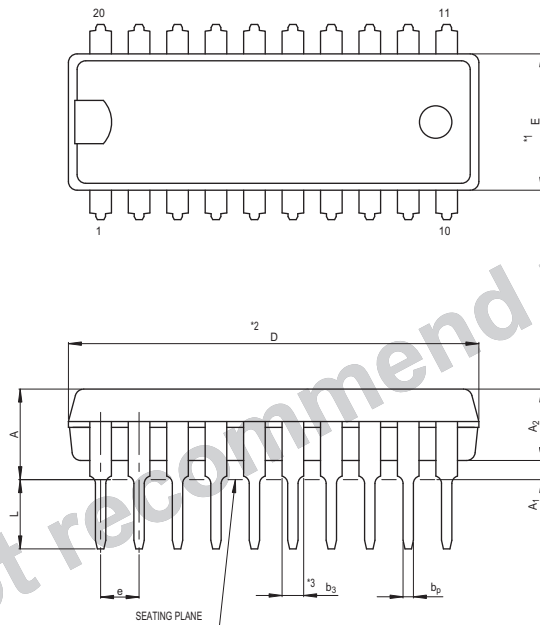


Typical Characteristics



Package Dimensions

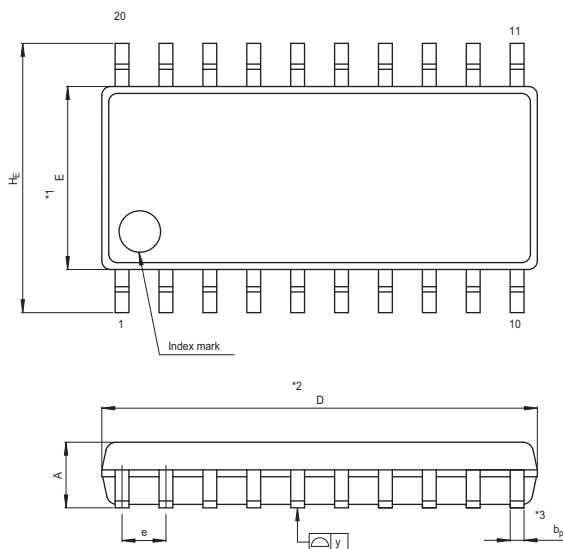
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SDIP20-6.3x19-1.78	PRDP0020BA-A	20P4B	1.0g



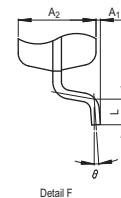
NOTE)
 1. DIMENSIONS $^1 E$ AND $^2 D$ DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION $^3 L$ DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	7.32	7.62	7.92
D	18.8	19.0	19.2
E	6.15	6.3	6.45
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b_p	0.38	0.48	0.58
b_3	0.9	1.0	1.3
c	0.22	0.27	0.34
θ	0°	—	15°
e	1.528	1.778	2.028
L	3.0	—	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP20-5.3x12.6-1.27	PRSP0020DA-A	20P2N-A	0.3g



NOTE)
 1. DIMENSIONS $^1 E$ AND $^2 D$ DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION $^3 L$ DOES NOT INCLUDE TRIM OFFSET.

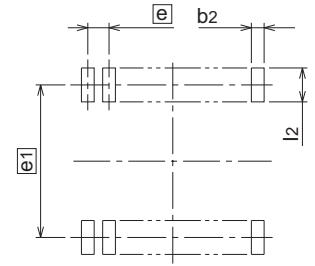
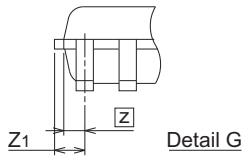
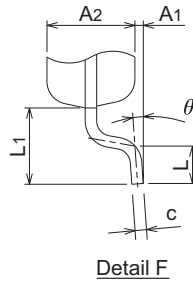
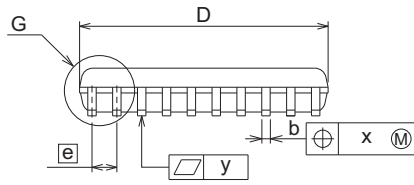
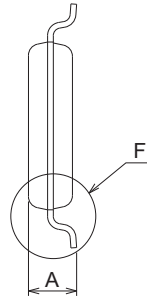
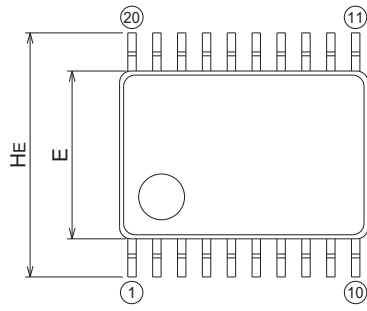


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	12.5	12.6	12.7
E	5.2	5.3	5.4
A_2	—	1.8	—
A_1	0	0.1	0.2
A	—	—	2.1
b_p	0.35	0.4	0.5
c	0.18	0.2	0.25
θ	0°	—	8°
H_E	7.5	7.8	8.1
e	1.12	1.27	1.42
y	—	—	0.1
L	0.4	0.6	0.8

20P2E-A

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP20-P-225-0.65	—	0.08	Alloy 42

Plastic 20pin 225mil SSOP



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.45
A1	0	0.1	0.2
A2	—	1.15	—
b	0.17	0.22	0.32
c	0.13	0.15	0.2
D	6.4	6.5	6.6
E	4.3	4.4	4.5
e	—	0.65	—
HE	6.2	6.4	6.6
L	0.3	0.5	0.7
L1	—	1.0	—
Z	—	0.325	—
Z1	—	—	0.475
x	—	—	0.13
y	—	—	0.1
θ	0°	—	10°
b2	—	0.35	—
e1	—	5.8	—
l2	1.0	—	—

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