



Low Cost, High Speed 12-Bit Monolithic D/A Converter

AD566A

T-51-09-12

1.1 Scope.

This specification covers the detail requirements for a precision, high speed current output 12-bit resolution D/A converter.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD566ASD/883B
-2	AD566ATD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000; package outline: D-24.

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{EE} to Power Ground	0 to -18V
Voltage on DAC Output (Pin 9)	-3V to +12V
Digital Inputs (Pins 13 to 24) to Power Ground	-1.0V to +7.0V
Ref In to Reference Ground	$\pm 12\text{V}$
Bipolar Offset to Reference Ground	$\pm 12\text{V}$
10V Span R to Reference Ground	$\pm 12\text{V}$
20V Span R to Reference Ground	$\pm 24\text{V}$
Power Dissipation	1000mW
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature Range (Soldering 10sec)	$+300^\circ\text{C}$

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 25^\circ\text{C}/\text{W}$
 $\theta_{JA} = 48^\circ\text{C}/\text{W}$

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Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Relative Accuracy	RA	-1	1/2	1/2	3/4		All Bits with Positive Errors On. All Bits with Negative Errors On.	± LSB max
		-2	1/4	1/2	1/2	1/4		
Differential Nonlinearity	DNL	-1	3/4	3/4	1		Major Transitions	± LSB max
		-2	1/2	3/4	1	1/2		
Gain Error	A _E	-1, 2	0.25	0.25			R _{REF} = 50Ω Fixed	± % of FS max
Gain Error Temperature	TC _{AE}	-1			10			± ppm of FS/°C max
		-2			5			
Offset Error	V _{OS}	-1, 2	0.05	0.05				± % of FS max
Offset Error Temperature Coefficient	TCV _{OS}	-1, 2			2			± ppm of FS/°C max
Bipolar Zero Error ²	B _{PZE}	-1	0.15	0.15			R _{BO} = 50Ω Fixed	± % of FS max
		-2	0.10	0.15		0.10		
B/P Zero Error ² Temperature Coefficient	TCB _{PZE}	-1, 2			10			± ppm of FS/°C max
Input Resistance	R _{IN}	-1, 2	15					kΩ min
			25					kΩ max
Full Scale Transition	t _{FS}	-1, 2	30				10% to 90% Delay Plus Rise Time	ns max
			50				90% to 10% Delay Plus Fall Time	
Output Current Settling Time	t _{SL}	-1, 2	350					ns max
Compliance Voltage	CV	-1, 2	1.5				-55°C to +125°C	-V min
			10					+V max
Output Resistance	R _{OUT}	-1, 2	6				Exclusive of Span Resistors	kΩ min
			10					kΩ max
Output Current	I _{OUT}	-1, 2	1.6	1.6			Unipolar (All Bits On)	-mA min
			2.4	2.4				-mA max
			0.8	0.8			Bipolar (All Bits On)	-mA min
			1.2	1.2				-mA max
Power Supply Rejection Ratio ³	PSRR	-1, 2	25	25				± ppm of FS/% max
Power Supply Current ³	I _{EE}	-1, 2	18	18				-mA max
Power Dissipation	P _D	-1, 2	300	300				mW max
Digital Input High Voltage	V _{IH}	-1, 2	2.0	2.0				+V min
			5.5	5.5			+V max	
Digital Input Low Voltage	V _{IL}	-1, 2	0.8	0.8				+V max
Digital Input High Current	I _{IH}	-1, 2	300	300			V _{IH} = 5.5V	+μA max
Digital Input Low Current	I _{IL}	-1, 2	100	100			V _{IL} = 0V	+μA max

NOTES

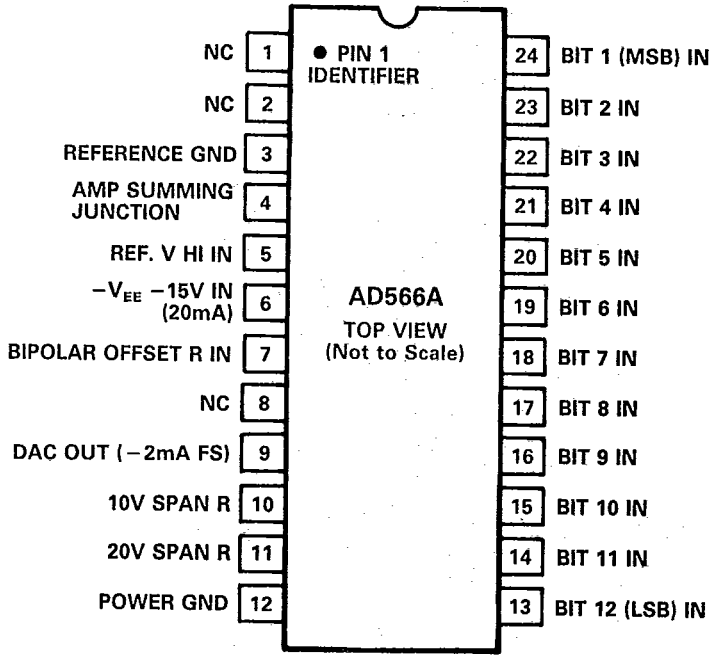
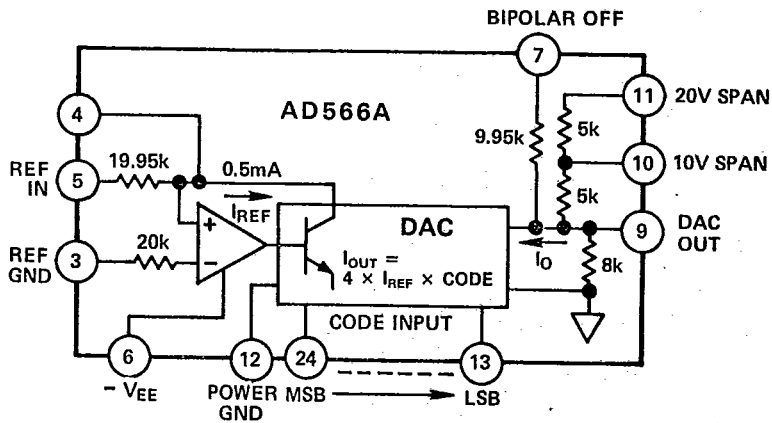
¹V_{BE} = -15V, V_{IH} = 2.0V, V_{IL} = 0.8V, T_A = +25°C unless otherwise indicated.V_{IH} = 2.0V, V_{IL} = 0.8V guaranteed design limits at -55°C to +125°C.²MSB on; all other bits off.³Guaranteed for -11.4 ≥ V_{BE} ≥ -16.5V.

Table 1.

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3.2.1 Functional Block Diagram and Terminal Assignments.

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3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (56).

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4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

