MCP48CXDX1/2

8/10/12-Bit Digital-to-Analog Converters, 1 LSb INL, Single/Dual Voltage Outputs with SPI Interface

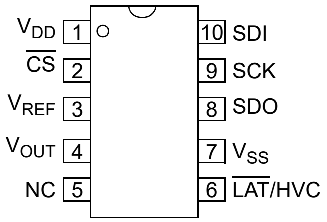
Features

- Memory Options:
  - Volatile memory: MCP48CVDX1/2
  - Nonvolatile memory: MCP48CMDX1/2
- Operating Voltage Range:
  - 2.7V to 5.5V – Full specifications
  - 1.8V to 2.7V – Reduced device specifications
- Output Voltage Resolutions:
  - 8-bit: MCP48CXD0X (256 steps)
  - 10-bit: MCP48CXD1X (1024 steps)
  - 12-bit: MCP48CXD2X (4096 steps)
- Nonvolatile Memory (MTP) Size: 32 Locations
- 1 LSb Integral Nonlinearity (INL) Specification
- DAC Voltage Reference Source Options:
  - Device V_{DD}
  - External V_{REF} pin (buffered or unbuffered)
  - Internal band gap (1.214V typical)
- Output Gain Options:
  - 1x (unity)
  - 2x (available when not using internal V_{DD} as voltage source)
- Power-on/Brown-out Reset (POR/BOR) Protection
- Power-Down Modes:
  - Disconnects output buffer (high-impedance)
  - Selection of V_{OUT} pull-down resistors (100 kΩ or 1 kΩ)
- SPI Interface:
  - Supports '`00`' and '`11`' modes
  - 50 MHz write speed
  - 25 MHz read speed
- Package Types:
  - Dual: 16-lead 3 x 3 QFN, 10-lead MSOP, 10-lead 3 x 3 DFN
  - Single: 16-lead 3 x 3 QFN, 10-lead MSOP, 10-lead 3 x 3 DFN
- Extended Temperature Range: -40°C to +125°C

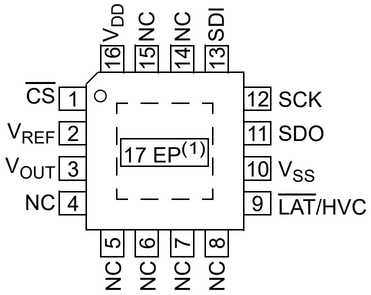
Package Types

MCP48CXDX1 (Single)

MSOP-10, DFN-10 (3 x 3)

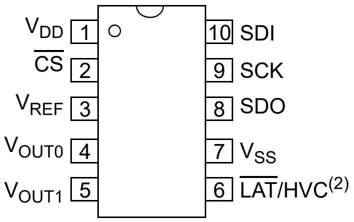


QFN-16 (3 x 3)

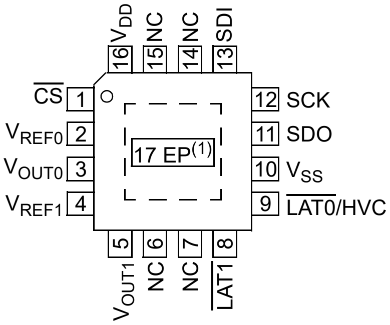


MCP48CXDX2 (Dual)

MSOP-10, DFN-10 (3 x 3)



QFN-16 (3 x 3)



Note 1: Exposed pad (substrate paddle).

2: This pin's signal can be connected to DAC0 and/or DAC1.

General Description

The MCP48CXDX1/2 are single and dual channel 8-bit, 10-bit and 12-bit buffered voltage output Digital-to-Analog Converters (DAC), with volatile or MTP memory and an SPI serial interface.

The MTP memory can be written by the user up to 32 times, for each specific register. It requires a high-voltage level on the HVC pin, typically 7.5V, in order to successfully program the desired memory location. The nonvolatile memory includes power-up output values, device configuration registers and general purpose memory.

The V_{REF} pin, the device V_{DD} or the internal band gap voltage can be selected as the DAC's reference voltage. When V_{DD} is selected, V_{DD} is internally connected to the DAC reference circuit.

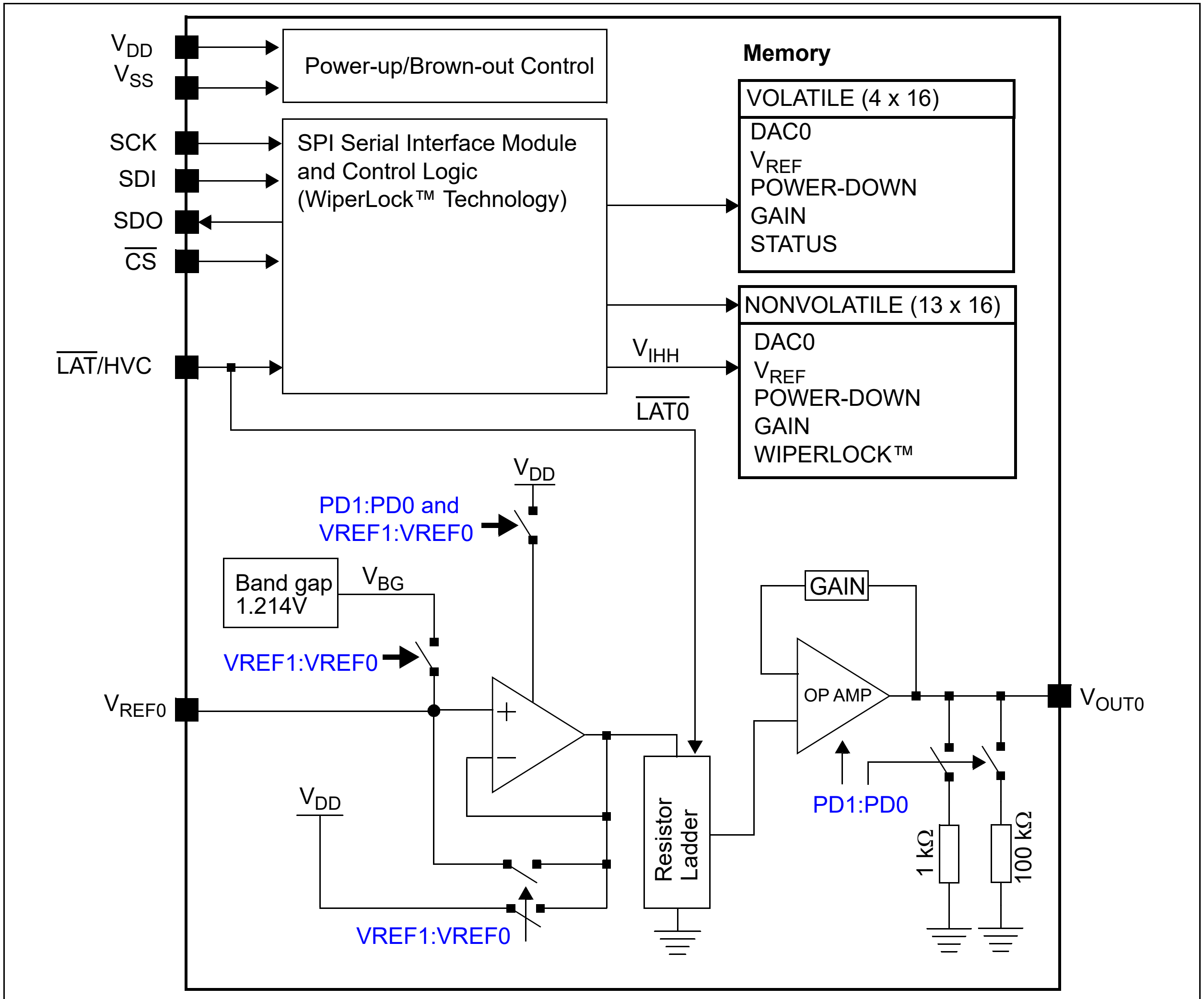
When the V_{REF} pin is used with an external voltage reference, the user can select between a gain of 1 or 2 and can have the reference buffer enabled or disabled. When the gain is 2, the V_{REF} pin voltage must be limited to a maximum of $V_{DD}/2$.

These devices have a four-wire SPI-compatible serial interface with speeds up to 50 MHz for write and 25 MHz for read operations.

Applications

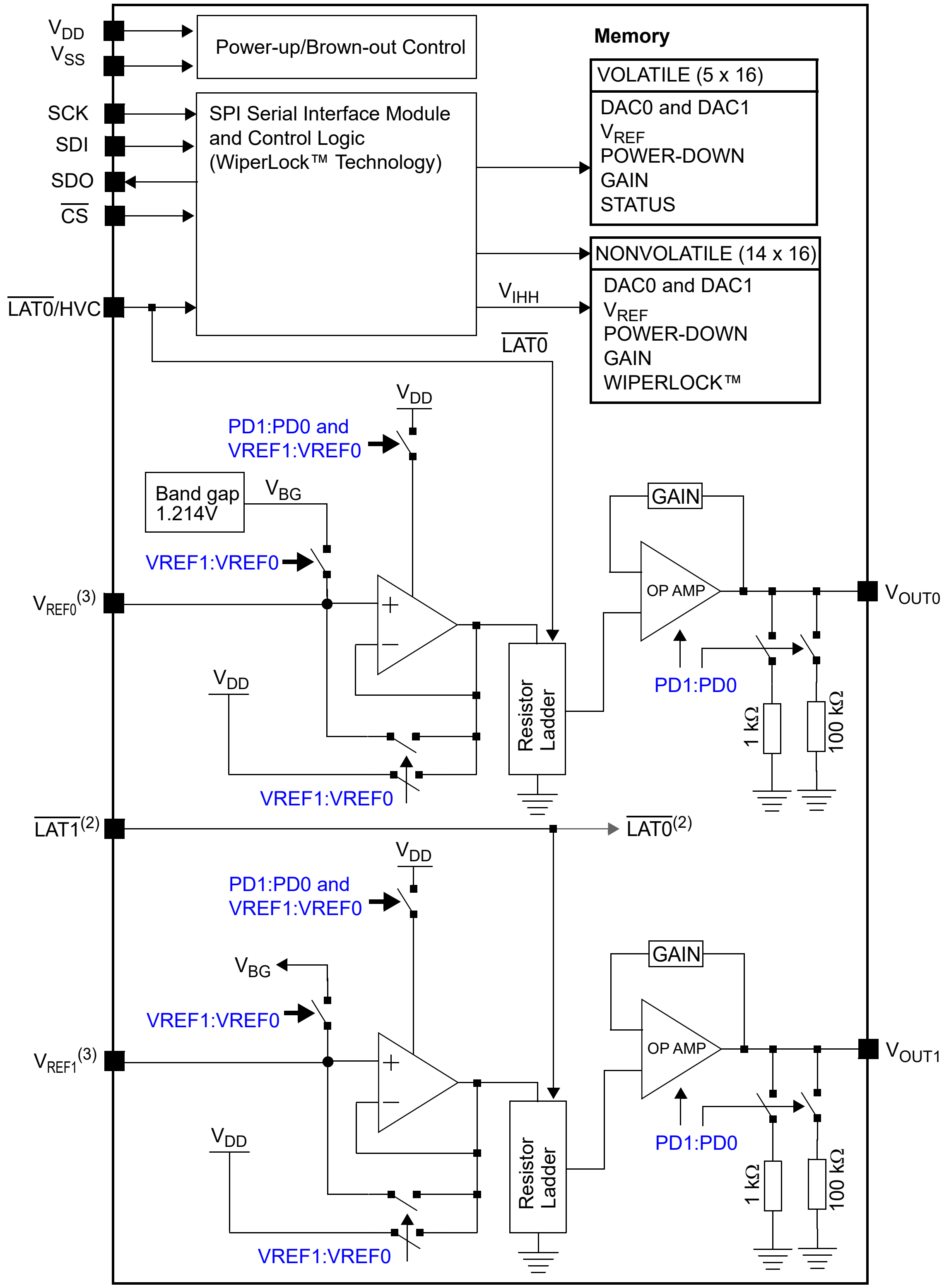
- Set Point or Offset Trimming
- Sensor Calibration
- Low-Power Portable Instrumentation
- PC Peripherals
- Data Acquisition Systems

MCP48CXDX1 Block Diagram (Single Channel Output)



Note 1: Available only on specific packages.

MCP48CXDX2 Block Diagram (Dual Channel Output)



Note 1: Available only on specific packages.

2: On dual output devices, except those in a QFN16 package, the $\overline{LAT0}$ pin is internally connected to the $\overline{LAT1}$ input of DAC1.

3: On dual output devices, except those in a QFN16 package, the V_{REF0} pin is internally connected to the V_{REF1} input of DAC1.

Family Device Features

Device	Package Type	# of Channels	Resolution (bits)	DAC Output POR/BOR Setting(1)	# of V_{REF} Inputs	# of $\overline{LAT}$ Inputs(3)	Memory(2)	GP MTP Locations
MCP48CVD01	MSOP, QFN, DFN	1	8	7Fh	1	1	RAM	—
MCP48CVD11	MSOP, QFN, DFN	1	10	1FFh	1	1	RAM	—
MCP48CVD21	MSOP, QFN, DFN	1	12	7FFh	1	1	RAM	—
MCP48CVD02	QFN	2	8	7Fh	2	2	RAM	—
	MSOP, DFN	2	8	7Fh	1	1	RAM	—
MCP48CVD12	QFN	2	10	1FFh	2	2	RAM	—
	MSOP, DFN	2	10	1FFh	1	1	RAM	—
MCP48CVD22	QFN	2	12	7FFh	2	2	RAM	—
	MSOP, DFN	2	12	7FFh	1	1	RAM	—
MCP48CMD01	MSOP, QFN, DFN	1	8	7Fh	1	1	MTP	8
MCP48CMD11	MSOP, QFN, DFN	1	10	1FFh	1	1	MTP	8
MCP48CMD21	MSOP, QFN, DFN	1	12	7FFh	1	1	MTP	8
MCP48CMD02	QFN	2	8	7Fh	2	2	MTP	8
	MSOP, DFN	2	8	7Fh	1	1	MTP	8
MCP48CMD12	QFN	2	10	1FFh	2	2	MTP	8
	MSOP, DFN	2	10	1FFh	1	1	MTP	8
MCP48CMD22	QFN	2	12	7FFh	2	2	MTP	8
	MSOP, DFN	2	12	7FFh	1	1	MTP	8

Note 1: The factory default value.

2: Each nonvolatile memory location can be written 32 times. For subsequent writes to the MTP, the device will ignore the commands and the memory will not be modified.

3: If the product is a dual device and the package has only one $\overline{LAT}$ pin, it is associated with both DAC0 and DAC1.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

Voltage on V_{DD} with Respect to V_{SS}	-0.6V to +6.5V
Voltage on all Pins with Respect to V_{SS}	-0.6V to V_{DD}+0.3V
Input Clamp Current, I_{IK} ($V_I < 0$, $V_I > V_{DD}$, $V_I > V_{PP}$ on HV Pins)	±20 mA
Output Clamp Current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	±20 mA
Maximum Current out of the V_{SS} Pin (Single)	50 mA
(Dual)	100 mA
Maximum Current into the V_{DD} Pin (Single)	50 mA
(Dual)	100 mA
Maximum Current Sourced by the V_{OUT} Pin	20 mA
Maximum Current Sunk by the V_{OUT} Pin	20 mA
Maximum Current Sourced/Sunk by the $V_{REF(0)}$ Pin (in Band Gap mode)	20 mA
Maximum Current Sunk by the V_{REFx} Pin (when V_{REF} is in Unbuffered mode)	175 µA
Maximum Current Sourced by the V_{REFx} Pin	20 µA
Maximum Current Sunk by the V_{REF} Pin	125 µA
Maximum Output Current Sunk by SDO Output Pin	25 mA
Maximum Output Current Sourced by SDO Output Pin	25 mA
Total Power Dissipation(1)	400 mW
ESD Protection on all Pins	≥ ±6 kV (HBM)
	≥ ±400V (MM)
	≥ ±2 kV (CDM)
Latch-Up (per JEDEC® JESD78A) at +125°C	±100 mA
Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Soldering Temperature of Leads (10 seconds)	+300°C
Maximum Junction Temperature (T_J)	+150°C

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Power dissipation is calculated as follows:

$$P_{DIS} = V_{DD} \times \{I_{DD} - \Sigma I_{OH}\} + \Sigma \{(V_{DD} - V_{OH}) \times I_{OH}\} + \Sigma(V_{OL} \times I_{OL})$$

DC CHARACTERISTICS

Standard Operating Conditions (unless otherwise specified): Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Supply Voltage	V_{DD}	2.7	—	5.5	V	—
		1.8	—	2.7	V	DAC operation (reduced analog specifications) and serial interface
V_{DD} Voltage (rising) to Ensure Device Power-on Reset	V_{POR}	—	—	1.75	V	RAM retention voltage (V_{RAM}) < V_{POR} V_{DD} voltages greater than the V_{POR} limit ensure that the device is out of reset
V_{DD} Voltage (falling) to Ensure Device Brown-out Reset	V_{BOR}	V_{RAM}	—	1.61	V	RAM retention voltage (V_{RAM}) < V_{BOR}
V_{DD} Rise Rate to Ensure Power-on Reset	V_{DDRR}	**Note 3**			V/ms	—
Power-on Reset to Output-Driven Delay (**Note 1**)	T_{POR2OD}	—	—	130	µs	V_{DD} rising, V_{DD} > V_{POR} single output
		—	—	145	µs	V_{DD} rising, V_{DD} > V_{POR} dual output

Note 1 This parameter is ensured by design.

Note 3 POR/BOR voltage trip point is not slope dependent. Hysteresis implemented with time delay.

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V,
R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions		
Supply Current	I_{DD}	—	—	190	µA	Single	1 MHz	Serial Interface Active VRxB:VRxA = `10`(4), V_{OUT} is unloaded, $V_{REF} = V_{DD}$ = 5.5V Volatile DAC register = mid-scale
		—	—	530			10 MHz(2)	
		—	—	1270			50 MHz(2)	
		—	—	290	µA	Dual	1 MHz	
		—	—	630			10 MHz(2)	
		—	—	1370			50 MHz(2)	
		—	—	140	µA	Single	Serial Interface Inactive VRxB:VRxA = `10`, $V_{REF} = V_{DD}$ = 5.5V SCK = SDI = V_{SS}, V_{OUT} is unloaded, Volatile DAC register = mid-scale	
		—	—	240	µA	Dual		
$\overline{\text{LAT}}$/HVC Pin Write Current(1)	$I_{DD(MTP\_WR)}$	—	—	6.40	mA	—	Serial Interface Inactive (MTP Write Active), VRxB:VRxA = `10` (valid for all modes) V_{DD} = 5.5V, $\overline{\text{LAT}}$/HVC = V_{IHH}, Write all ‘`1`’s to nonvolatile DAC0, V_{OUT} pins are unloaded.	
Power-Down Current	I_{DDP}	—	0.5	2.4	µA	—	PDxB:PDxA = `01`(5), VRxB:VRxA = `10`, V_{OUT} not connected	

Note 1 This parameter is ensured by design.

Note 2 This parameter is ensured by characterization.

Note 4 Supply current is independent of current through the resistor ladder in mode VRxB:VRxA = `10`.

Note 5 The PDxB:PDxA = `01`, `10` and `11` configurations must have the same current.

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C $\leq T_A \leq$ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V,
R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Resistor Ladder Resistance(6)	R_L	62.475	73.5	84.525	kΩ	VRxB:VRxA = `10`, $V_{REF} = V_{DD}$	
Resolution (# of Resistors and # of Taps) (see **B.1 “Resolution”**)	N		256		Taps	8-bit	No Missing Codes
			1024		Taps	10-bit	No Missing Codes
			4096		Taps	12-bit	No Missing Codes
Nominal V_{OUT} Match(10)	$\lvert V_{OUT} - V_{OUTMEAN}\rvert / V_{OUTMEAN}$	—	0.026	0.3	%	1.8V $\leq V_{DD} \leq$ 5.5V(2)	
V_{OUT} Tempco(2) (see **B.19 “V_{OUT} Temperature Coefficient”**)	$\Delta V_{OUT}/\Delta T$	—	3	—	ppm/°C	Code = mid-scale (7Fh, 1FFh or 7FFh), VRxB:VRxA = `00`, `10` and `11`	
V_{REF} Pin Input Voltage Range	V_{REF}	V_{SS}	—	V_{DD}	V	1.8V $\leq V_{DD} \leq$ 5.5V(1)	

Note 1 This parameter is ensured by design.

Note 2 This parameter is ensured by characterization.

Note 6 Resistance is defined as the resistance between the V_{REF} pin (mode VRxB:VRxA = `10`) and the V_{SS} pin. For dual channel devices (MCP48CXDX2), this is the effective resistance of each resistor ladder. The resistance measurement is one of the two resistor ladders measured in parallel.

Note 10 Variation of one output voltage to mean output voltage for dual devices only.

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V,
R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Zero-Scale Error (Code = 000h) (see **B.5 "Zero-Scale Error (EZS)"**)	E_{ZS}	—	—	0.5	LSb	8-bit	VRxB:VRxA = `10`, G = `0`, V_{REF} = V_{DD}, No Load.
		—	—	2	LSb	10-bit	VRxB:VRxA = `10`, G = `0`, V_{REF} = V_{DD}, no load
		—	—	8	LSb	12-bit	VRxB:VRxA = `10`, G = `0`, V_{REF} = V_{DD}, no load
Offset Error (see **B.7 "Offset Error (EOS)"**)	E_{OS}	-9	±1.1	+9	mV	VRxB:VRxA = `10`, Gx = `0`, no load 8-bit: Code = 4; 10-bit: Code = 16; 12-bit: Code = 64	
Offset Voltage Temperature Coefficient[2, 9]	V_{OSTC}	—	±9	—	µV/°C	—	
Full-Scale Error (see **B.4 "Full-Scale Error (EFS)"**)	E_{FS}	—	—	0.625	LSb	8-bit	VRxB:VRxA = `10`, G = `0`, V_{REF} = V_{DD}, no load
		—	—	2.5	LSb	10-bit	VRxB:VRxA = `10`, G = `0`, V_{REF} = V_{DD}, no load
		—	—	10	LSb	12-bit	VRxB:VRxA = `10`, G = `0`, V_{REF} = V_{DD}, no load
Gain Error[7] (see **B.9 "Gain Error (EG)"**)	E_G	-0.6	±0.1	+0.6	% of FSR	8-bit	VRxB:VRxA = `10`, G = `0`, Code = 252, V_{REF} = V_{DD}, no load
		-0.6	±0.1	+0.6	% of FSR	10-bit	VRxB:VRxA = `10`, G = `0`, Code = 1008, V_{REF} = V_{DD}, no load
		-0.6	±0.1	+0.6	% of FSR	12-bit	VRxB:VRxA = `10`, G = `0`, Code = 4032, V_{REF} = V_{DD}, no load
Gain-Error Drift[2] (see **B.10 "Gain Error Drift (EGD)"**)[9]	ΔG/°C	—	-10	—	ppm/°C	—	

Note 2 This parameter is ensured by characterization.

Note 7 This gain error does not include the offset error.

Note 9 Code range dependent on resolution: 8-bit, codes 4 to 252; 10-bit, codes 16 to 1008; 12-bit, codes 64 to 4032.

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V,
R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions		
Total Unadjusted Error (2, 9) (see **B.6 "Total Unadjusted Error (ET)"**)	E_T	-1.375	—	0.625	LSb	8-bit	VRxB:VRxA = `10`, G = `0`, V_{REF} = V_{DD}, no load	
		-5.5	—	2.5	LSb	10-bit	VRxB:VRxA = `10`, G = `0`, V_{REF} = V_{DD}, no load	
		-22	—	10	LSb	12-bit	VRxB:VRxA = `10`, G = `0`, V_{REF} = V_{DD}, no load	
		See **Section 2.0 "Typical Performance Curves"**			LSb	12-bit	VRxB:VRxA = `00` No Load	V_{DD} = 1.8-5.5V V_{REF} = V_{DD}, G = `0`
							VRxB:VRxA = `01` No Load	V_{DD} = 1.8-5.5V, G = `0`, V_{REF} = V_{BG} = 1.2V (typ.)
								V_{DD} = 2.7-5.5 V, G = `1`, V_{REF} = V_{BG} = 1.2V (typ.)
							VRxB:VRxA = `10` VRxB:VRxA = `11` No Load	V_{DD} = 1.8-5.5 V V_{REF} = V_{DD}, G = `0`
								V_{DD} = 2.7-5.5 V V_{REF} = 0.5 x V_{DD}, G = `1`
Integral Nonlinearity(9) (see **B.11 "Integral Nonlinearity (INL)"**)	INL	-0.10	—	+0.10	LSb	8-bit	VRxB:VRxA = `10`, G = `0`, V_{REF} = V_{DD}, no load	
		-0.25	—	+0.25	LSb	10-bit	VRxB:VRxA = `10`, G = `0`, V_{REF} = V_{DD}, no load	
		-1	—	+1	LSb	12-bit	VRxB:VRxA = `10`, G = `0`, V_{REF} = V_{DD}, no load	
		See **Section 2.0 "Typical Performance Curves"**			LSb	12-bit	VRxB:VRxA = `00` No Load	V_{DD} = 1.8-5.5V V_{REF} = V_{DD}, G = `0`
							VRxB:VRxA = `01` No Load	V_{DD} = 1.8-5.5V, G = `0`, V_{REF} = V_{BG} = 1.2V (typ.)
								V_{DD} = 2.7-5.5 V, G = `1`, V_{REF} = V_{BG} = 1.2V (typ.)
							VRxB:VRxA = `10` VRxB:VRxA = `11` No Load	V_{DD} = 1.8-5.5 V V_{REF} = V_{DD}, G = `0`
								V_{DD} = 2.7-5.5 V V_{REF} = 0.5 x V_{DD}, G = `1`

Note 2 This parameter is ensured by characterization.

Note 9 Code range dependent on resolution: 8-bit, codes 4 to 252; 10-bit, codes 16 to 1008; 12-bit, codes 64 to 4032.

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V,
R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions		
Differential Nonlinearity[9] (see **B.12 "Differential Nonlinearity (DNL)"**)	DNL	-0.1	—	+0.1	LSb	8-bit	VRxB:VRxA = `10`, G = `0`, V_{REF} = V_{DD}, no load	
		-0.25	—	+0.25	LSb	10-bit	VRxB:VRxA = `10`, G = `0`, V_{REF} = V_{DD}, no load	
		-1.0	—	+1.0	LSb	12-bit	VRxB:VRxA = `10`, G = `0`, V_{REF} = V_{DD}, no load	
		See **Section 2.0 "Typical Performance Curves"**			LSb	12-bit	VRxB:VRxA = `00` No Load	V_{DD} = 1.8-5.5V V_{REF} = V_{DD}, G = `0`
							VRxB:VRxA = `01` No Load	V_{DD} = 1.8-5.5V, G = `0`, V_{REF} = V_{BG} = 1.2V (typ.)
								V_{DD} = 2.7-5.5 V, G = `1`, V_{REF} = V_{BG} = 1.2V (typ.)
							VRxB:VRxA = `10` VRxB:VRxA = `11` No Load	V_{DD} = 1.8-5.5 V V_{REF} = V_{DD}, G = `0`
								V_{DD} = 2.7-5.5 V V_{REF} = 0.5 x V_{DD}, G = `1`

Note 9 Code range dependent on resolution: 8-bit, codes 4 to 252; 10-bit, codes 16 to 1008; 12-bit, codes 64 to 4032.

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C $\le T_A \le$ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V,
R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
-3 dB Bandwidth (see **B.16 "-3 dB Bandwidth"**)	BW	—	270	—	kHz	V_{REF} = 3.0V+/-2V, VRxB:VRxA = `10`, Gx = `0`	
		—	170	—	kHz	V_{REF} = 3.5V+/-1.5V, VRxB:VRxA = `10`, Gx = `1`	
Output Amplifier (Op Amp)							
Phase Margin[(1)]	PM	—	76	—	°	$R_L = \infty$	
Slew Rate	SR	—	0.7	—	V/µs	R_L = 2 kΩ	
Load Regulation	—	—	147	—	µV/mA	1 mA < I < 6 mA	V_{DD} = 5.5V, DAC code = mid-scale
		—	300	—	µV/mA	-6 mA < I < -1 mA	
Short-Circuit Current	I_{SC_OA}	6	10	14	mA	Short to V_{SS}	DAC code = full-scale
		6	10	14	mA	Short to V_{DD}	DAC code = zero-scale
Settling Time[(8)]	$t_{SETTLING}$	—	4	—	µs	R_L = 2 kΩ	
Internal Band Gap							
Band Gap Voltage	V_{BG}	1.180	1.214	1.260	V	1.8 < V_{DD} < 5.5V	
Short-Circuit Current	I_{SC_BG}	6	10	14	mA	Short to V_{SS}	
		6	10	14	mA	Short to V_{DD}	
Band Gap Voltage Temperature Coefficient	V_{BGTC}	—	18	—	ppm/°C	1.8V $\le V_{DD}$ < 5.5V	
Band Gap Mode V_{REF} Pin Load Regulation	I_{BG}	—	52	—	µV/mA	1 mA < I < 6 mA	V_{DD} = 5.5V, DAC code = mid-scale
		—	374	—	µV/mA	-6 mA < I < -1 mA	

Note 1 This parameter is ensured by design.

Note 8 Within 1/2 LSb of the final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in a 12-bit device.)

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V,
R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
External Reference (V_{REF})						
Input Range[1]	V_{REF}	V_{SS}	—	V_{DD}	V	VRxB:VRxA = `10` (Unbuffered mode)
Input Capacitance	C_{REF}	—	29	—	pF	VRxB:VRxA = `10` (Unbuffered mode)
Input Impedance	R_L	See Resistor Ladder Resistance(6)			kΩ	2.7V <= V_{DD} <= 5.5V VRxB:VRxA = `10` V_{REF} = V_{DD}
Current through V_{REF}[1]	I_{VREF}	—	—	176.07	µA	Mathematically from $R_{VREF(min)}$ spec (at 5.5V)
Total Harmonic Distortion[1]	THD	—	-76	—	dB	V_{REF} = 2.048V ± 0.1V, VRxB:VRxA = `10`, Gx = `0`, Frequency = 1 kHz
Dynamic Performance						
Major Code Transition Glitch (see **B.14 "Major-Code Transition Glitch"**)	—	—	60	—	nV-s	1 LSb change around major carry (7FFh to 800h)
Digital Feedthrough (see **B.15 "Digital Feed-Through"**)	—	—	<2	—	nV-s	—

Note 1 This parameter is ensured by design.

Note 6 Resistance is defined as the resistance between the V_{REF} pin (mode VRxB:VRxA = `10`) and the V_{SS} pin. For dual channel devices (MCP48CXDX2), this is the effective resistance of each resistor ladder. The resistance measurement is one of the two resistor ladders measured in parallel.

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V,
R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Digital Inputs/Outputs ($\overline{CS}$, SDI, SDO, SCK, $\overline{LAT}$x)							
Schmitt Trigger High-Input Threshold	V_{IH}	0.45 V_{DD}	—	—	V	1.8V ≤ V_{DD} ≤ 5.5V (allows 2.7V digital V_{DD} with 5.5V analog V_{DD} or 1.8V digital V_{DD} with 3.0V analog V_{DD})	
Schmitt Trigger Low-Input Threshold	V_{IL}	—	—	0.2 V_{DD}	V	—	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	0.1 V_{DD}	—	V	—	
Output Low Voltage (SDO)	V_{OL}	V_{SS}	—	0.3 V_{DD}	V	I_{OL} = 200 µA	
Output High Voltage (SDO)	V_{OH}	0.7 V_{DD}	—	V_{DD}	V	I_{OH} = -200 µA	
Input Leakage Current	I_{IL}	-1	—	1	µA	V_{IN} = V_{DD} and V_{IN} = V_{SS}	
Pin Capacitance	C_{IN}, C_{OUT}	—	10	—	pF	—	
RAM Value							
Value Range	N	0h	—	FFh	hex	8-bit	—
		0h	—	3FFh	hex	10-bit	—
		0h	—	FFFh	hex	12-bit	—
DAC Register POR/BOR Value	N	See **Table 4-2**			hex	8-bit	—
		See **Table 4-2**			hex	10-bit	—
		See **Table 4-2**			hex	12-bit	—
PDCON Initial Factory Setting	—	See **Table 4-2**			hex	—	
Power Requirements							
Power Supply Sensitivity (**B.17 "Power-Supply Sensitivity (PSS)"**)	PSS	—	0.0010	0.0070	%/%	8-bit	Code = mid-scale
						10-bit	
						12-bit	

DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V,
R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Multi-Time Programming Memory (MTP)						
MTP Programming Voltage (**Note 1**)	V_{PG_MTP}	2.0	—	5.5	V	HVC = V_{IHH}, -20°C ≤ T_A ≤ +125°C
$\overline{\text{LAT}}$/HVC pin Voltage for MTP Programming (High-Voltage Commands)(1)	V_{IHH}	7.25	7.5	7.75V	V	The $\overline{\text{LAT}}$/HVC pin will be at one of the three input levels (V_{IL}, V_{IH} or V_{IHH})(1,11) The $\overline{\text{LAT}}$/HVC pin must supply the required MTP programming current (up to 6.4 mA).
Writes Cycles	—	—	—	32(12)	Cycles	**Note 1**
Data Retention	DR_{MTP}	10	—	—	Years	at +85°C(1)
MTP Range	N	0h	—	FFh	hex	8-bit
		0h	—	3FFh	hex	10-bit
		0h	—	FFFh	hex	12-bit
		0000h		7FFFh	hex	All general purpose memory
Initial Factory Setting	N	See **Table 4-2**			—	—
MTP Programming Write Cycle Time	$t_{WC(MTP)}$	—	—	250	us	V_{DD} = +2.0V to 5.5V, -20°C ≤ T_A ≤ +125°C (**Note 1**)

Note 1 This parameter is ensured by design.

Note 11 High voltage on the LAT/HVC pin must be limited to the command plus programming time. After the programming cycle, the LAT/HVC pin voltage must be returned to 5.5V or lower.

Note 12 After 32 MTP write cycles, writes are inhibited and the 32nd write value is retained (not corrupted).

DC Characteristics Notes:

1. This parameter is ensured by design.
2. This parameter is ensured by characterization.
3. POR/BOR voltage trip point is not slope dependent. Hysteresis implemented with time delay.
4. Supply current is independent of current through the resistor ladder in mode VRxB:VRxA = `10`.
5. The PDxB:PDxA = `01`, `10` and `11` configurations must have the same current.
6. Resistance is defined as the resistance between the V_{REF} pin (mode VRxB:VRxA = `10`) and the V_{SS} pin. For dual channel devices (MCP48CXDX2), this is the effective resistance of each resistor ladder. The resistance measurement is one of the two resistor ladders measured in parallel.
7. This gain error does not include the offset error.
8. Within 1/2 LSb of the final value when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in a 12-bit device.)
9. Code range dependent on resolution: 8-bit, codes 4 to 252; 10-bit, codes 16 to 1008; 12-bit, codes 64 to 4032.
10. Variation of one output voltage to mean output voltage for dual devices only.
11. High voltage on the $\overline{\text{LAT}}$/HVC pin must be limited to the command plus programming time. After the programming cycle, the $\overline{\text{LAT}}$/HVC pin voltage must be returned to 5.5V or lower.
12. After 32 MTP write cycles, writes are inhibited and the 32nd write value is retained (not corrupted).

1.1 Timing Waveforms and Requirements

1.1.1 WIPER SETTLING TIME

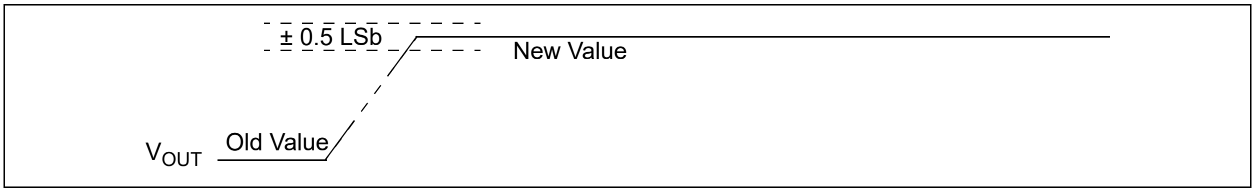


FIGURE 1-1: *V_{OUT} Settling Time Waveforms.*

TABLE 1-1: WIPER SETTLING TIMING

Timing Characteristics	**Standard Operating Conditions (unless otherwise specified)**: Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{SS} = 0V, R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
V_{OUT} Settling Time (see **B.13 “Settling Time”**)	t_S	—	4	—	µs	12-bit	Code = 400h → C00h; C00h → 400h[3]

Note 3 Within 1/2 LSb of the final value when code changes from 1/4 to 3/4 of FSR.

1.1.2 LATCH PIN ($\overline{\text{LAT}}$) TIMING

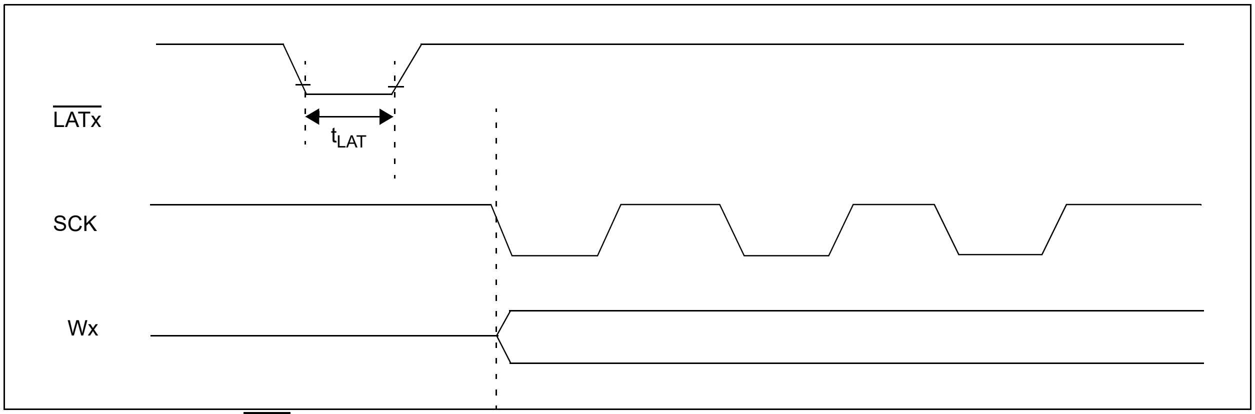


FIGURE 1-2: *$\overline{\text{LAT}}$ Pin Waveforms.*

TABLE 1-2: $\overline{\text{LAT}}$ PIN TIMING

Timing Characteristics	**Standard Operating Conditions (unless otherwise specified)**: Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges unless noted. V_{DD} = +2.7V to 5.5V, V_{SS} = 0V, RL = 2 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.					
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
$\overline{\text{LATx}}$ Pin Pulse Width	t_{LAT}	20	—	—	ns	—

1.1.3 RESET AND POWER-DOWN TIMING

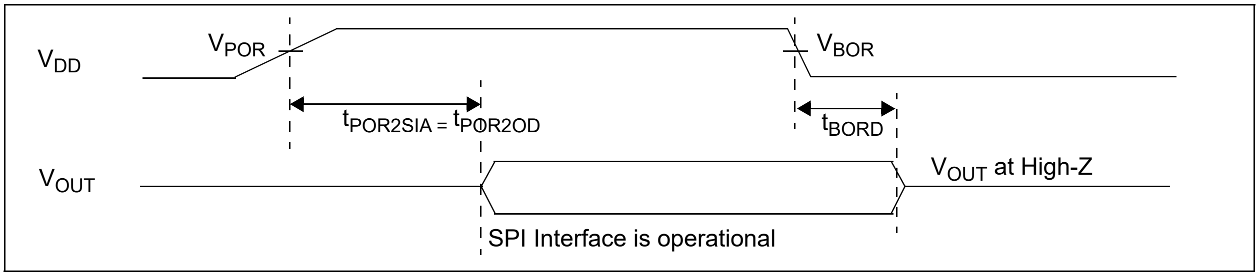


FIGURE 1-3: *Power-on and Brown-out Reset Waveforms.*

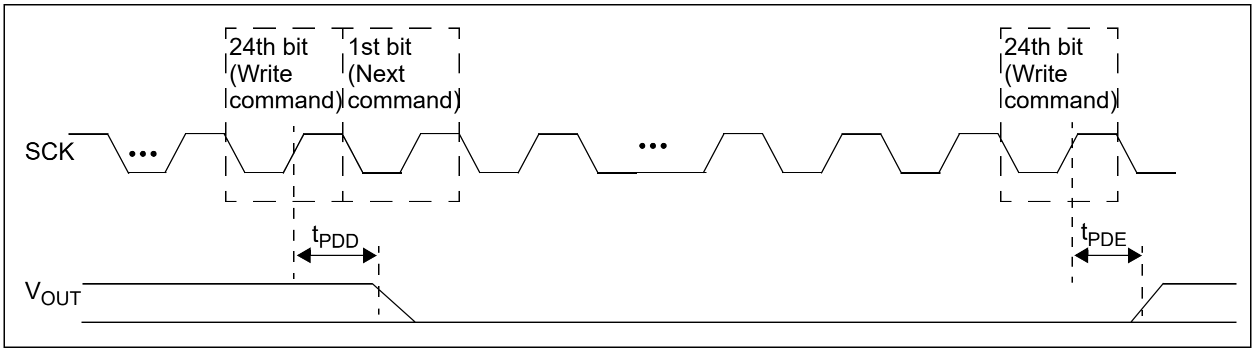


FIGURE 1-4: *SPI Power-Down Waveforms.*

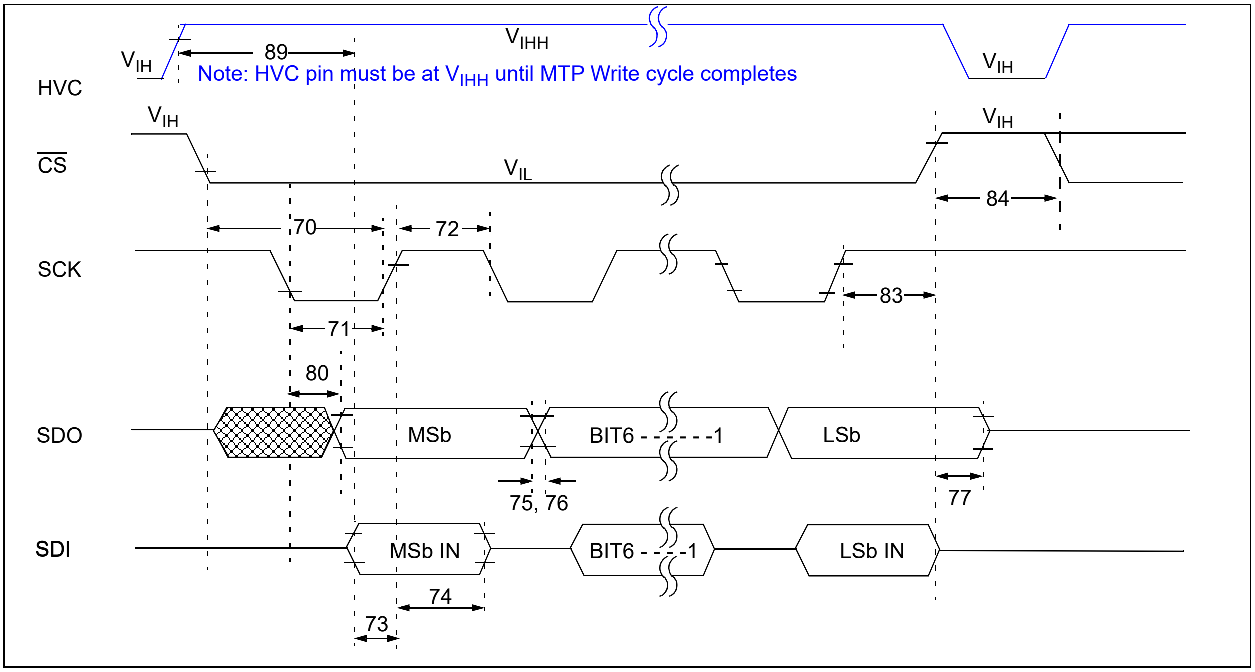
TABLE 1-3: RESET AND POWER-DOWN TIMING

Timing Characteristics	**Standard Operating Conditions (unless otherwise specified)**: Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended) All parameters apply across the specified operating ranges, unless noted. V_{DD} = +2.7V to 5.5V, V_{SS} = 0V, RL = 2 kΩ from V_{OUT} to GND, C_L = 100 pF. Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions	
Power-on Reset Delay[1]	$t_{POR2SIA}$	—	—	130	µs	Single	V_{DD} transitions from $V_{DD(MIN)}$ → > V_{POR}; V_{OUT} disabled to V_{OUT} driven
		—	—	145		Dual	
Brown-out Reset Delay	t_{BORD}	—	30	—	µs	V_{DD} transitions from $V_{DD(MIN)}$ → V_{DD}> V_{POR}, V_{OUT} driven to V_{OUT} disabled	
Power-Down Output Disable Time Delay	T_{PDD}	—	0.02	—	µs	PDxB:PDxA = `00` → `11`, `10` or `01` started from the rising edge of the 24th SCK clock cycle; V_{OUT} = V_{OUT} – 10 mV, V_{OUT} not connected	
Power-Down Output Enable Time Delay	T_{PDE}	—	7	—	µs	PDxB:PDxA = `11`, `10`, or `01` → `00` started from the rising edge of the 24th SCK clock cycle; Volatile DAC register = FFFh, V_{OUT} = 10 mV, V_{OUT} not connected	

Note 1 This parameter is ensured by design.

1.2 SPI Mode Timing Waveforms and Requirements



Note: HVC pin must be at V_{IHH} until MTP Write cycle completes

FIGURE 1-5: *SPI Timing Waveform (Mode = `11`).*

TABLE 1-4: SPI REQUIREMENTS (MODE = `11`)

#	Characteristic(2)	Sym.	Min.	Max.	Units	Conditions
—	SCK Input Frequency	F_{SCK}	—	25	MHz	V_{DD} = 2.7V to 5.5V – read command, C_L = 20 pF
			—	50	MHz	V_{DD} = 2.7V to 5.5V – write commands, C_L = 20 pF
			—	10	MHz	V_{DD} = 1.8V to 2.7V
70	$\overline{\text{CS}}$ Active (V_{IL}) to SCK↑ Input	$T_{csA2scH}$	15	—	ns	—
71	SCK Input High Time	T_{scH}	10	—	ns	V_{DD} = 2.7V to 5.5V
			20	—	ns	V_{DD} = 1.8V to 2.7V
72	SCK Input Low Time	T_{scL}	10	—	ns	V_{DD} = 2.7V to 5.5V
			20	—	ns	V_{DD} = 1.8V to 2.7V
73	SDI Input Valid to SCK↑ Edge (Setup Time)	$T_{DIV2scH}$	5	—	ns	—
74	SCK↑ Edge to SDI Input Invalid (Hold Time)	$T_{scH2DIL}$	10	—	ns	—
77	$\overline{\text{CS}}$ Inactive (V_{IH}) to SDO Output High-Impedance	$T_{csH2DOZ}$	—	20	ns	**Note 1**
80	SCK↓ Edge to SDO Data Output Valid	$T_{scL2DOV}$	—	20	ns	V_{DD} = 2.7V to 5.5V
			—	35	ns	V_{DD} = 1.8V to 2.7V
83	SCK↑ Edge to $\overline{\text{CS}}$ Inactive (V_{IH}) (Hold Time)	$T_{scH2csI}$	15	—	ns	V_{DD} = 2.7V to 5.5V
			20	—	ns	V_{DD} = 1.8V to 2.7V
84	$\overline{\text{CS}}$ Input High Time	$T_{csA2csI}$	30	—	ns	—
89	Delay from HVC V_{IHH} to First Command Byte(1)	—	0	—	ns	—

Note 1 This parameter is ensured by design.

Note 2 This parameter is ensured by characterization.

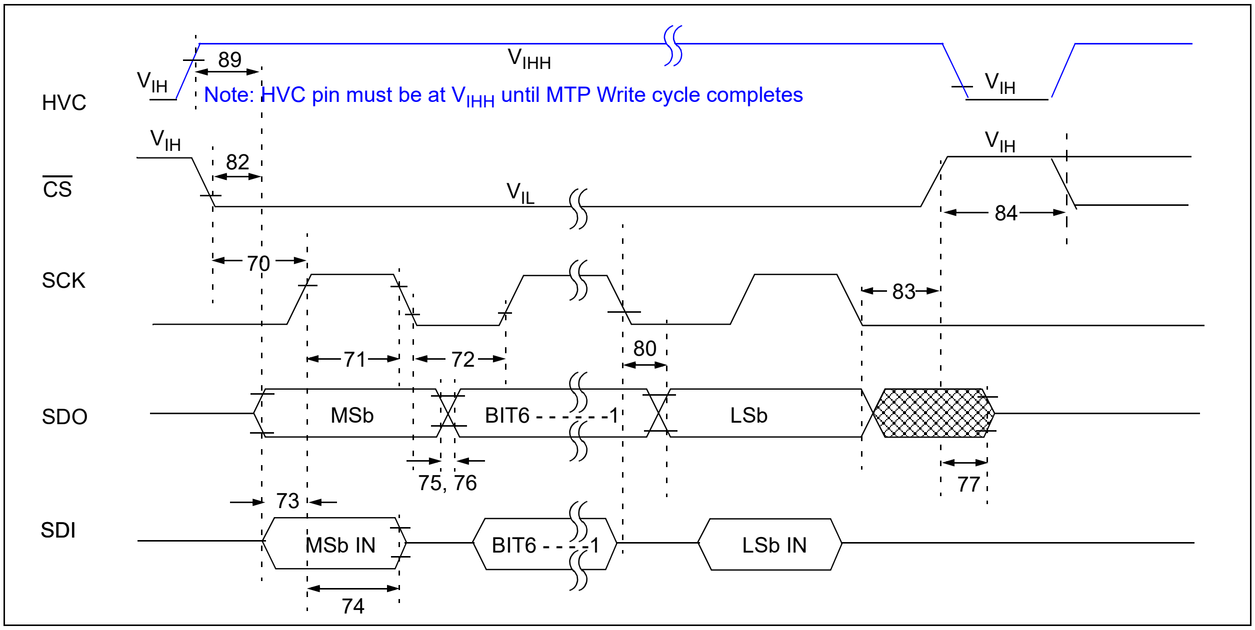


FIGURE 1-6: *SPI Timing Waveform (Mode = 00).*

TABLE 1-5: SPI REQUIREMENTS (MODE = 00)

#	Characteristic[2]	Sym.	Min.	Max.	Units	Conditions
—	SCK Input Frequency	F_{SCK}	—	25	MHz	V_{DD} = 2.7V to 5.5V – read command, C_L = 20 pF
			—	50	MHz	V_{DD} = 2.7V to 5.5V – write commands, C_L = 20 pF
			—	10	MHz	V_{DD} = 1.8V to 2.7V
70	$\overline{CS}$ Active (V_{IL} or V_{IHH}) to SCK↑ Input	$T_{csA2scH}$	15	—	ns	—
71	SCK Input High Time	T_{scH}	10	—	ns	V_{DD} = 2.7V to 5.5V
			20	—	ns	V_{DD} = 1.8V to 2.7V
72	SCK Input Low Time	T_{scL}	10	—	ns	V_{DD} = 2.7V to 5.5V
			20	—	ns	V_{DD} = 1.8V to 2.7V
73	SDI Input Valid to SCK↑ Edge (Setup Time)	$T_{DIV2scH}$	5	—	ns	—
74	SCK↑ Edge to SDI Input Invalid (Hold Time)	$T_{scH2DIL}$	10	—	ns	—
77	$\overline{CS}$ Inactive (V_{IH}) to SDO Output High-Impedance	$T_{csH2DOZ}$	—	20	ns	**Note 1**
80	SCK↓ Edge to SDO Data Output Valid	$T_{scL2DOV}$	—	20	ns	V_{DD} = 2.7V to 5.5V
			—	35	ns	V_{DD} = 1.8V to 2.7V
82	$\overline{CS}$ Active (V_{IL}) to SDO Data Output Valid	$T_{csL2DOV}$	—	20	ns	2.7V to 5.5V
			—	35	ns	1.8V to 2.7V
83	SCK↓ Edge to $\overline{CS}$ Inactive (V_{IH}) (Hold Time)	$T_{scH2csI}$	15	—	ns	V_{DD} = 2.7V to 5.5V
			20	—	ns	V_{DD} = 1.8V to 2.7V
84	$\overline{CS}$ Input High Time	$T_{csA2csI}$	30	—	ns	—
89	Delay from HVC V_{IHH} to First Command Byte[1]	—	0	—	ns	—

Note 1 This parameter is ensured by design.

Note 2 This parameter is ensured by characterization.

Timing Notes:

1. This parameter is ensured by design.
2. This parameter is ensured by characterization.
3. Within 1/2 LSb of the final value when code changes from 1/4 to 3/4 of FSR.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +5.5V, V_{SS} = GND.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	—
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	—
Thermal Package Resistances						
Thermal Resistance, 10L-MSOP	θ_{JA}	—	206	—	°C/W	—
Thermal Resistance, 10L-DFN (3 x 3)	θ_{JA}	—	91	—	°C/W	—
Thermal Resistance, 16L-QFN	θ_{JA}	—	58	—	°C/W	—

Note 1: The MCP48CXDX1/2 devices operate over this extended temperature range, but with reduced performance. Operation in this range must not cause T_J to exceed the Maximum Junction Temperature of +150°C.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and, therefore, outside the warranted range.

2.1 Electrical Data

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

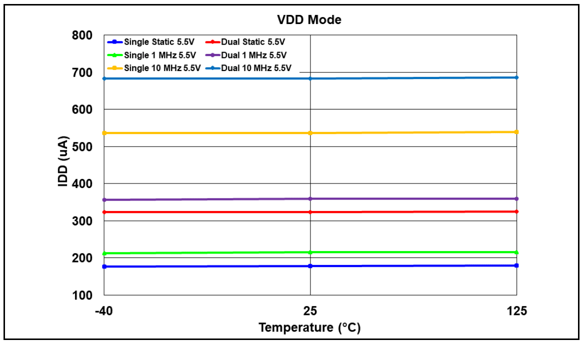


FIGURE 2-1: *Average Device Supply Current vs. F_{SCL} Frequency, Voltage and Temperature – Active Interface, VRxB:VRxA =* `00` *(V_{DD} Mode).*

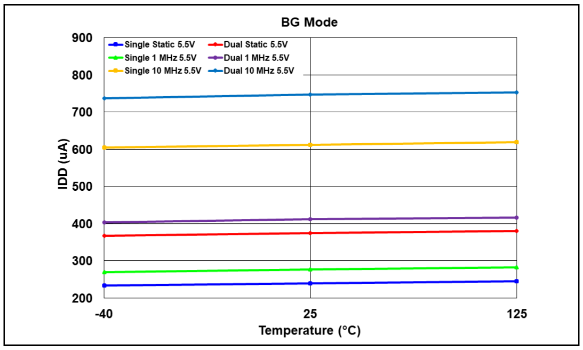


FIGURE 2-2: *Average Device Supply Current vs. F_{SCL} Frequency, Voltage and Temperature – Active Interface, VRxB:VRxA =* `01` *(Band Gap Mode).*

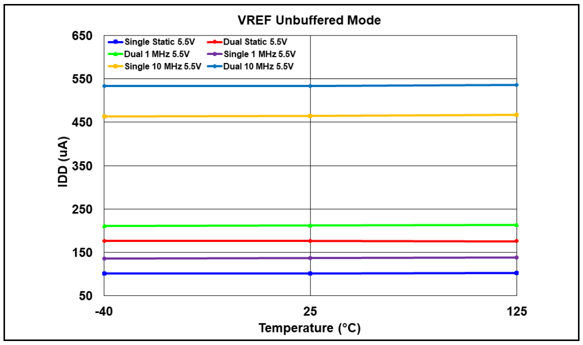


FIGURE 2-3: *Average Device Supply Current vs. F_{SCL} Frequency, Voltage and Temperature – Active Interface, VRxB:VRxA =* `10` *(V_{REF} Unbuffered Mode).*

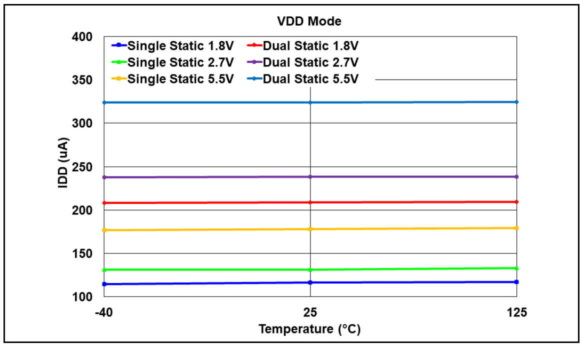


FIGURE 2-4: *Average Device Supply Current vs. Voltage and Temperature – Inactive Interface (SCL = V_{IH} or V_{IL}), VRxB:VRxA =* `00` *(V_{DD} Mode).*

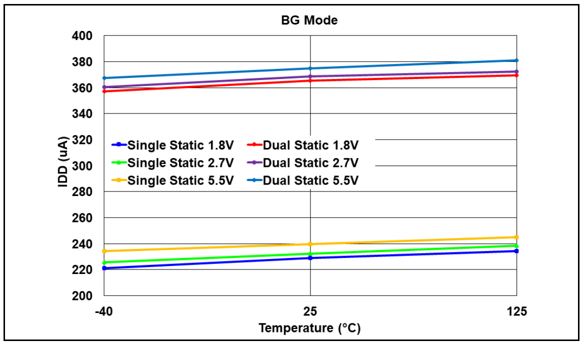


FIGURE 2-5: *Average Device Supply Current vs. Voltage and Temperature – Inactive Interface (SCL = V_{IH} or V_{IL}), VRxB:VRxA =* `01` *(Band Gap Mode).*

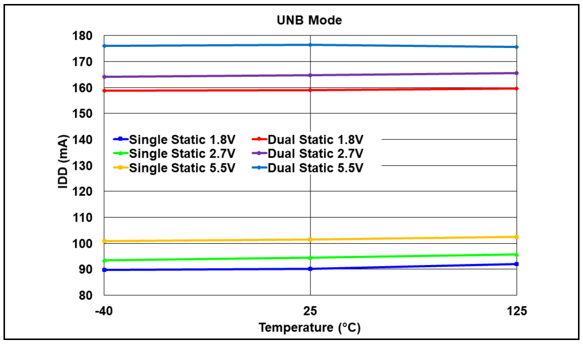


FIGURE 2-6: *Average Device Supply Current vs. Voltage and Temperature – Inactive Interface (SCL = V_{IH} or V_{IL}), VRxB:VRxA =* `10` *(V_{REF} Unbuffered Mode).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = 5.5V.

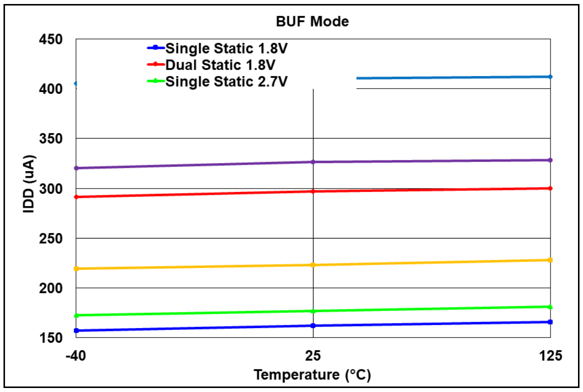


FIGURE 2-7: *Average Device Supply Current vs. F_{SCL} Frequency, Voltage and Temperature – Active Interface, VRxB:VRxA = `11` (V_{REF} Buffered Mode).*

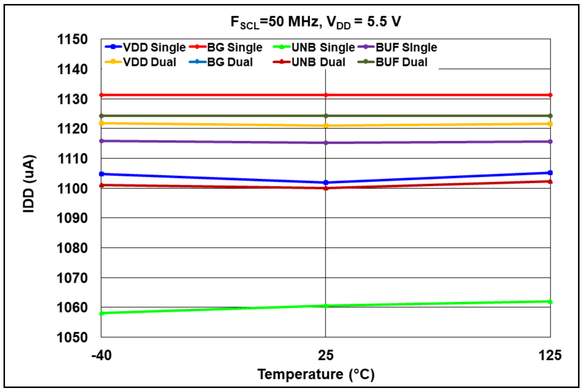


FIGURE 2-8: *Average Device Supply Active Current (I_{DDA}) (at 5.5V and F_{SCK} = 50MHz) vs. Temperature and DAC Reference Voltage Mode.*

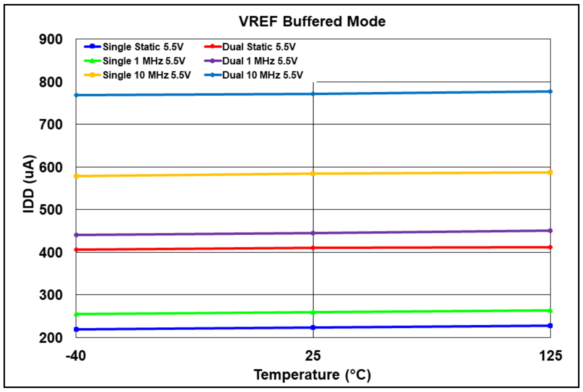


FIGURE 2-9: *Average Device Supply Current vs. Voltage and Temperature – Inactive Interface (SCL = V_{IH} or V_{IL}), VRxB:VRxA = `11` (V_{REF} Buffered Mode).*

2.2 Linearity Data

2.2.1 TOTAL UNADJUSTED ERROR (TUE) – V_{DD} MODE (VRXB:VRXA = `00`) MCP48CXD22 (12-BIT), CODE 64-4032

Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = 5.5V.

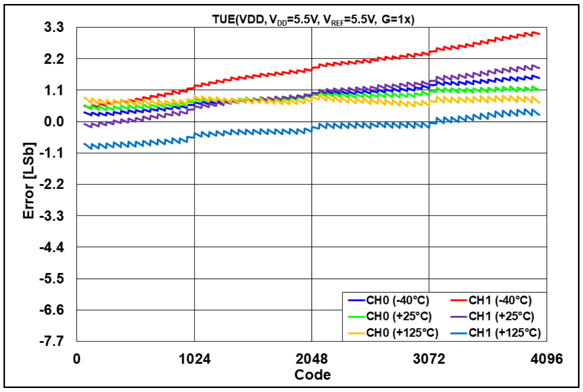


FIGURE 2-10: *TUE (V_{OUT}) vs. DAC Code and Temperature, V_{REF} = V_{DD} = 5.5V, G = 1x.*

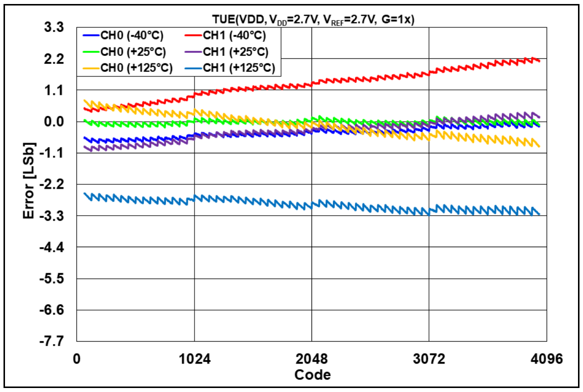


FIGURE 2-11: *TUE (V_{OUT}) vs. DAC Code and Temperature, V_{REF} = V_{DD} = 2.7V, G = 1x.*

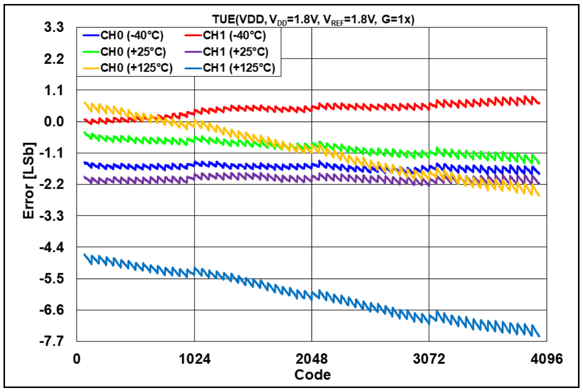


FIGURE 2-12: *TUE (V_{OUT}) vs. DAC Code and Temperature, V_{REF} = V_{DD} = 1.8V, G = 1x.*

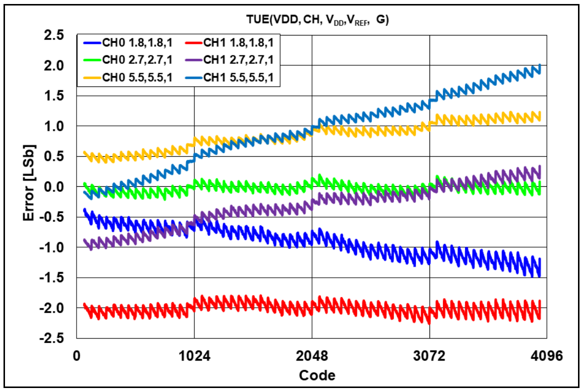


FIGURE 2-13: *TUE (V_{OUT}) vs. DAC Code, Temperature = +25°C.*

2.2.2 TOTAL UNADJUSTED ERROR (TUE) – INTERNAL BAND GAP MODE (VRXB:VRXA = `01`), MCP48CXD22 (12-BIT), CODE 64-4032

Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = 5.5V.

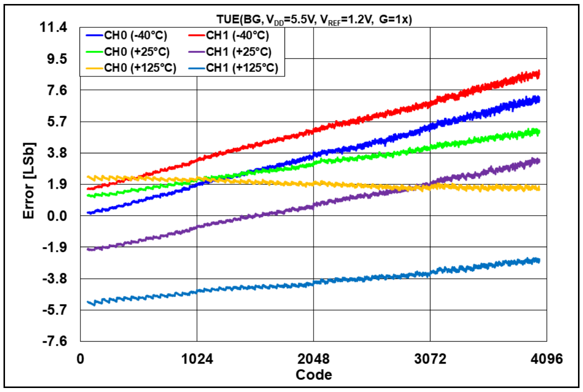


FIGURE 2-14: *TUE (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V,* V_{REF} = 1.2V, G = 1x.

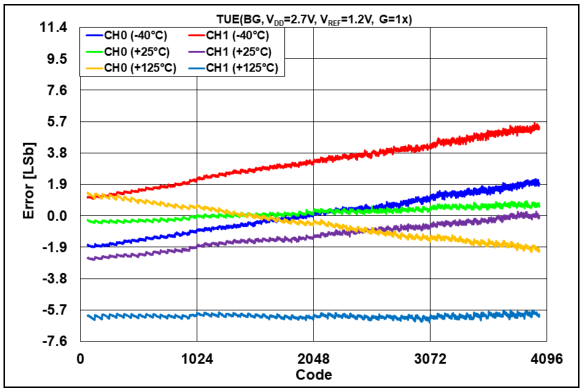


FIGURE 2-15: *TUE (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V,* V_{REF} = 1.2V, G = 1x.

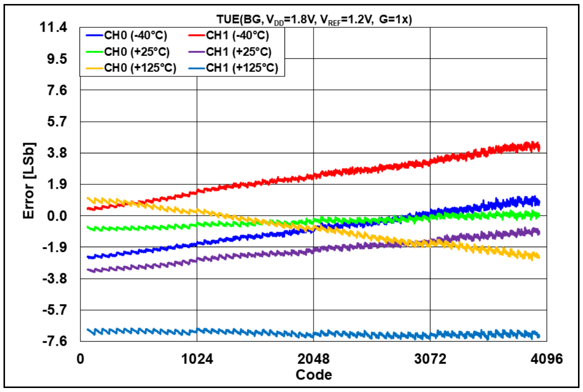


FIGURE 2-16: *TUE (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 1.8V,* V_{REF} = 1.2V, G = 1x.

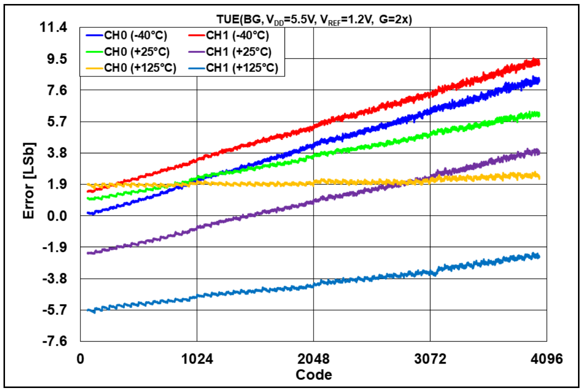


FIGURE 2-17: *TUE (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V,* V_{REF} = 1.2V, G = 2x.

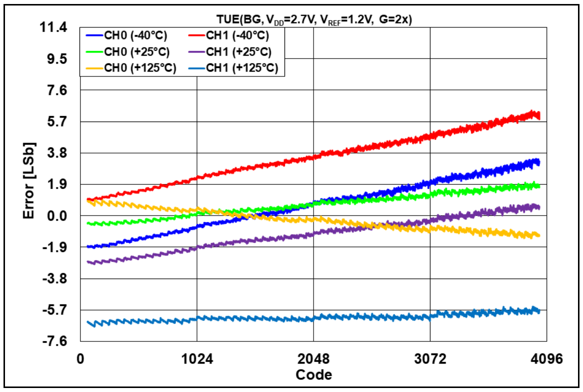


FIGURE 2-18: *TUE (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V,* V_{REF} = 1.2V, G = 2x.

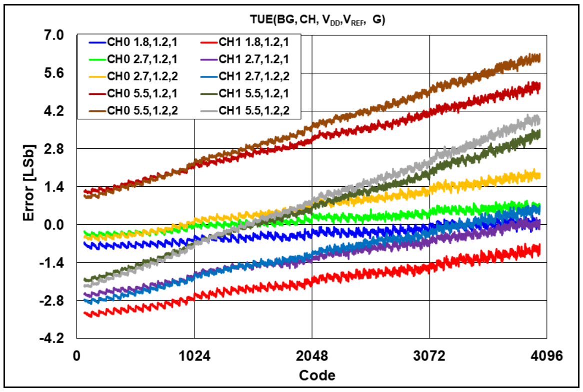


FIGURE 2-19: *TUE (V_{OUT}) vs. DAC Code, Temperature = +25°C.*

2.2.3 TOTAL UNADJUSTED ERROR (TUE) – EXTERNAL UNBUFFERED V_{REF} MODE (VRXB:VRXA = `10`), MCP48CXD22 (12-BIT), CODE 64-4032

Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = 5.5V.

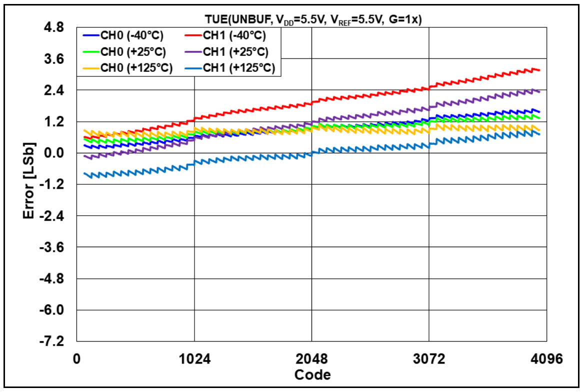


FIGURE 2-20: *TUE (V_{OUT}) vs. DAC Code and Temperature, V_{REF} = V_{DD} = 5.5V, G = 1x.*

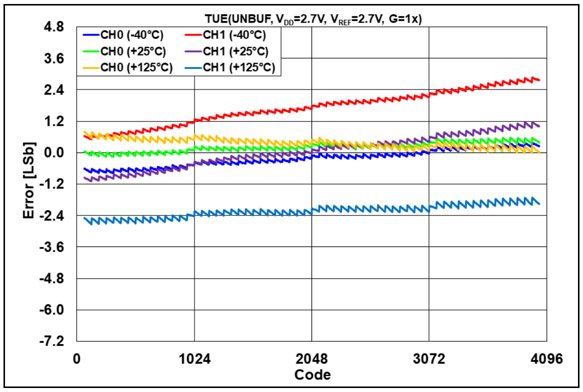


FIGURE 2-21: *TUE (V_{OUT}) vs. DAC Code and Temperature, V_{REF} = V_{DD} = 2.7V, G = 1x.*

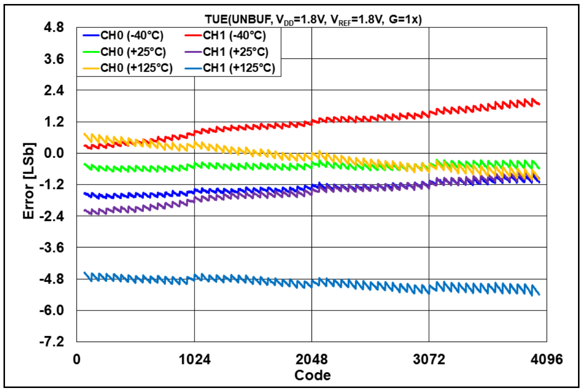


FIGURE 2-22: *TUE (V_{OUT}) vs. DAC Code and Temperature, V_{REF} = V_{DD} = 1.8V, G = 1x.*

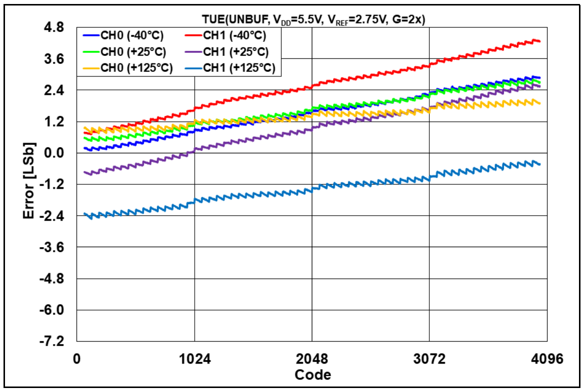


FIGURE 2-23: *TUE (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 5.5V, V_{REF} = 2.75V, G = 2x.*

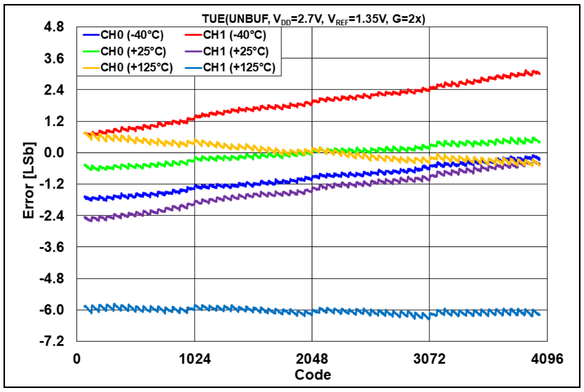


FIGURE 2-24: *TUE (V_{OUT}) vs. DAC Code and Temperature, V_{DD} = 2.7V, V_{REF} = 1.35V, G = 2x.*

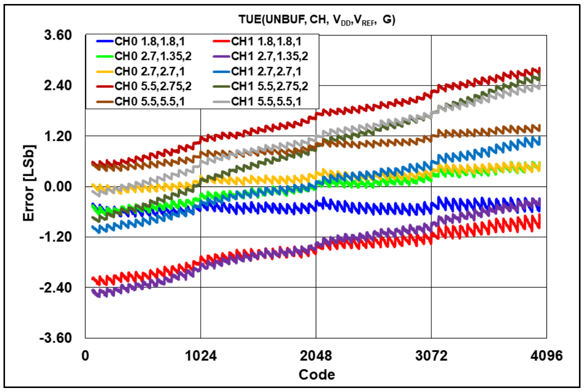


FIGURE 2-25: *TUE (V_{OUT}) vs. DAC Code, Temperature = +25°C.*

2.2.4 TOTAL UNADJUSTED ERROR (TUE) – EXTERNAL BUFFERED V_{REF} MODE (VRXB:VRXA = `11`), MCP48CXD22 (12-BIT), CODE 64-4032

Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = 5.5V.

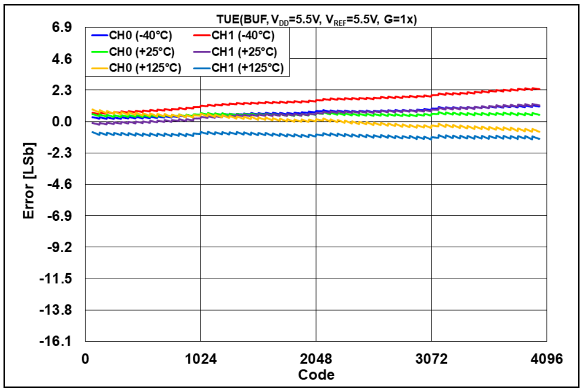


FIGURE 2-26: *TUE (V_{OUT}) vs. DAC Code and Temperature, V_{REF} = V_{DD} = 5.5V, G = 1x.*

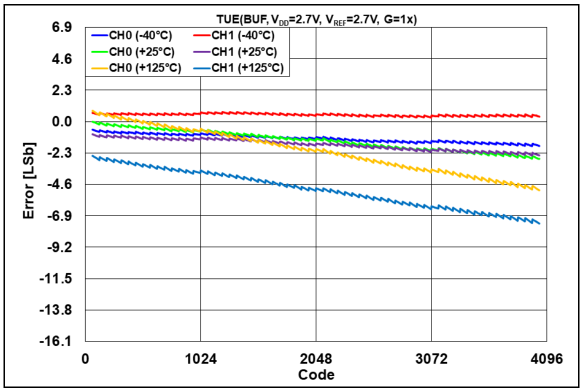


FIGURE 2-27: *TUE (V_{OUT}) vs. DAC Code and Temperature, V_{REF} = V_{DD} = 2.7V, G = 1x.*

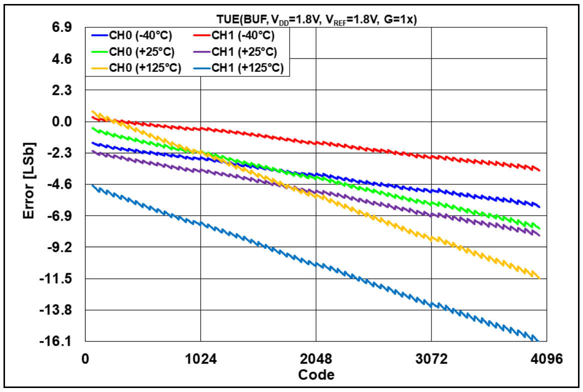


FIGURE 2-28: *TUE (V_{OUT}) vs. DAC Code and Temperature, V_{REF} = V_{DD} = 2.7V, G = 1x.*

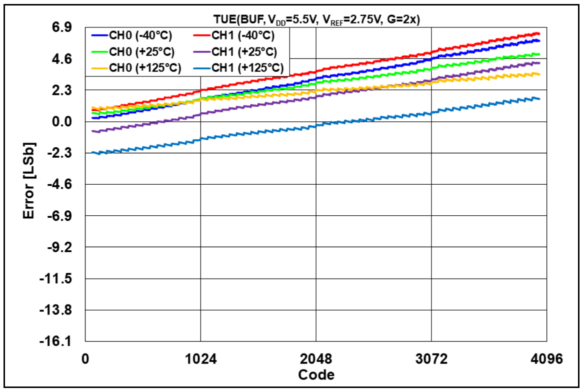


FIGURE 2-29: *TUE (V_{OUT}) vs. DAC Code and Temperature, V_{REF} = 2.75V, V_{DD} = 5.5V, G = 2x.*

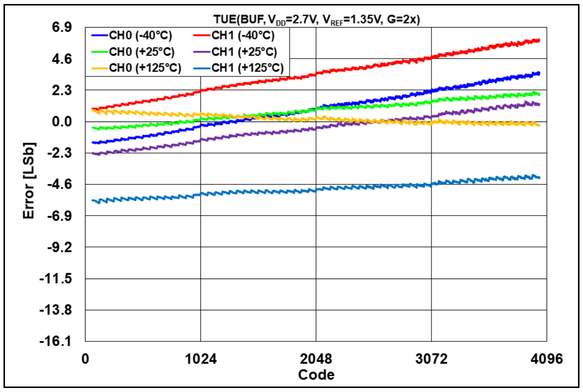


FIGURE 2-30: *TUE (V_{OUT}) vs. DAC Code and Temperature, V_{REF} = 1.35V, V_{DD} = 2.7V, G = 2x.*

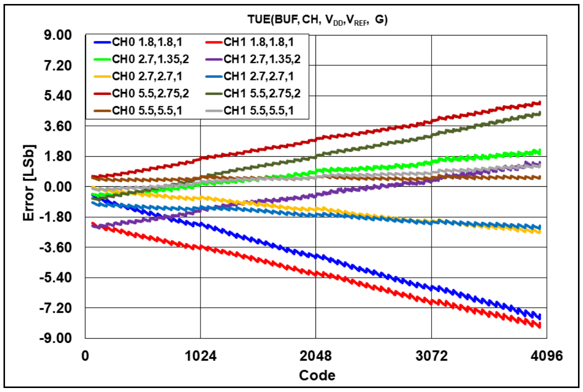


FIGURE 2-31: *TUE (V_{OUT}) vs. DAC Code, Temperature = +25°C.*

2.2.5 INTEGRAL NONLINEARITY (INL) – V_{DD} MODE (VRXB:VRXA = `00`) MCP48CXD22 (12-BIT), CODE 64-4032

Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = 5.5V.

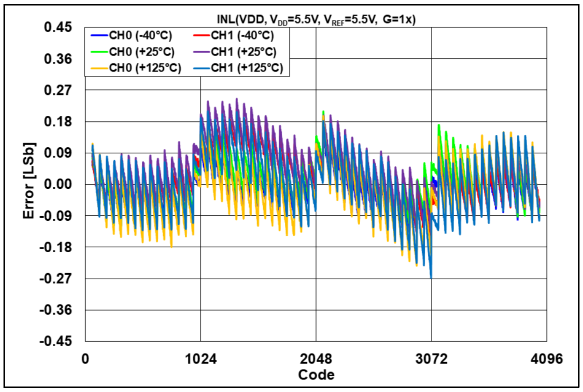


FIGURE 2-32: *INL Error vs. DAC Code and Temperature,* $V_{REF} = V_{DD}$ *= 5.5V,* G = 1x.

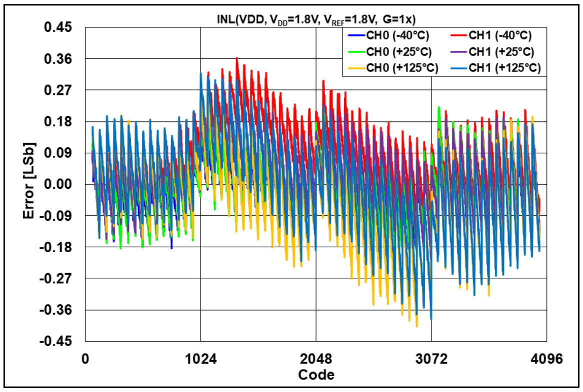


FIGURE 2-34: *INL Error vs. DAC Code and Temperature,* $V_{REF} = V_{DD}$ *= 1.8V,* G = 1x.

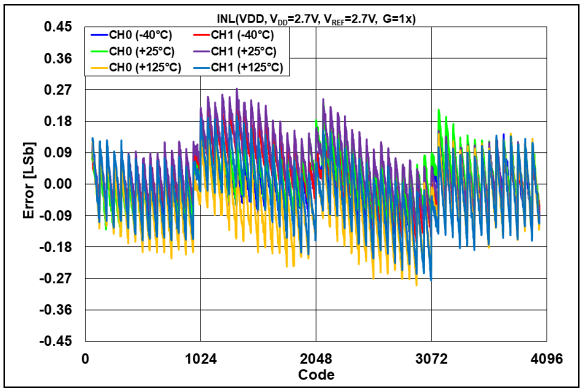


FIGURE 2-33: *INL Error vs. DAC Code and Temperature,* $V_{REF} = V_{DD}$ *= 2.7V,* G = 1x.

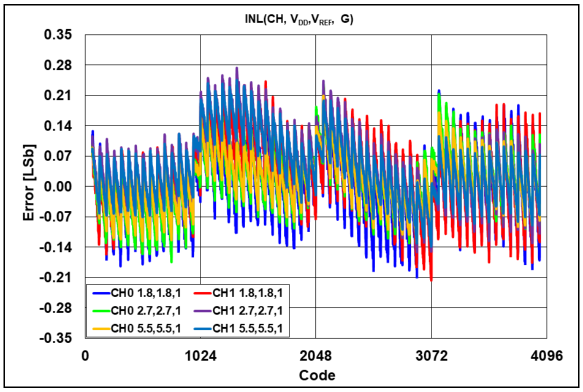


FIGURE 2-35: *INL Error vs. DAC Code, Temperature = +25°C.*

2.2.6 INTEGRAL NONLINEARITY (INL) – INTERNAL BAND GAP MODE (VRXB:VRXA = `01`), MCP48CXD22 (12-BIT), CODE 64-4032

Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = 5.5V.

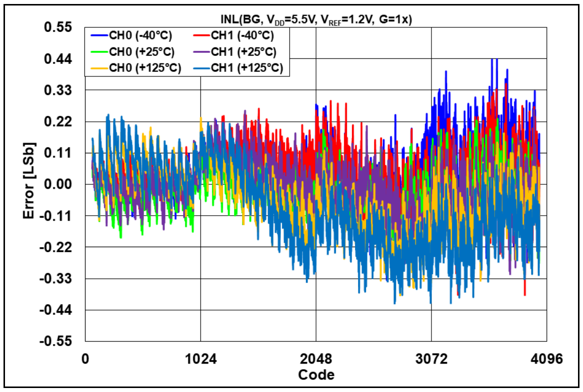


FIGURE 2-36: *INL Error vs. DAC Code and Temperature,* V_{DD} = 5.5V, V_{REF} = 1.2V, G = 1x.

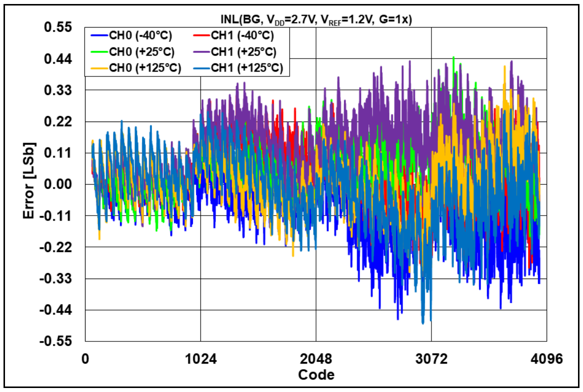


FIGURE 2-37: *INL Error vs. DAC Code and Temperature,* V_{DD} = 2.7V, V_{REF} = 1.2V, G = 1x.

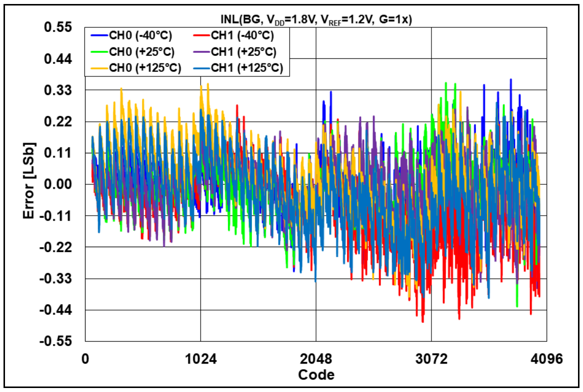


FIGURE 2-38: *INL Error vs. DAC Code and Temperature,* V_{DD} = 1.8V, V_{REF} = 1.2V, G = 1x.

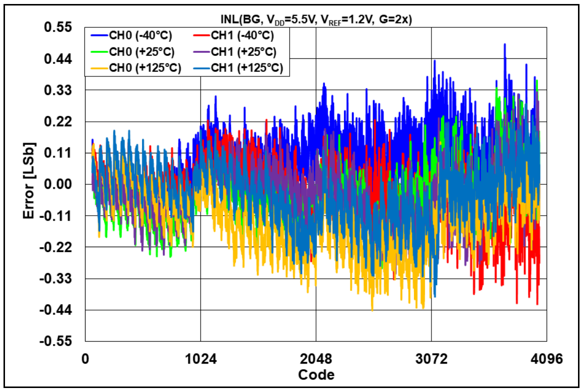


FIGURE 2-39: *INL Error vs. DAC Code and Temperature,* V_{DD} = 5.5V, V_{REF} = 1.2V, G = 2x.

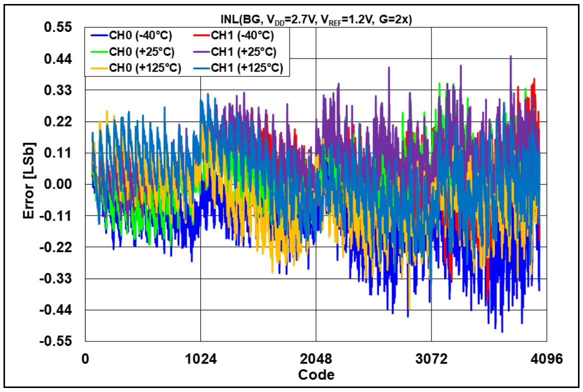


FIGURE 2-40: *INL Error vs. DAC Code and Temperature,* V_{DD} = 2.7V, V_{REF} = 1.2V, G = 2x.

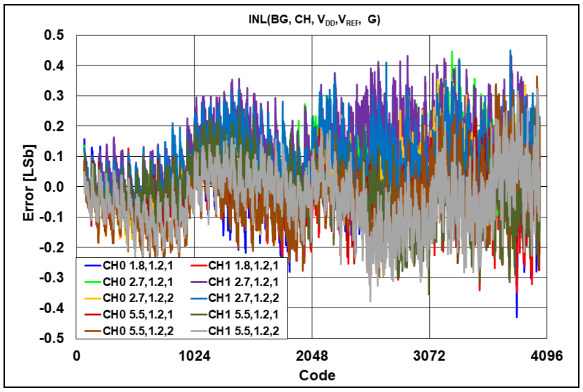


FIGURE 2-41: *INL Error vs. DAC Code, Temperature = +25°C.*

2.2.7 INTEGRAL NONLINEARITY (INL) – EXTERNAL UNBUFFERED V_{REF} MODE (VRXB:VRXA = `10`), MCP48CXD22 (12-BIT), CODE 64-4032

Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = 5.5V.

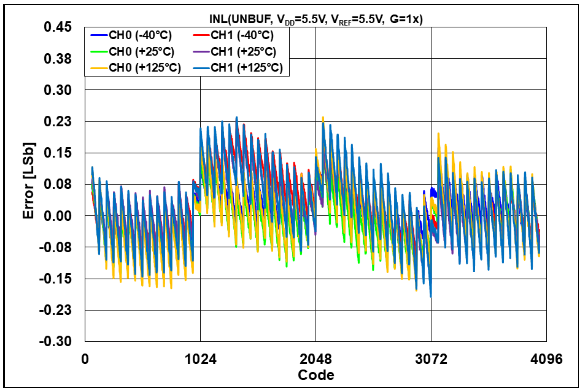


FIGURE 2-42: *INL Error vs. DAC Code and Temperature, V_{DD} = V_{REF} = 5.5V, G = 1x.*

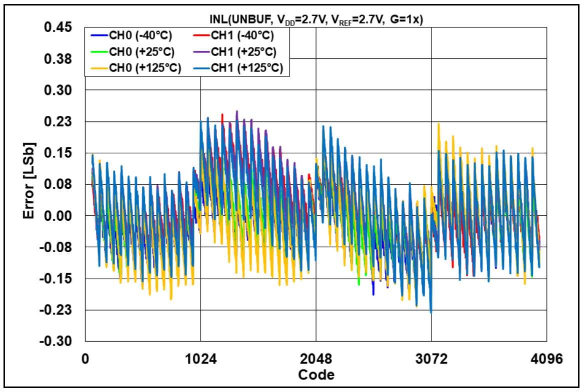


FIGURE 2-43: *INL Error vs. DAC Code and Temperature, V_{DD} = V_{REF} = 2.7V, G = 1x.*

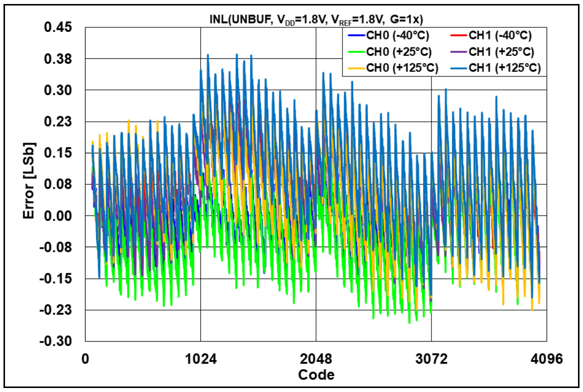


FIGURE 2-44: *INL Error vs. DAC Code and Temperature, V_{DD} = V_{REF} = 1.8V, G = 1x.*

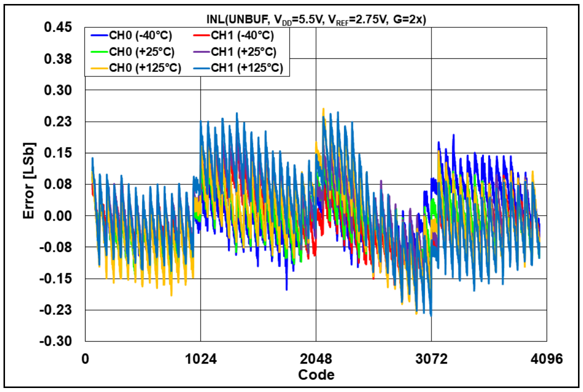


FIGURE 2-45: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, V_{REF} = 2.75V, G = 2x.*

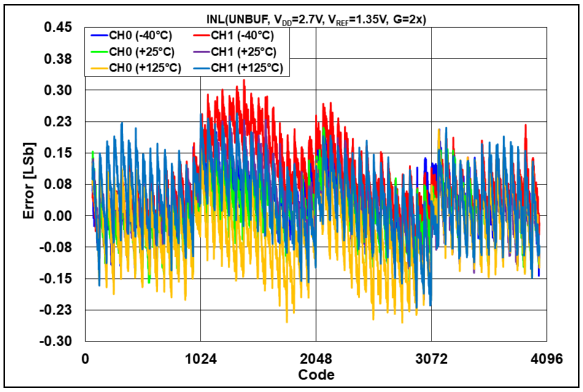


FIGURE 2-46: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, V_{REF} = 1.35V, G = 2x.*

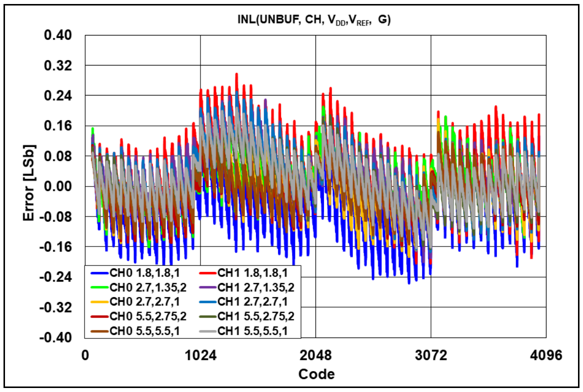


FIGURE 2-47: *INL Error vs. DAC Code, Temperature = +25°C.*

2.2.8 INTEGRAL NONLINEARITY (INL) – EXTERNAL BUFFERED V_{REF} MODE (VRXB:VRXA = `11`), MCP48CXD22 (12-BIT), CODE 64-4032

Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = 5.5V.

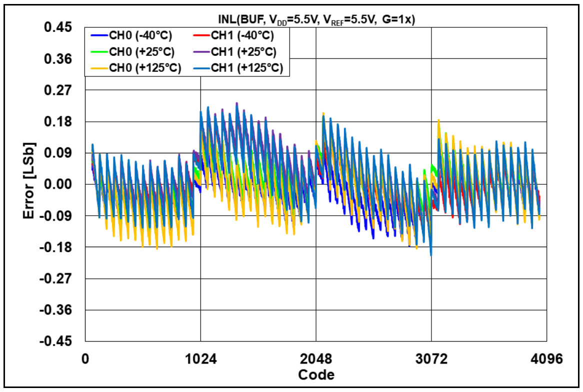


FIGURE 2-48: *INL Error vs. DAC Code and Temperature, V_{DD} = V_{REF} = 5.5V, G = 1x.*

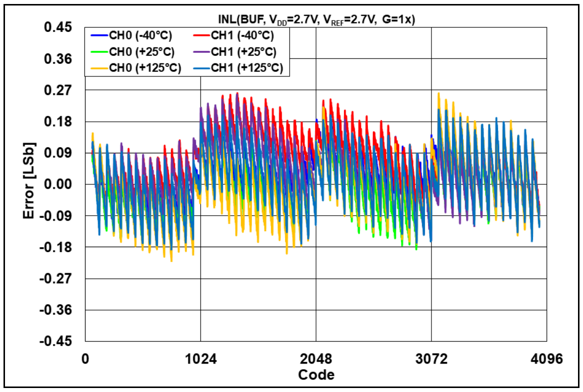


FIGURE 2-49: *INL Error vs. DAC Code and Temperature, V_{DD} = V_{REF} = 2.7V, G = 1x.*

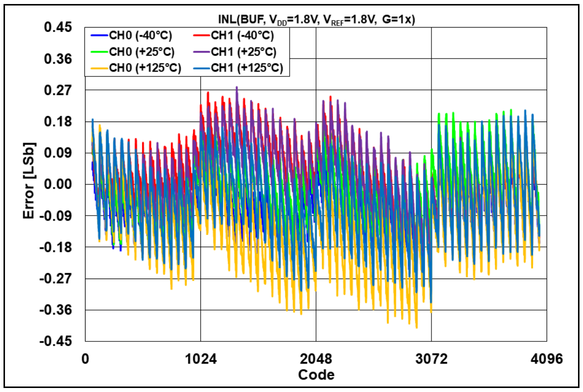


FIGURE 2-50: *INL Error vs. DAC Code and Temperature, V_{DD} = V_{REF} = 1.8V, G = 1x.*

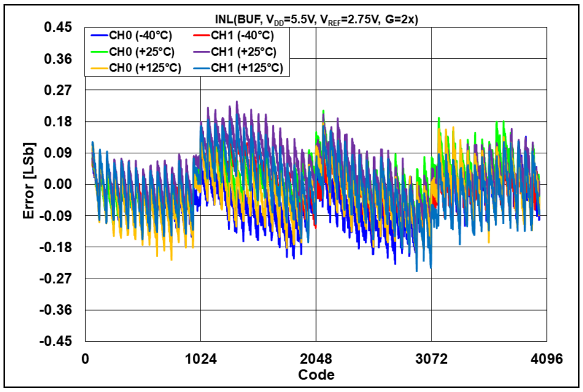


FIGURE 2-51: *INL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, V_{REF} = 2.75V, G = 2x.*

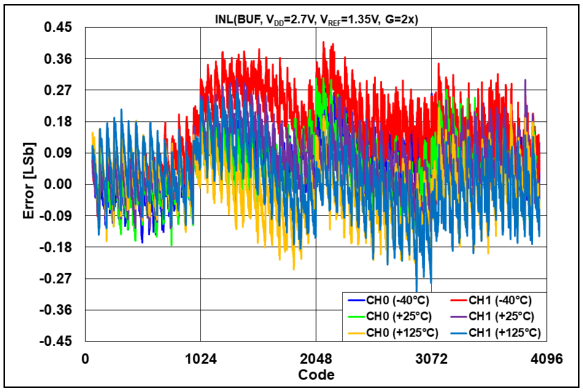


FIGURE 2-52: *INL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, V_{REF} = 1.35V, G = 2x.*

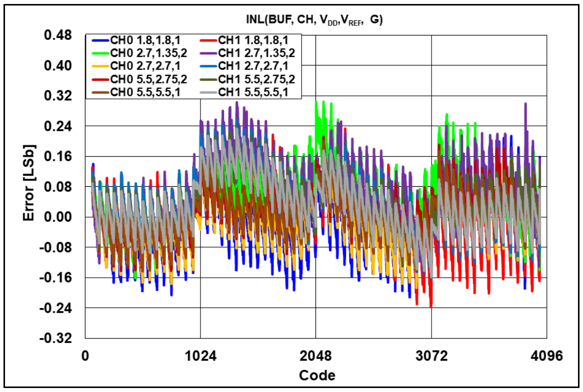


FIGURE 2-53: *INL Error vs. DAC Code, Temperature = +25°C.*

2.2.9 DIFFERENTIAL NONLINEARITY (DNL) – V_{DD} MODE (VRXB:VRXA = `00`) MCP48CXD22 (12-BIT), CODE 64-4032

Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = 5.5V.

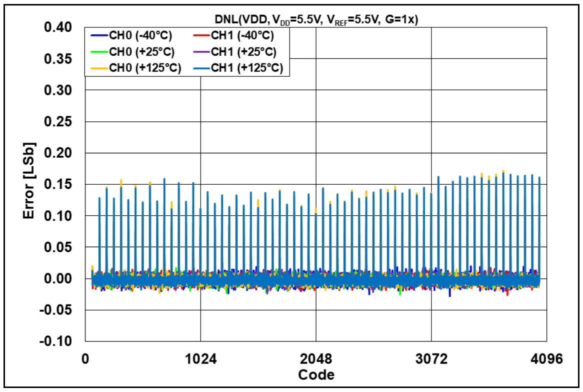


FIGURE 2-54: *DNL Error vs. DAC Code and Temperature,* V_{REF} = V_{DD} = 5.5V, G = 1x.

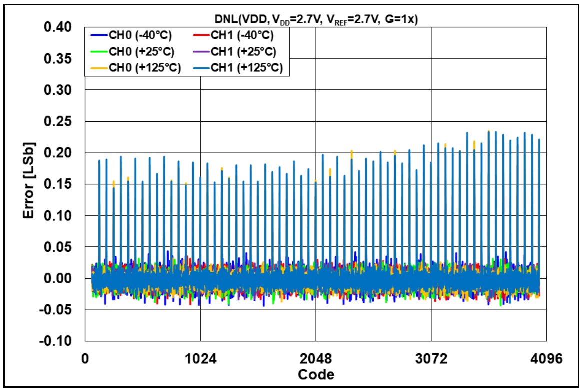


FIGURE 2-55: *DNL Error vs. DAC Code and Temperature,* V_{REF} = V_{DD} = 2.7V, G = 1x.

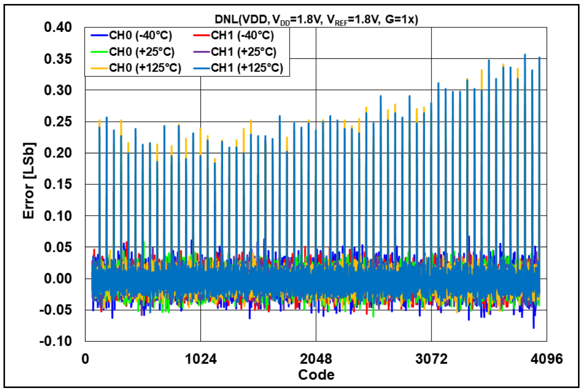


FIGURE 2-56: *DNL Error vs. DAC Code and Temperature,* V_{REF} = V_{DD} = 1.8V, G = 1x.

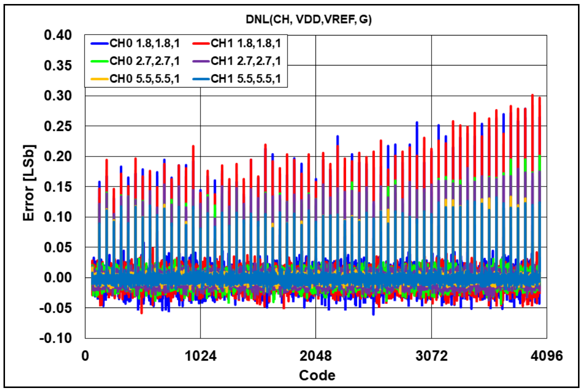


FIGURE 2-57: *DNL Error vs. DAC Code, Temperature = +25°C.*

2.2.10 DIFFERENTIAL NONLINEARITY (DNL) – INTERNAL BAND GAP MODE (VRXB:VRXA = `01`), MCP48CXD22 (12-BIT), CODE 64-4032

Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = 5.5V.

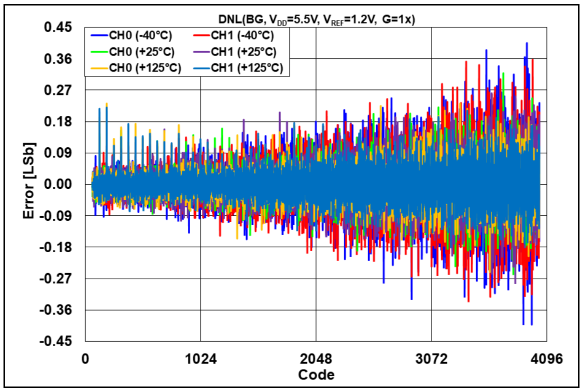


FIGURE 2-58: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, V_{REF} = 1.2V,* G = 1x.

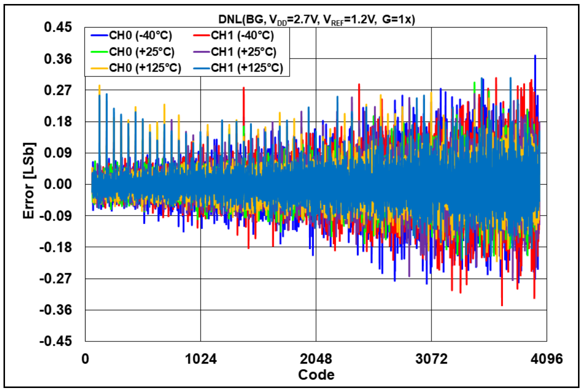


FIGURE 2-59: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, V_{REF} = 1.2V,* G = 1x.

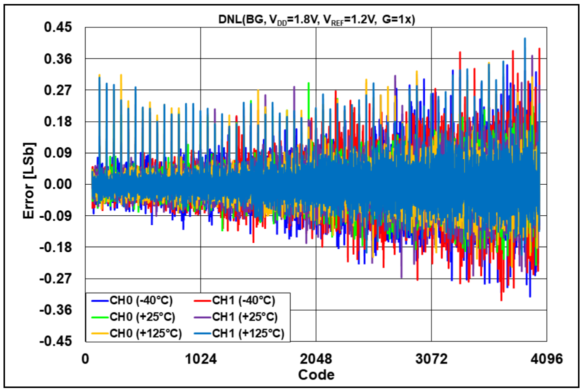


FIGURE 2-60: *DNL Error vs. DAC Code and Temperature, V_{DD} = 1.8V, V_{REF} = 1.2V,* G = 1x.

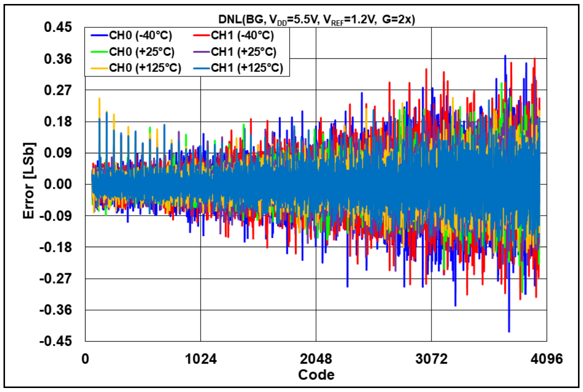


FIGURE 2-61: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, V_{REF} = 1.2V,* G = 2x.

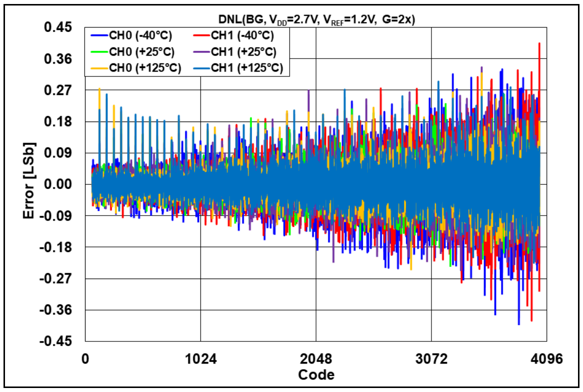


FIGURE 2-62: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, V_{REF} = 1.2V,* G = 2x.

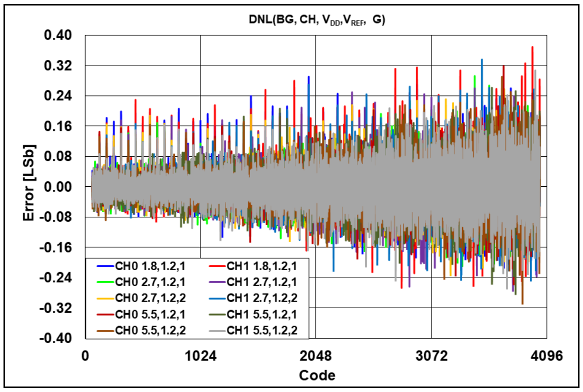


FIGURE 2-63: *DNL Error vs. DAC Code, Temperature = +25°C.*

2.2.11 DIFFERENTIAL NONLINEARITY (DNL) – EXTERNAL UNBUFFERED V_{REF} MODE (VRXB:VRXA = `10`), MCP48CXD22 (12-BIT), CODE 64-4032

Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = 5.5V.

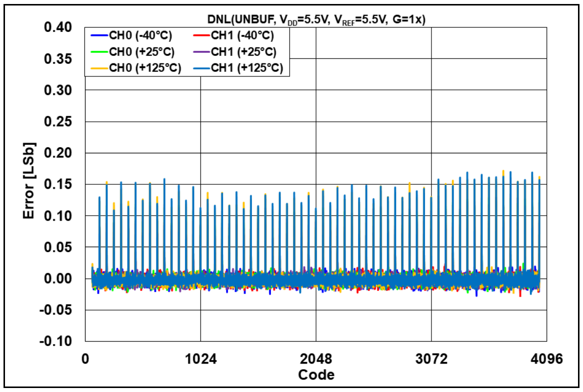


FIGURE 2-64: *DNL Error vs. DAC Code and Temperature, V_{DD} = V_{REF} = 5.5V, G = 1x.*

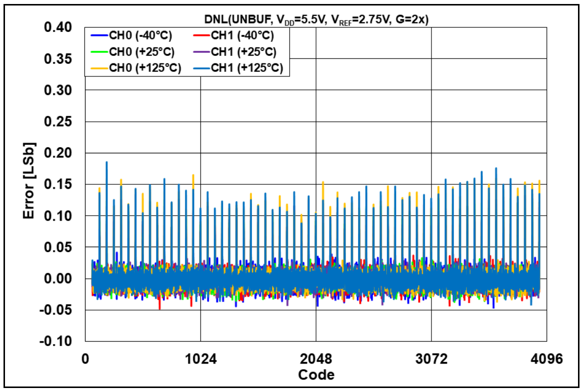


FIGURE 2-67: *DNL Error vs. DAC Code and Temperature, V_{DD} = 5.5V, V_{REF} = 2.75V, G = 2x.*

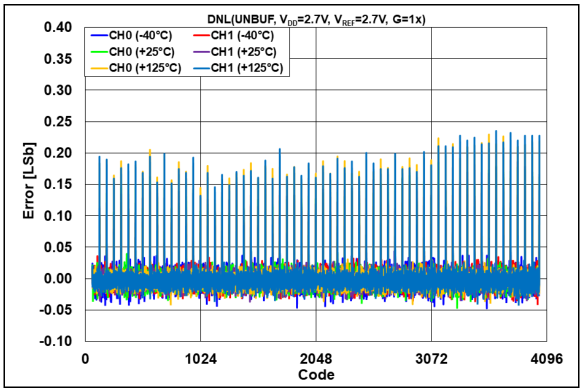


FIGURE 2-65: *DNL Error vs. DAC Code and Temperature, V_{DD} = V_{REF} = 2.7V, G = 1x.*

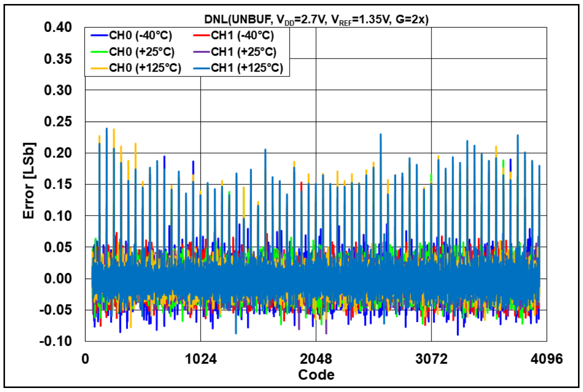


FIGURE 2-68: *DNL Error vs. DAC Code and Temperature, V_{DD} = 2.7V, V_{REF} = 1.35V, G = 2x.*

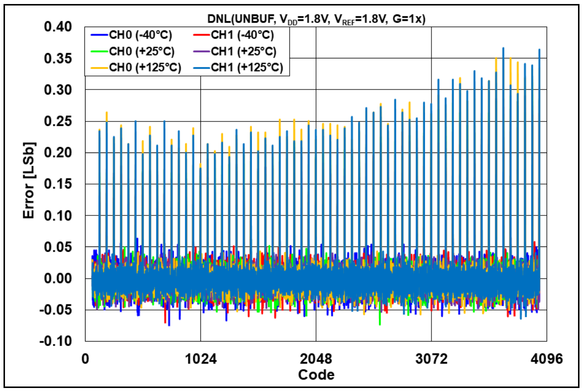


FIGURE 2-66: *DNL Error vs. DAC Code and Temperature, V_{DD} = V_{REF} = 2.7V, G = 1x.*

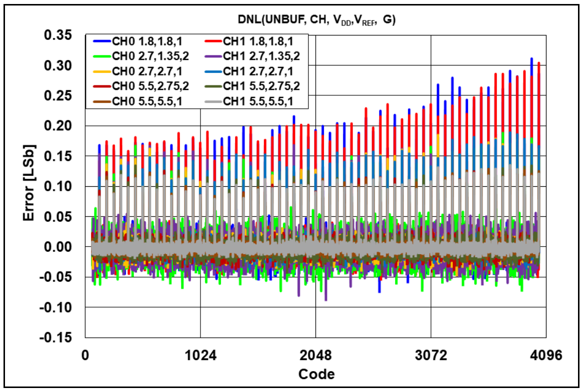


FIGURE 2-69: *DNL Error vs. DAC Code, Temperature = +25°C.*

2.2.12 DIFFERENTIAL NONLINEARITY (DNL) – EXTERNAL BUFFERED V_{REF} MODE (VRXB:VRXA = `11`), MCP48CXD22 (12-BIT), CODE 64-4032

Note: Unless otherwise indicated: T_A = +25°C, V_{DD} = 5.5V.

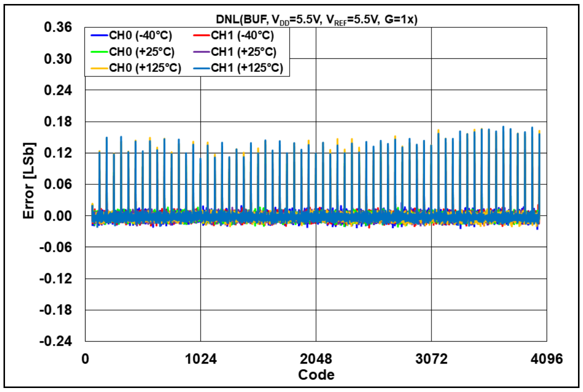


FIGURE 2-70: *DNL Error vs. DAC Code and Temperature,* V_{DD} = V_{REF} = 5.5V, G = 1x.

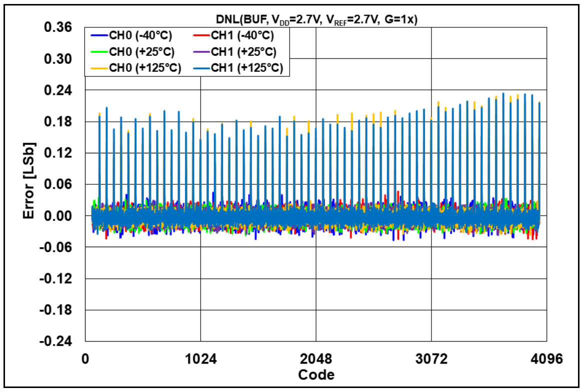


FIGURE 2-71: *DNL Error vs. DAC Code and Temperature,* V_{DD} = V_{REF} = 2.7V, G = 1x.

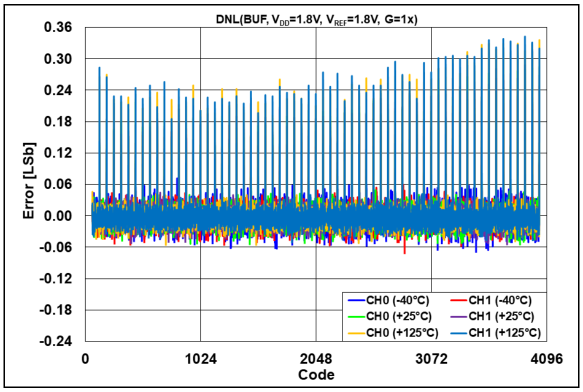


FIGURE 2-72: *DNL Error vs. DAC Code and Temperature,* V_{REF} = V_{DD} = 1.8V, G = 1x.

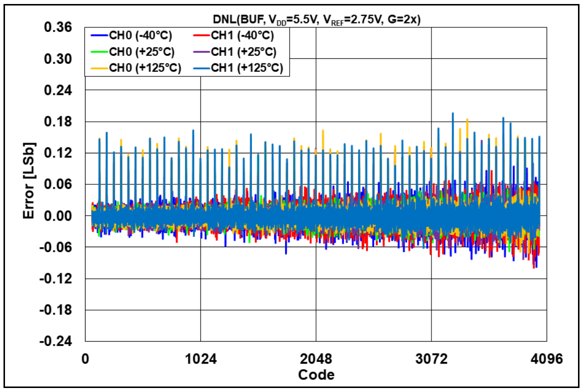


FIGURE 2-73: *DNL Error vs. DAC Code and Temperature,* V_{DD} = 5.5V, V_{REF} = 2.75V, G = 1x.

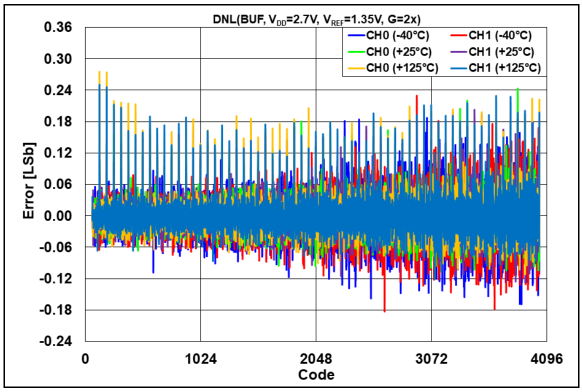


FIGURE 2-74: *DNL Error vs. DAC Code and Temperature,* V_{DD} = 2.7V, V_{REF} = 1.35V, G = 2x.

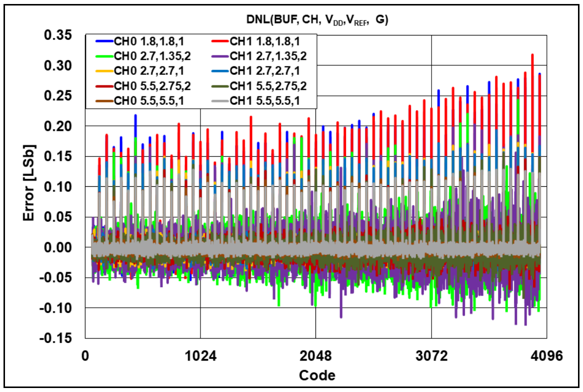


FIGURE 2-75: *DNL Error vs. DAC Code, Temperature = +25°C.*

3.0 PIN DESCRIPTIONS

Overviews of the pin functions are provided from **Section 3.1 "Positive Power Supply Input (V_{DD})"** to **Section 3.10 "SPI – Serial Data Out Pin (SDO)"**.

The descriptions of the pins for the single DAC output device are listed in Table 3-1, and descriptions for the dual DAC output device are listed in Table 3-2.

TABLE 3-1: MCP48CXDX1 (SINGLE DAC) PIN FUNCTION TABLE

Pin			Symbol	I/O	Buffer Type	Description
MSOP 10L	DFN 10L	QFN 16L				
1	1	16	V_{DD}	—	P	Supply Voltage
2	2	1	$\overline{CS}$	I	ST	SPI Chip Select
3	3	2	V_{REF}	A	Analog	Voltage Reference Input/Output
4	4	3	V_{OUT}	A	Analog	Buffered Analog Voltage Output
5	5	4,5,6,7, 8,14,15	NC	—	—	Not Internally Connected
6	6	9	$\overline{LAT}$/HVC	I	ST	DAC Wiper Register Latch/High-Voltage Command Pin. The Latch Pin allows the value in the volatile DAC registers (wiper and configuration bits) to be transferred to the DAC output (V_{OUT}). High-Voltage commands allow the User MTP configuration bits to be written.
7	7	10	V_{SS}	—	P	Ground Reference for all circuitries on the device
8	8	11	SDO	O	ST	SPI Serial Data Output
9	9	12	SCK	I	ST	SPI Serial Clock
10	10	13	SDI	I	ST	SPI Serial Data Input
—	—	17	EP	—	P	Exposed Thermal Pad, must be connected to V_{SS}

Note 1: A = Analog, I = Input, ST = Schmitt Trigger, O = Output, I/O = Input/Output, P = Power

TABLE 3-2: MCP48CXDX2 (DUAL DAC) PIN FUNCTION TABLE

Pin			Symbol	I/O	Buffer Type	Description
MSOP 10L	**DFN 10L**	**QFN 16L**				
1	1	16	V_{DD}	—	P	Supply Voltage
2	2	1	$\overline{CS}$	I	ST	SPI Chip Select
3	3	—	V_{REF}	A	Analog	Voltage Reference Input/Output
—	—	2	V_{REF0}	A	Analog	Voltage Reference Input/Output for DAC0
—	—	4	V_{REF1}	A	Analog	Voltage Reference Input/Output for DAC1
4	4	3	V_{OUT0}	A	Analog	Buffered Analog Voltage Output 0
5	5	5	V_{OUT1}	A	Analog	Buffered Analog Voltage Output 1
—	—	6,7,14, 15	NC	—	—	Not Internally Connected
6	6	—	$\overline{LAT}$/HVC	I	ST	DAC Wiper Register Latch/High-Voltage Command Pin. The Latch Pin allows the value in the volatile DAC registers (wiper and configuration bits) to be transferred to the DAC output (V_{OUT}). High-Voltage commands allow the User MTP configuration bits to be written.
—	—	9	$\overline{LAT0}$/HVC	I	ST	DAC0 Wiper Register Latch/High-Voltage Command Pin. The Latch Pin allows the value in the volatile DAC0 registers (wiper and configuration bits) to be transferred to the DAC0 output (V_{OUT0}). High-Voltage commands allow the User MTP configuration bits to be written.
—	—	8	$\overline{LAT1}$	I	ST	DAC1 Wiper Register Latch. The Latch Pin allows the value in the volatile DAC1 registers (wiper and configuration bits) to be transferred to the DAC1 output (V_{OUT1}).
7	7	10	V_{SS}	—	P	Ground Reference for all circuitries on the device
8	8	11	SDO	O	ST	SPI Serial Data Output
9	9	12	SCK	I	ST	SPI Serial Clock
10	10	13	SDI	I	ST	SPI Serial Data Input
—	—	17	EP	—	P	Exposed Thermal Pad, must be connected to V_{SS}

Note 1: A = Analog, I = Input, ST = Schmitt Trigger, O = Output, I/O = Input/Output, P = Power

3.1 Positive Power Supply Input (V_{DD})

V_{DD} is the positive supply voltage input pin. The input supply voltage is relative to V_{SS}.

The power supply at the V_{DD} pin must be as clean as possible for good DAC performance. It is recommended to use an appropriate bypass capacitor of about 0.1 µF (ceramic) to ground as close as possible to the pin. An additional 10 µF capacitor (tantalum) in parallel is also recommended to further attenuate noise present in application boards.

3.2 Ground (V_{SS})

The V_{SS} pin is the device ground reference.

The user must connect the V_{SS} pin to a ground plane through a low-impedance connection. If an analog ground path is available in the application PCB (Printed Circuit Board), it is highly recommended that the V_{SS} pin be tied to the analog ground path or isolated within an analog ground plane of the circuit board.

3.3 Voltage Reference Pin (V_{REF})

The V_{REF} pin is either an input or an output. When the DAC's voltage reference is configured as the V_{REF} pin, the pin is an input. When the DAC's voltage reference is configured as the internal band gap, the pin is an output.

When the DAC's voltage reference is configured as the V_{REF} pin, there are two options for this voltage input: the V_{REF} pin voltage is buffered or unbuffered. The buffered option is offered in cases where the external reference voltage does not have sufficient current capability to not drop its voltage when connected to the internal resistor ladder circuit.

When the DAC's voltage reference is configured as the device V_{DD}, the V_{REF} pin is disconnected from the internal circuit.

When the DAC's voltage reference is configured as the internal band gap, the V_{REF} pin's drive capability is minimal, so the output signal must be buffered.

See **Section 5.2 "Voltage Reference Selection"** and Register 4-2 for more details on the configuration bits.

3.4 No Connect (NC)

The NC pin is not internally connected to the device.

3.5 Analog Output Voltage Pins (V_{OUT0}, V_{OUT1})

V_{OUT0} and V_{OUT1} are the DAC analog voltage output pins. Each DAC output has an output amplifier. The DAC output range depends on the selection of the voltage reference source (and potential output gain selection). These are:

- Device V_{DD} – The full-scale range of the DAC output is from V_{SS} to approximately V_{DD}.
- V_{REF} pin – The full-scale range of the DAC output is from V_{SS} to G x V_{RL}, where G is the gain selection option (1X or 2X).
- Internal band gap – The full-scale range of the DAC output is from V_{SS} to G x V_{BG}, where G is the gain selection option (1X or 2X).

In Normal mode, the DC impedance of the output pin is about 1Ω. In Power-Down mode, the output pin is internally connected to a known pull-down resistor of 1 kΩ, 100 kΩ or open. The Power-Down selection bits settings are shown in Register 4-3 (Table 5-5).

3.6 $\overline{\text{Latch}}$/High-Voltage Command Pin ($\overline{\text{LAT}}$/HVC)

The DAC output value update event can be controlled and synchronized using the $\overline{\text{LAT}}$ pin, for one or both channels, on a single or different devices.

The $\overline{\text{LAT}}$ pin controls the effect of the volatile wiper registers, VRxB:VRxA, PDxB:PDxA and Gx bits on the DAC output.

If the $\overline{\text{LAT}}$ pin is held at V_{IH}, the values sent to the volatile wiper registers and configuration bits have no effect on the DAC outputs.

Once voltage on the pin transitions to V_{IL}, the values in the volatile wiper registers and configuration bits are transferred to the DAC outputs.

The pin is level-sensitive, so writing to the volatile wiper registers and configuration bits, while it is being held at V_{IL}, will trigger an immediate change in the outputs.

For dual output devices in MSOP and DFN packages, the $\overline{\text{LAT}}$ pin controls both channels at the same time.

The HVC pin allows the device's MTP memory to be programmed for the MCP48CXDX1/2 devices. The programming voltage supply must provide 7.5V and at least 6.4 mA.

Note: The HVC pin must have voltages greater than 5.5V present only during the MTP programming operation. Using voltages greater than 5.5V for an extended time on the pin may cause device reliability issues.

3.7 SPI – Chip Select Pin ($\overline{\text{CS}}$)

The $\overline{\text{CS}}$ pin enables/disables the serial interface (SDI, SDO and SCK). The serial interface must be enabled for the device to receive any serial commands.

See **Section 6.4 "Interface Pins (CS, SCK, SDI, SDO and LAT/HVC)"** for more details regarding the SPI serial interface communication.

3.8 SPI – Serial Clock Pin (SCK)

The SCK pin is the serial clock pin of the SPI interface. The MCP48CXDX1/2 SPI interface only accepts external serial clocks.

3.9 SPI – Serial Data In Pin (SDI)

The SDI pin is the serial data input pin of the SPI interface. The SDI pin is used to write the DAC wiper registers and configuration bits.

3.10 SPI – Serial Data Out Pin (SDO)

The SDO pin is the serial data output pin of the SPI interface. The SDO pin is used to read the DAC wiper registers and configuration bits.

4.0 GENERAL DESCRIPTION

The MCP48CXDX1 devices are single channel voltage output devices.

The MCP48CXDX2 devices are dual channel voltage output devices.

These devices are offered with 8-bit (MCP48CXD0X), 10-bit (MCP48CXD1X) and 12-bit (MCP48CXD2X) resolutions.

The family offers two memory options: the MCP48CVDXX devices have a volatile memory, while the MCP48CMDXX have a 32-times programmable nonvolatile memory (MTP).

All devices include an SPI serial interface and a write latch ($\overline{\text{LAT}}$) pin to control the update of the analog output voltage value from the value written in the volatile DAC output register.

The devices use a resistor ladder architecture. The resistor ladder DAC is driven from a software-selectable voltage reference source. The source can be either the device's internal V_{DD}, an external V_{REF} pin voltage (buffered or unbuffered) or an internal band gap voltage source.

The DAC output is buffered with a low power and precision output amplifier. This output amplifier provides a rail-to-rail output with low offset voltage and low noise. The gain (1X or 2X) of the output buffer is software configurable.

The devices operate from a single supply voltage. This voltage is specified from 2.7V to 5.5V for full specified operation, and from 1.8V to 5.5V for digital operation. The device operates between 1.8V and 2.7V, but some device parameters are not specified.

The MCP48CXDX1/2 devices also have user-programmable nonvolatile configuration memory (MTP). This allows the device's desired POR values to be saved. The device also has general purpose MTP memory locations for storing system-specific information (calibration data, serial numbers, system ID information). A high-voltage requirement for programming the nonvolatile locations on the HVC pin ensures that these device settings are not accidentally modified during normal system operation. Therefore, it is recommended that the MTP memory be only programmed at the user's factory.

The main functional blocks are:

- **Power-on Reset/Brown-out Reset (POR/BOR)**
- **Device Memory**
- **Resistor Ladder**
- **Output Buffer/V_{OUT} Operation**
- **SPI Serial Interface Module**

4.1 Power-on Reset/Brown-out Reset (POR/BOR)

The internal POR/BOR circuit monitors the power supply voltage (V_{DD}) during operation. This circuit ensures correct device start-up at system power-up and power-down events.

The device's RAM retention voltage (V_{RAM}) is lower than the POR/BOR voltage trip point (V_{POR}/V_{BOR}). The maximum V_{POR}/V_{BOR} voltage is less than 1.8V.

The POR and BOR trip points are at the same voltage, and the condition is determined by whether the V_{DD} voltage is rising or falling (see Figure 4-1). What occurs is different depending on whether the reset is a POR or BOR.

POR occurs as the voltage rises (typically from 0V), while BOR occurs as the voltage falls (typically from $V_{DD(MIN)}$ or higher).

When $V_{POR}/V_{BOR} < V_{DD} < 2.7V$, the electrical performance may not meet the data sheet specifications. In this region, the device is capable of reading and writing to its volatile memory if the proper serial command is executed.

4.1.1 POWER-ON RESET

The POR is the case where the device's V_{DD} has power applied to it from the V_{SS} voltage level. As the device powers-up, the V_{OUT} pin floats to an unknown value. When the device's V_{DD} is above the transistor threshold voltage of the device, the output starts to be pulled low.

After the V_{DD} is above the POR/BOR trip point (V_{BOR}/V_{POR}), the resistor network's wiper is loaded with the POR value. The POR value is either mid-scale (MCP48CVDXX) or the user's MTP programmed value (MCP48CMDXX).

Note: In order to have the MCP48CMDXX devices load the values from nonvolatile memory locations at POR, they have to be programmed at least once by the user; otherwise, the loaded values will be the default ones. After MTP programming, a POR event is required to load the written values from the nonvolatile memory.

Volatile memory determines the analog output (V_{OUT}) pin voltage. After the device is powered-up, the user can update the device memory.

When the rising V_{DD} voltage crosses the V_{POR} trip point, the following occurs:

- The default DAC POR value is latched into the volatile DAC register.
- The default DAC POR Configuration bit values are latched into the volatile configuration bits.
- POR Status bit is set (`1`).
- The reset delay timer (t_{PORD}) starts; when the reset delay timer times out, the SPI serial interface is operational. During this delay time, the SPI interface will not accept commands.
- The device memory address pointer is forced to 00h.

The analog output (V_{OUT}) state is determined by the state of the volatile configuration bits and the DAC register. This is called a Power-on Reset (event).

Figure 4-1 illustrates the conditions for power-up and power-down events under typical conditions.

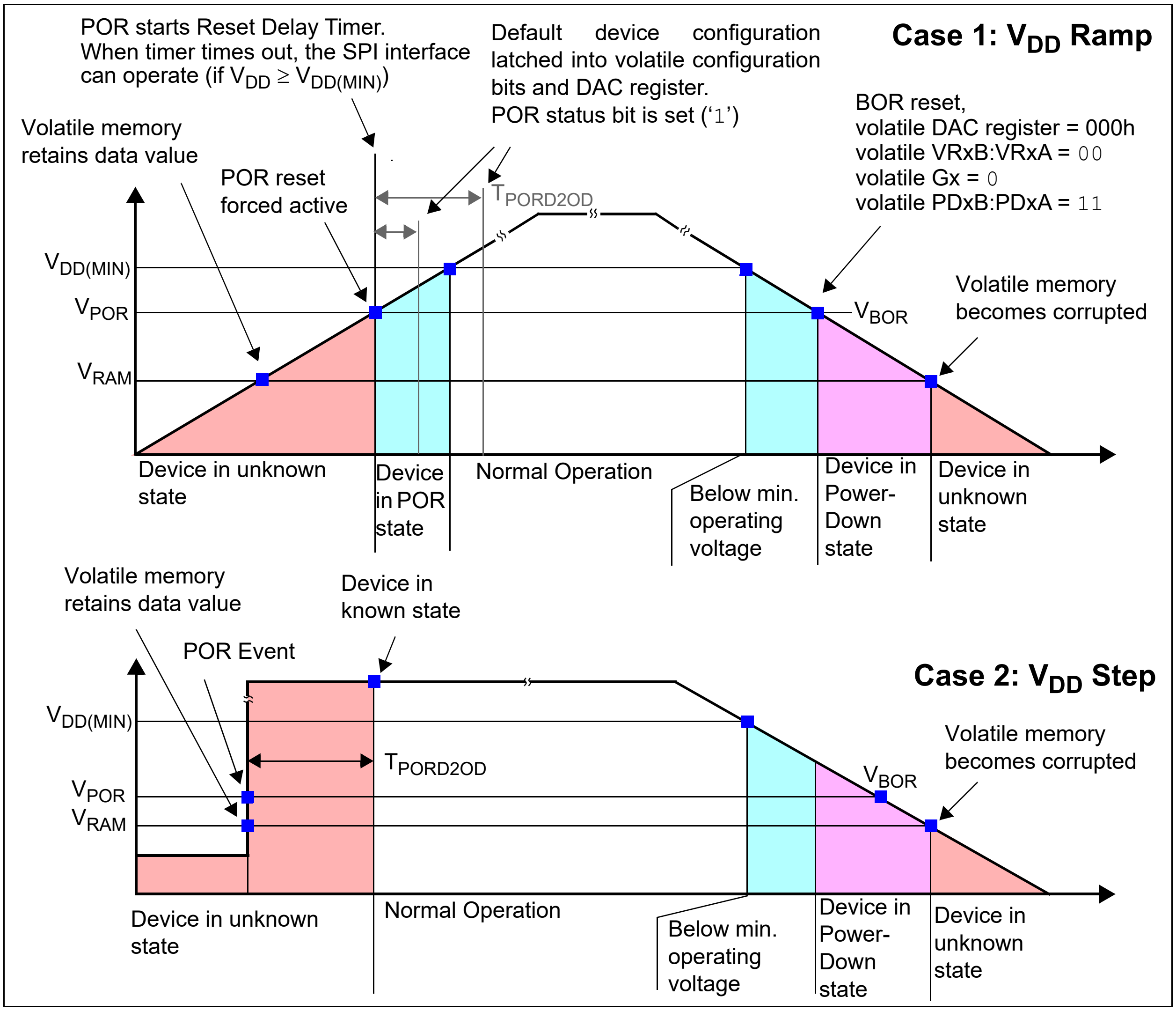


FIGURE 4-1: *Power-on Reset Operation.*

4.1.2 BROWN-OUT RESET

A BOR occurs when a device has power applied to it and that power (voltage) drops below the specified range.

When the falling V_{DD} voltage crosses the V_{POR} trip point (BOR event), the following occurs:

- Serial interface is disabled.
- MTP writes are disabled.
- Device is forced into a Power-Down state (PDxB:PDxA = `11`). Analog circuitry is turned off.
- Volatile DAC register is forced to 000h.

Volatile configuration bits VRxB:VRxA and GX are forced to ‘`0`’.

If the V_{DD} voltage decreases below the V_{RAM} voltage, all volatile memory may become corrupted.

As the voltage recovers above the V_{POR}/V_{BOR} voltage, see **Section 4.1.1 “Power-on Reset”** for further details.

Serial commands not completed due to a brown-out condition may cause the memory location to become corrupted.

Figure 4-1 illustrates the conditions for power-up and power-down events under typical conditions.

4.2 Device Memory

User memory includes the following types:

- **Volatile Register Memory (RAM)**
- **Nonvolatile Register Memory (MTP)**

MTP memory is present just for the MCP48CMDXX devices and has three groupings:

- NV DAC Output Values (loaded on POR event)
- Device Configuration Memory
- General Purpose NV Memory

Each memory location is up to 16 bits wide. The memory mapped register space is shown in Table 4-1.

The SPI interface depends on how this memory is read and written. Refer to **Section 6.0 “SPI Serial Interface Module”** and **Section 7.0 “Device Commands”** for more details on reading and writing the device’s memory.

4.2.1 VOLATILE REGISTER MEMORY (RAM)

The MCP48CXDX1/2 devices have volatile memory to directly control the operation of the DACs. There are up to five volatile memory locations:

- DAC0 and DAC1 Output Value registers
- V_{REF} Select register
- Power-Down Configuration register
- Gain and Status register

The volatile memory starts functioning when the device V_{DD} is at (or above) the RAM retention voltage (V_{RAM}). The volatile memory will be loaded with the default device values when the V_{DD} rises across the V_{POR}/V_{BOR} voltage trip point.

After the device is powered-up, the user can update the device memory. Table 4-2 shows the volatile memory locations and their interaction due to a POR event.

4.2.2 NONVOLATILE REGISTER MEMORY (MTP)

This memory option is available only for the MCP48CMDXX devices.

MTP memory starts functioning below the device’s V_{POR}/V_{BOR} trip point and, once the V_{POR} event occurs, the volatile memory registers are loaded with the corresponding MTP register memory values.

Memory addresses 0Ch through 1Fh are nonvolatile memory locations. These locations contain the DAC POR/BOR wiper values, the DAC POR/BOR configuration bits and 8 general purpose memory locations for storing user-defined data as calibration constants or identification numbers.

The nonvolatile wiper registers and configuration bits determine the DAC Output and Configuration values at the POR event.

These nonvolatile values will overwrite the factory default values. If these MTP addresses are unprogrammed, the factory default values define the output state.

The nonvolatile DAC registers enable the standalone operation of the device (without microcontroller control), after being programmed to the desired values.

To program nonvolatile memory locations, a high-voltage source on the $\overline{\text{LAT}}$/HVC pin is required. Each register/MTP location can be programmed 32 times. After 32 writes, a new write operation will not be possible and the last successful value written will remain associated with the memory location.

The device starts writing the MTP memory cells at the completion of the serial interface command. The high voltage must remain present on the $\overline{\text{LAT}}$/HVC pin until the write cycle is complete; otherwise, the write is unsuccessful and the location is compromised (cannot be used again and the number of available writes decreases by one).

To recover from an aborted MTP write operation, the following procedure must be used:

- Write any valid value to the same address again
- Force a POR condition
- Write the desired value to the MTP location again

It is recommended to keep high voltage on only during the MTP write command and programming cycle; otherwise, the reliability of the device could be affected.

4.2.3 UNIMPLEMENTED LOCATIONS

4.2.3.1 Unimplemented Register Bits

When issuing read commands to a valid memory location with unimplemented bits, the unimplemented bits will be read as ‘`0`’.

4.2.4 UNIMPLEMENTED (RESERVED) LOCATIONS

There are a number of unimplemented memory locations that are reserved for future use. Normal (voltage) commands (read or write) to any unimplemented memory address will result in a Command Error condition (SPI Command Error – CMDERR). High-Voltage commands to any unimplemented configuration bit(s) will also result in a Command Error condition.

4.2.5 POR/BOR OPERATION WITH WIPERLOCK™ TECHNOLOGY ENABLED

Regardless of the WiperLock Technology state, a POR event will load the Volatile DACx Wiper register value with the Nonvolatile DACx Wiper register value. Refer to **Section 4.1 “Power-on Reset/Brown-out Reset (POR/BOR)”** for further information.

TABLE 4-1: MCP48CXDX1/2 MEMORY MAP (16-BIT)

Address	Function	Single	Dual	Address	Function	Single(1)	Dual(1)
00h	Volatile DAC Wiper Register 0	Y	Y	10h	Nonvolatile DAC Wiper Register 0	Y	Y
01h	Volatile DAC Wiper Register 1	—	Y	11h	Nonvolatile DAC Wiper Register 1	—	Y
02h	Reserved	—	—	12h	Reserved	—	—
03h	Reserved	—	—	13h	Reserved	—	—
04h	Reserved	—	—	14h	Reserved	—	—
05h	Reserved	—	—	15h	Reserved	—	—
06h	Reserved	—	—	16h	Reserved	—	—
07h	Reserved	—	—	17h	Reserved	—	—
08h	Volatile VREF Register	Y	Y	18h	Nonvolatile VREF Register	Y	Y
09h	Volatile Power-Down Register	Y	Y	19h	Nonvolatile Power-Down Register	Y	Y
0Ah	Volatile Gain and Status Register	Y	Y	1Ah	NV Gain	Y	Y
0Bh	Reserved	—	—	1Bh	NV WiperLock™ Technology Register	Y	Y
0Ch	General Purpose MTP	(1)		1Ch	General Purpose MTP	(1)	
0Dh	General Purpose MTP	(1)		1Dh	General Purpose MTP	(1)	
0Eh	General Purpose MTP	(1)		1Eh	General Purpose MTP	(1)	
0Fh	General Purpose MTP	(1)		1Fh	General Purpose MTP	(1)	

Legend:

🟪	Volatile memory addresses
🟦	MTP memory addresses
⬜	Memory locations not implemented on this device family

Note 1: On nonvolatile memory devices only (MCP48CMDXX)

TABLE 4-2: FACTORY DEFAULT POR/BOR VALUES (MTP MEMORY UNPROGRAMMED)

Address	Function	POR/BOR Value		
		8-bit	10-bit	12-bit
00h	Volatile DAC0 Register	7Fh	1FFh	7FFh
01h	Volatile DAC1 Register	7Fh	1FFh	7FFh
02h	Reserved	—	—	—
03h	Reserved	—	—	—
04h	Reserved	—	—	—
05h	Reserved	—	—	—
06h	Reserved	—	—	—
07h	Reserved	—	—	—
08h	Volatile VREF Register	0000h	0000h	0000h
09h	Volatile Power-Down Register	0000h	0000h	0000h
0Ah	Volatile Gain and Status Register(2)	0080h	0080h	0080h
0Bh	Reserved	0000h	0000h	0000h
0Ch	General Purpose MTP(1)	—	—	—
0Dh	General Purpose MTP(1)	0000h	0000h	0000h
0Eh	General Purpose MTP(1)	0000h	0000h	0000h
0Fh	General Purpose MTP(1)	0000h	0000h	0000h

Address	Function	POR/BOR Value		
		8-bit	10-bit	12-bit
10h	Nonvolatile DAC0 Wiper Register(1)	7Fh	1FFh	7FFh
11h	Nonvolatile DAC1 Wiper Register(1)	7Fh	1FFh	7FFh
12h	Reserved	—	—	—
13h	Reserved	—	—	—
14h	Reserved	—	—	—
15h	Reserved	—	—	—
16h	Reserved	—	—	—
17h	Reserved	—	—	—
18h	Nonvolatile VREF register(1)	0000h	0000h	0000h
19h	Nonvolatile Power-Down Register(1)	0000h	0000h	0000h
1Ah	NV Gain(1)	0000h	0000h	0000h
1Bh	NV WiperLock™ Technology Register(1)	0000h	0000h	0000h
1Ch	General Purpose MTP(1)	0000h	0000h	0000h
1Dh	General Purpose MTP(1)	0000h	0000h	0000h
1Eh	General Purpose MTP(1)	0000h	0000h	0000h
1Fh	General Purpose MTP(1)	0000h	0000h	0000h

	Legend:
🟪	Volatile memory address range
🟦	Nonvolatile memory address range
⬜	Not implemented

Note 1: On nonvolatile devices only (MCP48CMDXX).

2: The ‘1’ bit is the POR status bit, which is set after the POR event and cleared after address 0Ah is read.

4.2.6 DEVICE REGISTERS

Register 4-1 shows the format of the DAC Output Value registers for the volatile memory locations. These registers will be either 8 bits, 10 bits or 12 bits wide. The values are right justified.

REGISTER 4-1: DAC0 (00H/10H) AND DAC1 (01H/11H) OUTPUT VALUE REGISTERS (VOLATILE/NONVOLATILE)

	U-0	U-0	U-0	U-0	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n	R/W-n
12-bit	—	—	—	—	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
10-bit	—	—	—	—	—	—	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
8-bit	—	—	—	—	—	—	—	—	D07	D06	D05	D04	D03	D02	D01	D00

bit 15 bit 0

Legend:

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
-n = Value at POR
‘1’ = Bit is set
‘0’ = Bit is cleared
x = Bit is unknown
🟪 = 12-bit device
🟦 = 10-bit device
☐ = 8-bit device

12-bit	**10-bit**	**8-bit**	
bit 15-12	bit 15-10	bit 15-8	**Unimplemented:** Read as ‘0’
bit 11-0	—	—	**D11-D00:** DAC Output value – 12-bit devices FFFh = Full-Scale output value 7FFh = Mid-Scale output value 000h = Zero-Scale output value
—	bit 9-0	—	**D09-D00:** DAC Output value – 10-bit devices 3FFh = Full-Scale output value 1FFh = Mid-Scale output value 000h = Zero-Scale output value
—	—	bit 7-0	**D07-D00:** DAC Output value – 8-bit devices FFh = Full-Scale output value 7Fh = Mid-Scale output value 00h = Zero-Scale output value

Note 1: Unimplemented bit, read as ‘0’.

Register 4-2 shows the format of the Voltage Reference Control register. Each DAC has two bits to control the source of the voltage reference of the DAC. This register is for the volatile memory locations. The width of this register is two times the number of DACs for the device.

REGISTER 4-2: VOLTAGE REFERENCE (VREF) CONTROL REGISTERS (08h/18h) (VOLATILE/NONVOLATILE)

	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-n	R/W-n	R/W-n	R/W-n
Single	—	—	—	—	—	—	—	—	—	—	—	—	—(1)	—(1)	VR0B	VR0A
Dual	—	—	—	—	—	—	—	—	—	—	—	—	VR1B	VR1A	VR0B	VR0A

bit 15 bit 0

Legend:

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
-n = Value at POR
‘1’ = Bit is set
‘0’ = Bit is cleared
x = Bit is unknown
🟪 = Single channel device
☐ = Dual channel device

Single	Dual	
bit 15-2	bit 15-4	**Unimplemented:** Read as ‘`0`’
bit 1-0	bit 3-0	**VRxB-VRxA:** DAC Voltage Reference Control bits `11` = V_{REF} pin (Buffered); V_{REF} buffer enabled `10` = V_{REF} pin (Unbuffered); V_{REF} buffer disabled `01` = Internal band gap(2) (1.214V typical); V_{REF} buffer enabled. V_{REF} voltage driven when powered-down. `00` = V_{DD} (Unbuffered); V_{REF} buffer disabled. Use this state with power-down bits for lowest current.

Note 1: Unimplemented bit, read as ‘`0`’.

2: When the internal band gap is selected, the band gap voltage source will continue to output the voltage on the V_{REF} pin in any of the Power-Down modes. To reduce the power consumption to its lowest level (band gap disabled), after selecting the desired Power-Down mode, the voltage reference must be changed to V_{DD} or V_{REF} pin unbuffered (‘`00`’ or ‘`10`’), which turns off the internal band gap circuitry. After wake-up, the user needs to reselect the internal band gap (‘`01`’) for the voltage reference source.

Register 4-3 shows the format of the Power-Down Control register. Each DAC has two bits to control the Power-Down state of the DAC. This register is for the volatile and nonvolatile memory locations. The width of this register is two times the number of DACs for the device.

REGISTER 4-3: POWER-DOWN CONTROL REGISTERS (09h/19h) (VOLATILE/NONVOLATILE)

	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-n	R/W-n	R/W-n	R/W-n
Single	—	—	—	—	—	—	—	—	—	—	—	—	—(1)	—(1)	PD0B	PD0A
Dual	—	—	—	—	—	—	—	—	—	—	—	—	PD1B	PD1A	PD0B	PD0A
	bit 15															bit 0

Legend:
R = Readable bit W = Writable bit U = Unimplemented bit, read as ‘0’
-n = Value at POR ‘1’ = Bit is set ‘0’ = Bit is cleared x = Bit is unknown
▨ = Single channel device ☐ = Dual channel device

Single	Dual	
bit 15-2	bit 15-4	**Unimplemented:** Read as ‘0’
bit 1-0	bit 3-0	**PDxB-PDxA:** DAC Power-Down Control bits(2) 11 =Powered-Down – V_{OUT} is open circuit 10 =Powered-Down – V_{OUT} is loaded with a 100 kΩ resistor to ground 01 =Powered-Down – V_{OUT} is loaded with a 1 kΩ resistor to ground 00 =Normal Operation (not powered-down)

Note 1: Unimplemented bit, read as ‘0’.
2: See Table 5-5 for more details.

Register 4-4 shows the format of the Gain Control and System Status register. Each DAC has one bit to control the gain of the DAC and two Status bits.

REGISTER 4-4: GAIN CONTROL AND SYSTEM STATUS REGISTER (0Ah) (VOLATILE)

	U-0	U-0	U-0	U-0	U-0	U-0	R/W-n	R/W-n	R/C-1	R	U-0	U-0	U-0	U-0	U-0	U-0
Single	—	—	—	—	—	—	—[1]	G0	POR	MTPMA	—	—	—	—	—	—
Dual	—	—	—	—	—	—	G1	G0	POR	MTPMA	—	—	—	—	—	—
	bit 15															bit 0

Legend:			
R = Readable bit	W = Writable bit	C = Clearable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown
🟪 = Single channel device		☐ = Dual channel device	

Single	Dual	
bit 15-9	bit 15-10	**Unimplemented:** Read as ‘0’
—	bit 9	**G1:** DAC1 Output Driver Gain control bits 1 = 2x Gain. Not applicable when V_{DD} is used as V_{RL}(2) 0 = 1x Gain
bit 8	bit 8	**G0:** DAC0 Output Driver Gain control bits 1 = 2x Gain. Not applicable when V_{DD} is used as V_{RL}(2) 0 = 1x Gain
bit 7	bit 7	**POR:** Power-on Reset (Brown-out Reset) Status bit This bit indicates if a POR or BOR event has occurred since the last read command of this register. Reading this register clears the state of the POR Status bit. 1 = A POR (BOR) event occurred since the last read of this register. Reading this register clears this bit. 0 = A POR (BOR) event has not occurred since the last read of this register.
bit 6	bit 6	**MTPMA:** MTP Memory Access Status bit(3) This bit indicates if the MTP Memory Access is occurring. 1 = An MTP Memory Access is currently occurring (during the POR MTP read cycle or an MTP write cycle is occurring). Only serial commands addressing the volatile memory are allowed. 0 = An MTP Memory Access is NOT currently occurring
bit 5-0	bit 5-0	**Unimplemented:** Read as ‘0’

Note 1: Unimplemented bit, read as ‘0’.

2: The DAC’s Gain bit is ignored and the gain is forced to 1x (Gx = 0) when the DAC voltage reference is selected as V_{DD} (VRxB:VRxA = 00).

3: For volatile memory devices, this bit is read as ‘0’.

Register 4-5 shows the format of the Nonvolatile Gain Control register. Each DAC has one bit to control the gain of the DAC.

REGISTER 4-5: GAIN CONTROL REGISTER (1Ah) (NONVOLATILE)

	U-0	U-0	U-0	U-0	U-0	U-0	R/W-n	R/W-n	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
Single	—	—	—	—	—	—	—[1]	G0	—	—	—	—	—	—	—	—
Dual	—	—	—	—	—	—	G1	G0	—	—	—	—	—	—	—	—

bit 15 bit 0

Legend:

R = Readable bit	W = Writable bit	C = Clearable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown
🟪 = Single channel device		☐ = Dual channel device	

Single	Dual	
bit 15-10	bit 15-10	**Unimplemented:** Read as ‘0’
bit 9-8	bit 9-8	**Gx**[2]: DAC Output Driver Gain control bits 1 = 2x Gain 0 = 1x Gain
bit 7-0	bit 7-0	**Unimplemented:** Read as ‘0’

Note 1: Unimplemented bit, read as ‘0’.

2: When the DAC voltage reference is selected as V_{DD} (VRxB:VRxA = 00), the DAC’s Gain bit is ignored and the gain is forced to 1x (Gx = 0).

Register 4-6 shows the format of the DAC WiperLock Technology Status register. The width of this register is two times the number of DACs for the device.

WiperLock Technology bits only control access to volatile memory. Nonvolatile memory write access is controlled by the requirement of high voltage on the HVC pin, which is recommended to not be available during normal device operation.

REGISTER 4-6: WIPERLOCK™ TECHNOLOGY CONTROL REGISTER (1BH) (NONVOLATILE)

	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-n	R/W-n	R/W-n	R/W-n
Single	—	—	—	—	—	—	—	—	—	—	—	—	—(1)	—(1)	WL0B	WL0A
Dual	—	—	—	—	—	—	—	—	—	—	—	—	WL1B	WL1A	WL0B	WL0A
	bit 15															bit 0

Legend:

R = Readable bit	W = Writable bit	C = Clearable bit	U = Unimplemented bit, read as ‘0’
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown
▨ = Single channel device		☐ = Dual channel device	

Single	Dual	
bit 15-2	bit 15-4	**Unimplemented:** Read as ‘0’
bit 1-0	bit 3-0	**WLXB-WLXA:** WiperLock™ Technology Status bits(2) 11 = Vol. DAC Wiper register and Vol. DAC configuration bits are locked 10 = Vol. DAC Wiper register is locked, and Vol. DAC configuration bits are unlocked 01 = Vol. DAC Wiper register is unlocked, and Vol. DAC configuration bits are locked 00 = Vol. DAC Wiper register and Vol. DAC configuration bits are unlocked

Note 1: Unimplemented bit, read as ‘0’.

2: The volatile PDxB:PDxA bits are NOT locked due to the requirement of being able to exit Power-Down mode.

NOTES:

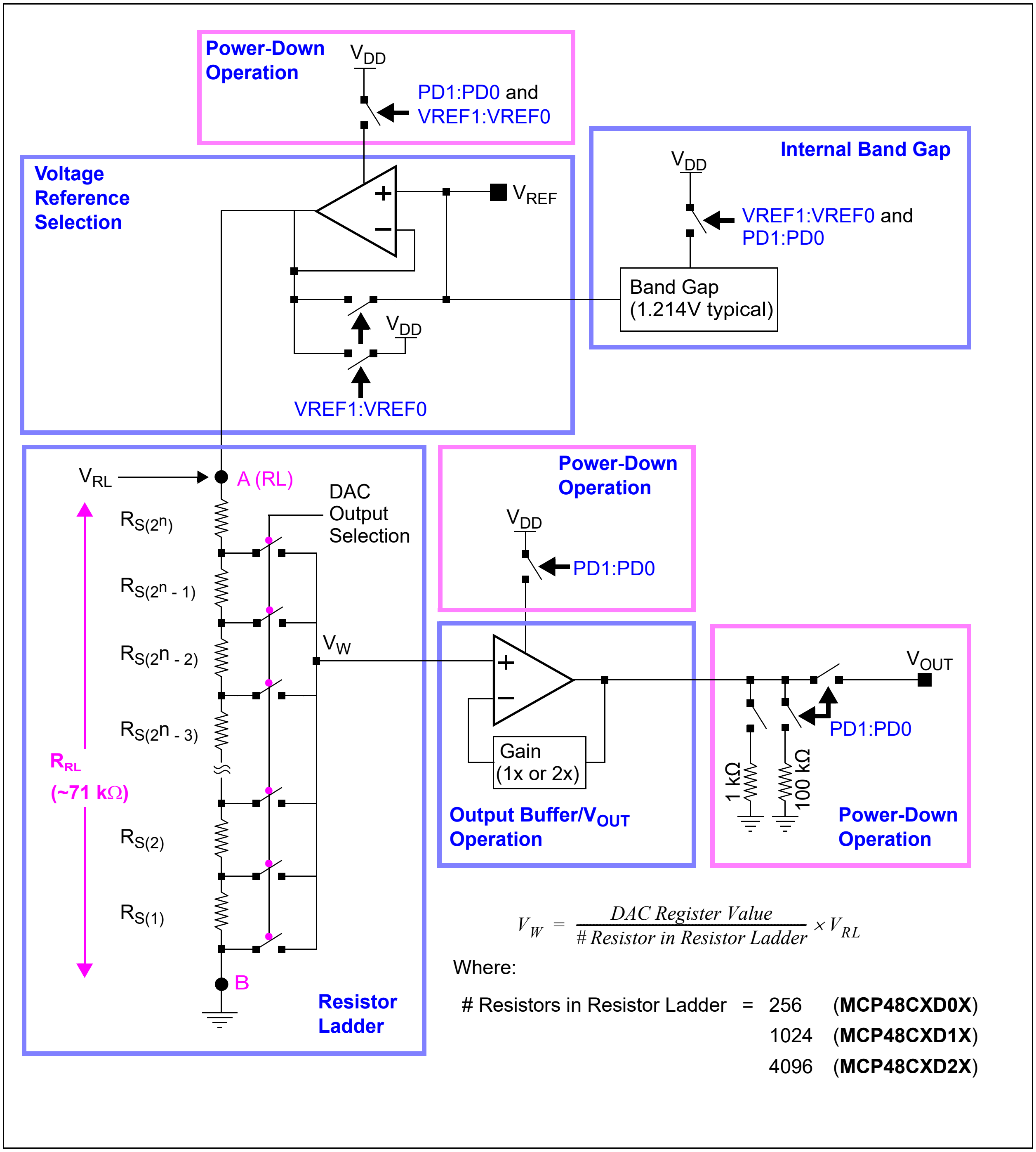
5.0 DAC CIRCUITRY

The Digital to Analog Converter circuitry converts a digital value into its analog representation. The description describes the functional operation of the device.

The DAC circuit uses a resistor ladder implementation. Devices have up to two DACs. The figure below shows the functional block diagram for the MCP48CXDX1/2 DAC circuitry.

The functional blocks of the DAC include:

- **Resistor Ladder**
- **Voltage Reference Selection**
- **Output Buffer/V_{OUT} Operation**
- **Latch Pin (LAT)**
- **Power-Down Operation**



$$V_W = \frac{DAC\ Register\ Value}{\#\ Resistor\ in\ Resistor\ Ladder} \times V_{RL}$$

Where:

Resistors in Resistor Ladder = 256 (**MCP48CXD0X**)
1024 (**MCP48CXD1X**)
4096 (**MCP48CXD2X**)

FIGURE 5-1: *MCP48CXDX1/2 DAC Module Block Diagram.*

5.1 Resistor Ladder

The resistor ladder is a digital potentiometer with the A Terminal connected to the selected reference voltage and the B Terminal internally grounded (see Figure 5-2). The volatile DAC register controls the wiper position. The wiper voltage (V_W) is proportional to the DAC register value divided by the number of resistor elements (R_S) in the ladder (256, 1024 or 4096) related to the V_{RL} voltage.

The output of the resistor network will drive the input of an output buffer.

The Resistor Network is made up of three parts:

- Resistor ladder (string of R_S elements)
- Wiper switches
- DAC register decode

The resistor ladder has a typical impedance (R_{RL}) of approximately 71 kΩ. This resistor ladder resistance (R_{RL}) may vary from device to device up to ±10%. This is a voltage divider configuration; therefore, the actual R_{RL} resistance does not affect the output, given a fixed voltage at V_{RL}.

Equation 5-1 shows the calculation for the step resistance.

Note:	The maximum wiper position is $2^n - 1$, while the number of resistors in the resistor ladder is 2^n. This means that when the DAC register is at full scale, there is one resistor element (R_S) between the wiper and the V_{RL} voltage.

If the unbuffered V_{REF} pin is used as the V_{RL} voltage source, the external voltage source must have a low output impedance.

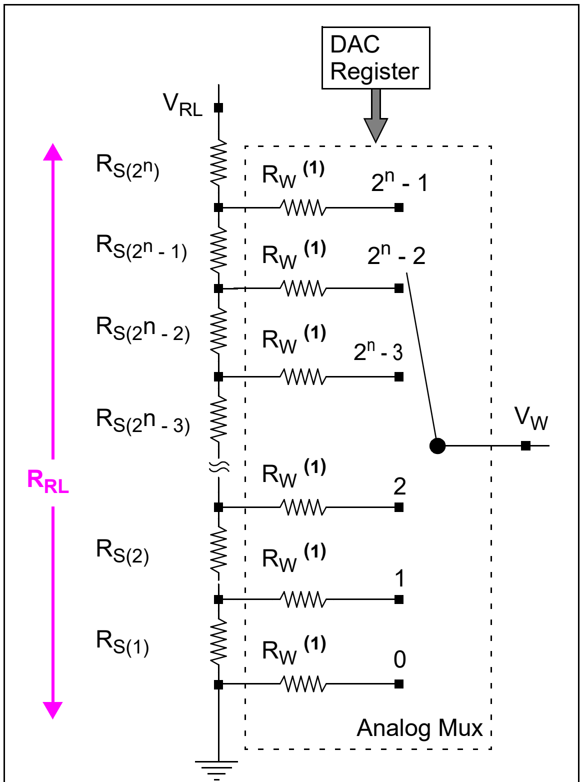
When the DAC is powered down, the resistor ladder is disconnected from the selected reference voltage.

EQUATION 5-1: R_S CALCULATION

$$R_S = \frac{R_{RL}}{(256)} \quad \text{8-bit Device}$$

$$R_S = \frac{R_{RL}}{(1024)} \quad \text{10-bit Device}$$

$$R_S = \frac{R_{RL}}{(4096)} \quad \text{12-bit Device}$$



Note 1: The analog switch resistance (R_W) does not affect performance due to the voltage divider configuration.

FIGURE 5-2: Resistor Ladder Model Block Diagram.

5.2 Voltage Reference Selection

The resistor ladder has up to four sources for the reference voltage. The selection of the voltage reference source is specified with the volatile VREF1:VREF0 configuration bits (see Register 4-2). The selected voltage source is connected to the V_{RL} node (see Figure 5-3 and Figure 5-4).

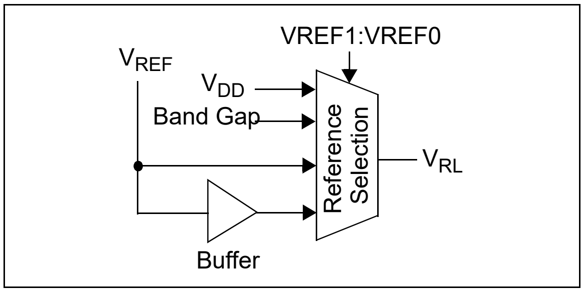


FIGURE 5-3: *Resistor Ladder Reference Voltage Selection Block Diagram.*

The four voltage source options for the resistor ladder are:

1. V_{DD} pin voltage
2. Internal band gap voltage reference (V_{BG})
3. V_{REF} pin voltage – unbuffered
4. V_{REF} pin voltage – internally buffered

On a POR/BOR event, the default configuration state or the value written in the nonvolatile register is latched into the volatile VREF1:VREF0 configuration bits.

If the V_{REF} pin is used with an external voltage source, then the user must select between Buffered or Unbuffered mode.

5.2.1 USING V_{DD} AS V_{REF}

When the user selects the V_{DD} as the reference, the V_{REF} pin voltage is not connected to the resistor ladder. The V_{DD} voltage is internally connected to the resistor ladder.

5.2.2 USING AN EXTERNAL V_{REF} SOURCE IN UNBUFFERED MODE

In this case, the V_{REF} pin voltage may vary from V_{SS} to V_{DD}. The voltage source must have a low-output impedance. If the voltage source has a high-output impedance, the voltage on the V_{REF} pin can be lower than expected. The resistor ladder has a typical impedance of 71 kΩ and a typical capacitance of 29 pF.

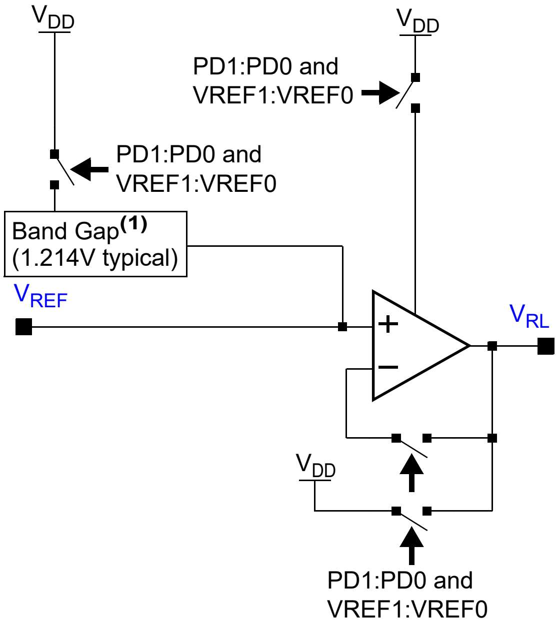
If a single V_{REF} pin is supplying multiple DACs, the V_{REF} pin source must have adequate current capability to support the number of DACs. It must be assumed that the resistor ladder resistance (R_{RL}) of each DAC is at the minimum specified resistance and these resistances are in parallel.

If the V_{REF} pin is tied to the V_{DD} voltage, selecting the V_{DD} Reference mode (VREF1:VREF0 = `00`) is recommended.

5.2.3 USING AN EXTERNAL V_{REF} SOURCE IN BUFFERED MODE

The V_{REF} pin voltage may be from 0V to V_{DD}. The input buffer (amplifier) provides low offset voltage, low noise and a very high input impedance, with only minor limitations on the input range and frequency response.

Any variation or noises on the reference source can directly affect the DAC output. The reference voltage needs to be as clean as possible for accurate DAC performance.



Note 1: The band gap voltage (V_{BG}) is 1.214V typical. The band gap output goes through the buffer with a 2X gain to create the V_{RL} voltage. See Table 5-1 for additional information on the band gap circuit.

FIGURE 5-4: *Reference Voltage Selection Implementation Block Diagram.*

5.2.4 USING THE INTERNAL BAND GAP AS VOLTAGE REFERENCE

The internal band gap is designed to drive the resistor ladder buffer.

If the internal band gap is selected, the band gap voltage source will drive the external V_{REF} pins. The V_{REF1} pin must be left unloaded in this mode. The voltage reference source can be independently selected on devices with two DAC channels, but restrictions apply:

- The V_{DD} mode can be used without issues on any channel.
- When the internal band gap is selected as the voltage source, all the V_{REF} pins are connected to its output. The use of the Unbuffered mode is only possible on V_{REF0}, because it is the only one that can be loaded.
- When using the Internal Band Gap mode on channel 0, channel 1 must be put in Buffered External V_{REF} mode or V_{DD} Reference mode and the V_{REF1} pin must be left unloaded.

The resistance of the resistor ladder (R_{RL}) is targeted to be 71 kΩ (±10%), which means a minimum resistance of 63.9 kΩ.

The band gap selection can be used across the V_{DD} voltages while maximizing the V_{OUT} voltage ranges. For V_{DD} voltages below the Gain $*$ V_{BG} voltage, the output for the upper codes will be clipped to the V_{DD} voltage. The table below shows the maximum DAC register code given device V_{DD} and Gain bit setting.

TABLE 5-1: V_{OUT} USING BAND GAP

V_{DD}	DAC Gain	Max DAC Code[1]			Comment
		12-bit	10-bit	8-bit	
5.5	1	FFFh	3FFh	FFh	$V_{OUT(max)} = 1.214V$[3]
	2	FFFh	3FFh	FFh	$V_{OUT(max)} = 2.428V$[3]
2.7	1	FFFh	3FFh	FFh	$V_{OUT(max)} = 1.214V$[3]
	2	FFFh	3FFh	FFh	$V_{OUT(max)} = 2.428V$
1.8	1	FFFh	3FFh	FFh	$V_{OUT(max)} = 1.214V$
	2[2]	BBCh	2EFh	BBh	1.8V

Note 1: Without the V_{OUT} pin voltage being clipped.
2: Recommended to use the Gain = `1` setting.
3: When V_{BG} = 1.214V typical.

5.3 Output Buffer/V_{OUT} Operation

The output driver buffers the wiper voltage (V_W) of the resistor ladder.

The DAC output is buffered with a low-power, precision output amplifier with selectable gain. This amplifier provides a rail-to-rail output with low offset voltage and low noise. The amplifier's output can drive the resistive and high-capacitive loads without oscillation. The amplifier provides a maximum load current that is enough for most programmable voltage reference applications. Refer to **Section 1.0 "Electrical Characteristics"** for the specifications of the output amplifier.

> **Note:** The load resistance must be kept higher than 2 kΩ to maintain stability of the analog output and have it meet electrical specifications.

The figure below shows a block diagram of the output driver circuit.

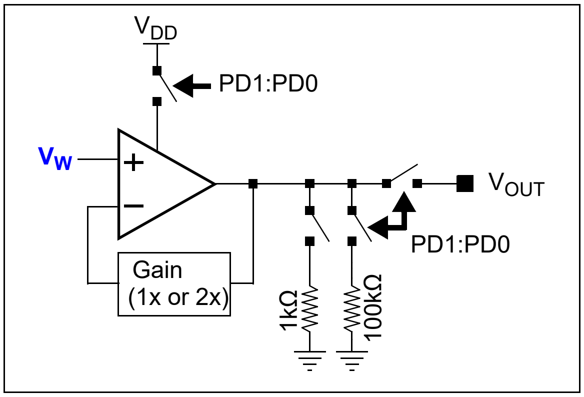


FIGURE 5-5: Output Driver Block Diagram.

Power-Down logic also controls the output buffer operation (see **Section 5.5 "Power-Down Operation"** for additional information on Power-Down). In any of the three Power-Down modes, the output amplifier is powered down and its output becomes a high impedance to the V_{OUT} pin.

5.3.1 PROGRAMMABLE GAIN

The amplifier's gain is controlled by the Gain (G) Configuration bit (see Register 4-4) and the V_{RL} reference selection (see Register 4-2).

The Gain options are:

a) Gain of '`1`', with either the V_{DD} or V_{REF} pin used as reference voltage.

b) Gain of '`2`', only when the V_{REF} pin or the internal band gap is used as reference voltage. The V_{REF} pin voltage must be limited to $V_{DD}/2$. When the reference voltage selection (V_{RL}) is the device's V_{DD} voltage, the G bit is ignored and a gain of '`1`' is used.

The table below shows the gain bit operation.

TABLE 5-2: OUTPUT DRIVER GAIN

Gain Bit	Gain	Comment
0	1	
1	2	Limits V_{REF} pin voltages relative to device V_{DD} voltage

The volatile G bit value can be modified by:

- POR event
- BOR event
- SPI write commands

5.3.2 OUTPUT VOLTAGE

The volatile DAC register values, along with the device's configuration bits, control the analog V_{OUT} voltage. The volatile DAC register's value is unsigned binary. The formula for the output voltage is provided in the equation below. Examples of volatile DAC register values and the corresponding theoretical V_{OUT} voltage for the MCP48CXDX1/2 devices are shown in Table 5-6.

EQUATION 5-2: CALCULATING OUTPUT VOLTAGE (V_{OUT})

$$V_{OUT} = \frac{V_{RL} \times DAC\ Register\ Value}{\#\ Resistor\ in\ Resistor\ Ladder} \times Gain$$

Where:

Resistors in R-Ladder = 4096 (**MCP48CXD2X**)
1024 (**MCP48CXD1X**)
256 (**MCP48CXD0X**)

When Gain = 2 ($V_{RL} = V_{REF}$), if $V_{REF} > V_{DD}/2$, the V_{OUT} voltage is limited to V_{DD}. So, if $V_{REF} = V_{DD}$, the V_{OUT} voltage does not change for volatile DAC register values mid-scale and greater because the output amplifier is at full-scale output.

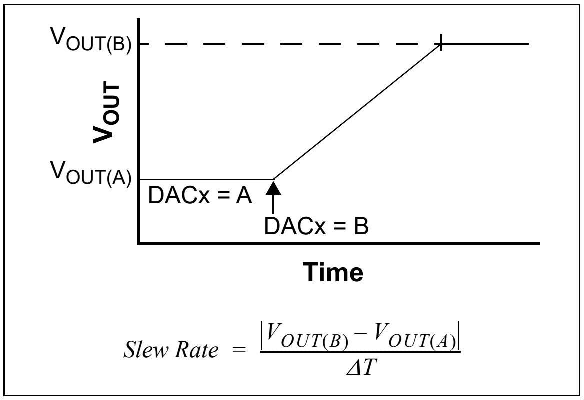
The following events update the DAC register value and, therefore, the analog voltage output (V_{OUT}):

- Power-on Reset
- Brown-out Reset
- SPI write command (to volatile registers)

Next, the V_{OUT} voltage starts driving to the new value after the event has occurred.

5.3.3 OUTPUT SLEW RATE

The figure below shows an example of the slew rate of the V_{OUT} pin. The slew rate can be affected by the characteristics of the circuit connected to the V_{OUT} pin.



$$Slew\ Rate = \frac{|V_{OUT(B)} - V_{OUT(A)}|}{\Delta T}$$

FIGURE 5-6: *V_{OUT} Pin Slew Rate.*

5.3.3.1 Small Capacitive Load

With a small capacitive load, the output buffer's current is not affected by the capacitive load (C_L). But still, the V_{OUT} pin's voltage is not a step transition from one output value (DAC register value) to the next output value. The change of the V_{OUT} voltage is limited by the output buffer's characteristics, so the V_{OUT} pin voltage will have a slope from the old voltage to the new voltage. This slope is fixed for the output buffer, and is referred to as the buffer slew rate (SR_{BUF}).

5.3.3.2 Large Capacitive Load

With a larger capacitive load, the slew rate is determined by two factors:

- The output buffer's short-circuit current (I_{SC})
- The V_{OUT} pin's external load

I_{OUT} cannot exceed the output buffer's short-circuit current (I_{SC}), which fixes the output buffer slew rate (SR_{BUF}). The voltage on the capacitive load (C_L), V_{CL}, changes at a rate proportional to I_{OUT}, which fixes a capacitive load slew rate (SR_{CL}).

So the V_{CL} voltage slew rate is limited to the slower of the output buffer's internally set slew rate (SRBUF) and the capacitive load slew rate (SR_{CL}).

5.3.4 DRIVING RESISTIVE AND CAPACITIVE LOADS

The V_{OUT} pin can drive up to 100 pF of capacitive load in parallel with a 5-kΩ resistive load (to meet electrical specifications). V_{OUT} drops slowly as the load resistance decreases after about 3.5 kΩ. It is recommended that a load with R_L greater than 2 kΩ be used.

Refer to the Characterization Data documents for a detailed V_{OUT} vs. resistive load characterization graph.

Driving large capacitive loads can cause stability problems for voltage feedback output amplifiers. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response with overshoot and ringing in the step response. That is, the V_{OUT} pin's voltage does not quickly follow the buffer's input voltage (due to the large capacitive load); therefore, the output buffer will overshoot the desired target voltage. Once the driver detects this overshoot, it compensates by forcing it to a voltage below the target. This causes voltage ringing on the V_{OUT} pin.

So, when driving large capacitive loads with the output buffer, a small series resistor (R_{ISO}) at the output (see the figure below) improves the output buffer's stability (feedback loop's phase margin) by making the output load resistive at higher frequencies. The bandwidth will generally be lower than the bandwidth with no capacitive load.

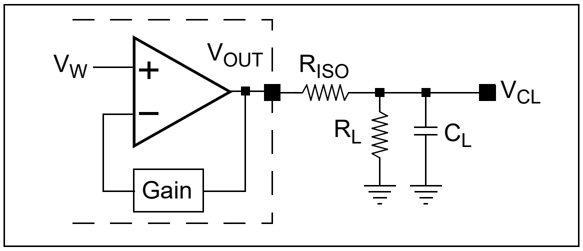


FIGURE 5-7: *Circuit to Stabilize Output Buffer for Large Capacitive Loads (C_L).*

The R_{ISO} resistor value for your circuit needs to be selected. The resulting frequency response peaking and step response overshoot for this R_{ISO} resistor value must be verified on the bench. Modify the R_{ISO}'s resistance value until the output characteristics meet your requirements.

A method to evaluate the system's performance is to inject a step voltage on the V_{REF} pin and observe the V_{OUT} pin's characteristics.

> **Note:** Additional insight into circuit design for driving capacitive loads can be found in AN884 – *"Driving Capacitive Loads With Op Amps"* (DS00000884).

5.3.5 STEP VOLTAGE (V_S)

The step voltage depends on the device resolution and the calculated output voltage range. 1 LSb is defined as the ideal voltage difference between two successive codes. The step voltage can easily be calculated using the equation below (the DAC register value is equal to 1). Theoretical step voltages are shown in Table 5-3 for several V_{REF} voltages.

EQUATION 5-3: V_S CALCULATION

$$V_S = \frac{V_{RL}}{\#\ Resistor\ in\ Resistor\ Ladder} \times Gain$$

Where:

Resistors in R-Ladder = 4096 (**12-bit**)
1024 (**10-bit**)
256 (**8-bit**)

TABLE 5-3: THEORETICAL STEP VOLTAGE (V_S)[1]

Step Voltage	V_{REF}					#bits
	5.0	2.7	1.8	1.5	1.0	
V_S	1.22 mV	659 µV	439 µV	366 µV	244 µV	12-bit
	4.88 mV	2.64 mV	1.76 mV	1.46 mV	977 µV	10-bit
	19.5 mV	10.5 mV	7.03 mV	5.86 mV	3.91 mV	8-bit

Note 1: When Gain = 1X, $V_{FS} = V_{RL}$ and V_{ZS} = 0V.

5.4 Latch Pin ($\overline{\text{LAT}}$)

The Latch pin controls when the volatile DAC register value is transferred to the DAC wiper. This is useful for applications that need to synchronize the wiper(s) updates to an external event, such as zero crossing or updates to the other wipers on the device. The $\overline{\text{LAT}}$ pin is asynchronous to the serial interface operation.

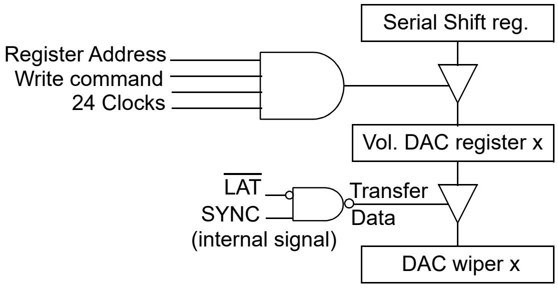
When the $\overline{\text{LAT}}$ pin is high, transfers from the volatile DAC register to the DAC wiper are inhibited. The volatile DAC register value(s) can continue to be updated.

When the $\overline{\text{LAT}}$ pin is low, the volatile DAC register value is transferred to the DAC wiper.

> **Note:** This allows both the volatile DAC0 and DAC1 registers to be updated while the $\overline{\text{LAT}}$ pin is high and to have outputs synchronously updated as the $\overline{\text{LAT}}$ pin is driven low.

The figure below shows the interaction of the $\overline{\text{LAT}}$ pin and the loading of the DAC wiper x (from the volatile DAC register x). The transfers are level driven. If the $\overline{\text{LAT}}$ pin is held low, the corresponding DAC wiper is updated as soon as the volatile DAC register value is updated.

The $\overline{\text{LAT}}$ pin allows the DAC wiper to be updated to an external event and to have multiple DAC channels/devices update at a common event.



$\overline{\text{LAT}}$	SYNC	Transfer Data	Comment
1	1	0	No Transfer
1	0	0	No Transfer
0	1	1	Vol. DAC register x → DAC wiper x
0	0	0	No Transfer

FIGURE 5-8: $\overline{\text{LAT}}$ and DAC Interaction.

The DAC wiper x is updated from the volatile DAC register x; therefore, all DACs that are associated with a given $\overline{\text{LAT}}$ pin can be updated synchronously.

If the application does not require synchronization, this signal must be tied low.

The figure below shows two cases of using the $\overline{\text{LAT}}$ pin to control when the wiper register is updated relative to the value of a sine wave signal.

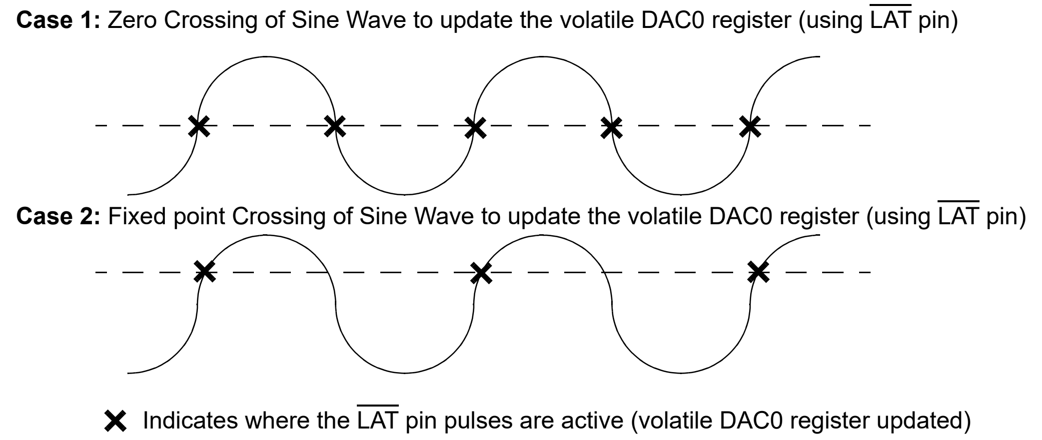


FIGURE 5-9: Example Use of $\overline{\text{LAT}}$ Pin Operation.

5.5 Power-Down Operation

To allow the application to conserve power when DAC operation is not required, three Power-Down modes are available. On devices with multiple DACs, each DAC's Power-Down mode is individually controllable.

All Power-Down modes do the following:

- Turn off most of the DAC module's internal circuits
- Op amp is powered down and the V_{OUT} pin becomes high-impedance
- Retain the value of the volatile DAC register and configuration bits

Depending on the selected Power-Down mode, the following will occur:

- V_{OUT} pin is switched to one of the two resistive pull-downs:
  - 100 kΩ (typical)
  - 1 kΩ (typical)

The Power-Down configuration bits (PD1:PD0) control the power-down operation, shown in the table below.

TABLE 5-4: POWER-DOWN BITS AND OUTPUT RESISTIVE LOAD

PD1	PD0	Function
`0`	`0`	Normal operation
`0`	`1`	1 kΩ resistor to ground
`1`	`0`	100 kΩ resistor to ground
`1`	`1`	Open circuit

There is a delay (T_{PDD}) between the PD1:PD0 bits changing from ‘`00`’ to either ‘`01`’, ‘`10`’ or ‘`11`’ and the op amp no longer driving the V_{OUT} output and the pull-down resistors sinking current.

In any of the Power-Down modes where the V_{OUT} pin is not externally connected (sinking or sourcing current), as the number of DACs increases, the device’s power-down current will also increase**.**

The following table shows the current sources for the DAC based on the selected source of the DAC’s reference voltage and if the device is in normal operating mode or one of the Power-Down modes.

TABLE 5-5: DAC CURRENT SOURCES

Device V_{DD} Current Source	PDxB:xA = `00`, VREFxB:xA =				PDxB:xA ≠ `00`, VREFxB:xA =			
	`00`	`01`	`10`	`11`	`00`	`01`	`10`	`11`
Output Op Amp	Y	Y	Y	Y	N	N	N	N
Resistor Ladder	Y	Y	N(1)	Y	N	N	N(1)	N
V_{REF} Selection Buffer	N	Y	N	Y	N	N	N	N
Band Gap	N	Y	N	N	N(2)	Y(2)	N(2)	N(2)

Note 1: The current is sourced from the V_{REF} pin, not the device V_{DD}.

2: If DAC0 and DAC1 are in one of the Power-Down modes, MTP write operations are not recommended.

The power-down bits are modified by using a write command to the volatile Power-Down register or a POR event, which transfers the nonvolatile Power-Down Register to the volatile Power-Down Register.

Section 7.0 “Device Commands” describes the SPI command for writing the power-down bits.

Note 1: The SPI serial interface circuit is not affected by the Power-Down mode. This circuit remains active in order to receive any command that might come from the SPI Host device.

5.5.1 EXITING POWER-DOWN

The following event changes the PD1:PD0 bits to ‘`00`’ and, therefore, exits the Power-Down mode. This is any SPI write command where the PD1:PD0 bits are ‘`00`’.

When the device exits Power-Down mode, the following occurs:

- Disabled internal circuits are turned on
- Resistor ladder is connected to the selected reference voltage (V_{RL})
- Selected pull-down resistor is disconnected
- The V_{OUT} output is driven to the voltage represented by the volatile DAC register’s value and configuration bits

DAC Wiper register and DAC Wiper value may be different due to the DAC Wiper register being modified while the $\overline{\text{LAT}}$ pin was driven to (and remaining at) V_{IH}.

The V_{OUT} output signal requires time as these circuits are powered-up and the output voltage is driven to the specified value as determined by the volatile DAC register and configuration bits.

Note: The op amp and resistor ladder were powered off (0V); therefore, the op amp’s input voltage (V_W) can be considered 0V. There is a delay (T_{PDE}) between the PD1:PD0 bits updating to ‘`00`’ and the op amp driving the V_{OUT} output. The op amp’s settling time (from 0V) needs to be taken into account to ensure the V_{OUT} voltage reflects the selected value.

TABLE 5-6: DAC INPUT CODE VS. CALCULATED ANALOG OUTPUT (V_{OUT}) (V_{DD} = 5.0V)

Device	Volatile DAC Register Value	V_{RL}(1)	LSb		Gain Selection(2)	V_{OUT}(3)	
			Equation	µV		Equation	V
MCP48CVD2X (12-bit)	`1111 1111 1111`	5.0V	5.0V/4096	1,220.7	1x	V_{RL} ∗ (4095/4096) ∗ 1	4.998779
		2.5V	2.5V/4096	610.4	1x	V_{RL} ∗ (4095/4096) ∗ 1	2.499390
					2x(2)	V_{RL} ∗ (4095/4096) ∗ 2)	4.998779
	`0111 1111 1111`	5.0V	5.0V/4096	1,220.7	1x	V_{RL} ∗ (2047/4096) ∗ 1)	2.498779
		2.5V	2.5V/4096	610.4	1x	V_{RL} ∗ (2047/4096) ∗ 1)	1.249390
					2x(2)	V_{RL} ∗ (2047/4096) ∗ 2)	2.498779
	`0011 1111 1111`	5.0V	5.0V/4096	1,220.7	1x	V_{RL} ∗ (1023/4096) ∗ 1)	1.248779
		2.5V	2.5V/4096	610.4	1x	V_{RL} ∗ (1023/4096) ∗ 1)	0.624390
					2x(2)	V_{RL} ∗ (1023/4096) ∗ 2)	1.248779
	`0000 0000 0000`	5.0V	5.0V/4096	1,220.7	1x	V_{RL} ∗ (0/4096) * 1)	0
		2.5V	2.5V/4096	610.4	1x	V_{RL} ∗ (0/4096) * 1)	0
					2x(2)	V_{RL} ∗ (0/4096) * 2)	0
MCP48CVD1X (10-bit)	`11 1111 1111`	5.0V	5.0V/1024	4,882.8	1x	V_{RL} ∗ (1023/1024) ∗ 1	4.995117
		2.5V	2.5V/1024	2,441.4	1x	V_{RL} ∗ (1023/1024) ∗ 1	2.497559
					2x(2)	V_{RL} ∗ (1023/1024) ∗ 2	4.995117
	`01 1111 1111`	5.0V	5.0V/1024	4,882.8	1x	V_{RL} ∗ (511/1024) ∗ 1	2.495117
		2.5V	2.5V/1024	2,441.4	1x	V_{RL} ∗ (511/1024) ∗ 1	1.247559
					2x(2)	V_{RL} ∗ (511/1024) ∗ 2	2.495117
	`00 1111 1111`	5.0V	5.0V/1024	4,882.8	1x	V_{RL} ∗ (255/1024) ∗ 1	1.245117
		2.5V	2.5V/1024	2,441.4	1x	V_{RL} ∗ (255/1024) ∗ 1	0.622559
					2x(2)	V_{RL} ∗ (255/1024) ∗ 2	1.245117
	`00 0000 0000`	5.0V	5.0V/1024	4,882.8	1x	V_{RL} ∗ (0/1024) ∗ 1	0
		2.5V	2.5V/1024	2,441.4	1x	V_{RL} ∗ (0/1024) ∗ 1	0
					2x(2)	V_{RL} ∗ (0/1024) ∗ 1	0
MCP48CVD0X (8-bit)	`1111 1111`	5.0V	5.0V/256	19,531.3	1x	V_{RL} ∗ (255/256) ∗ 1	4.980469
		2.5V	2.5V/256	9,765.6	1x	V_{RL} ∗ (255/256) ∗ 1	2.490234
					2x(2)	V_{RL} ∗ (255/256) ∗ 2	4.980469
	`0111 1111`	5.0V	5.0V/256	19,531.3	1x	V_{RL} ∗ (127/256) ∗ 1	2.480469
		2.5V	2.5V/256	9,765.6	1x	V_{RL} ∗ (127/256) ∗ 1	1.240234
					2x(2)	V_{RL} ∗ (127/256) ∗ 2	2.480469
	`0011 1111`	5.0V	5.0V/256	19,531.3	1x	V_{RL} ∗ (63/256) ∗ 1	1.230469
		2.5V	2.5V/256	9,765.6	1x	V_{RL} ∗ (63/256) ∗ 1	0.615234
					2x(2)	V_{RL} ∗ (63/256) ∗ 2	1.230469
	`0000 0000`	5.0V	5.0V/256	19,531.3	1x	V_{RL} ∗ (0/256) ∗ 1	0
		2.5V	2.5V/256	9,765.6	1x	V_{RL} ∗ (0/256) ∗ 1	0
					2x(2)	V_{RL} ∗ (0/256) ∗ 2	0

Note 1: V_{RL} is the resistor ladder's reference voltage. It is independent of the VREF1:VREF0 selection.

2: Gain selection of 2X (GX = `1`) requires the voltage reference source to come from the V_{REF} pin (VREF1:VREF0 = `10` or `11`) and requires V_{REF} pin voltage (or V_{RL}) ≤ V_{DD}/2 or from the internal band gap (VREF1:VREF0 = `01`).

3: These theoretical calculations do not take into account the Offset, Gain and Nonlinearity errors.

NOTES:

6.0 SPI SERIAL INTERFACE MODULE

The MCP48CXDX1/2's SPI serial interface module is a four-wire interface. The devices operate only as Clients (do not generate the Host clock). The figure below shows a typical SPI interface connection.

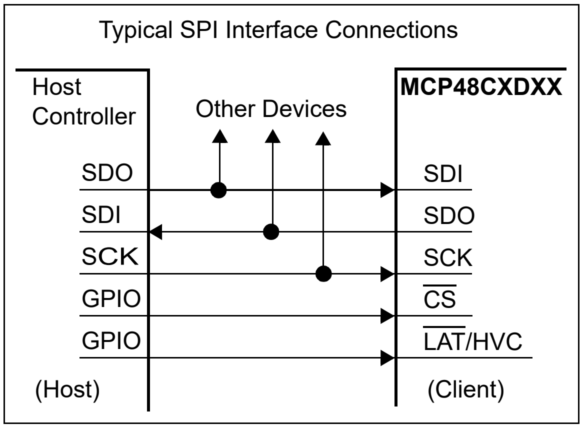


FIGURE 6-1: *Typical SPI Interface.*

The frame content (commands) for the MCP48CXDX1/2 are defined in **Section 7.0 "Device Commands"**.

6.1 Overview

This section discusses some of the specific characteristics of the MCP48CXDX1/2's SPI serial interface module. This is to assist in the development of your application.

The following sections discuss some of these device-specific characteristics:

- **Communication Data Rates**
- **POR/BOR**
- **Interface Pins (CS, SCK, SDI, SDO and LAT/HVC)**
- **Device Memory Address**
- **SPI Modes**

The MCP48CXDX1/2 devices support the SPI serial protocol. This SPI operates in Client mode (does not generate the serial clock).

The SPI interface uses four pins. These are:

- $\overline{\text{CS}}$ – Chip Select
- SCK – Serial Clock
- SDI – Serial Data In
- SDO – Serial Data Out

A fifth pin is used if a write is being done in the MTP memory. This pin is HVC – High-Voltage command (customer manufacturing only, multiplexed with $\overline{\text{LAT0}}$ functionality).

The HVC pin is used to program the MTP memory. This is intended to be used only during the customer's factory production flow. On volatile devices, the HVC pin is high-voltage tolerant. To enter a high-voltage command, the HVC pin must be greater than the V_{IHH} voltage.

Typical SPI Interfaces are shown in Figure 6-1. In the SPI interface, the Host's Output pin is connected to the Client's Input pin and the Host's Input pin is connected to the Client's Output pin.

The MCP48CXDX1/2 SPI module supports two (of the four) standard SPI modes. These are Mode `0,0` and `1,1`. The SPI mode is determined by the state of the SCK pin (V_{IH} or V_{IL}) when the $\overline{\text{CS}}$ pin transitions from inactive (V_{IH}) to active (V_{IL}).

6.2 Communication Data Rates

The MCP48CXDX1/2 supports clock rates (bit rates) of up to 25 MHz for read and 50 MHz for write commands.

For most applications, the write time will be considered more important because that is how the device operation is controlled.

6.3 POR/BOR

On a POR/BOR event, the SPI serial interface module state machine is reset, which includes forcing the device's memory address pointer to 00h.

6.4 Interface Pins ($\overline{\text{CS}}$, SCK, SDI, SDO and LAT/HVC)

The operation of the four interface pins and the High-Voltage command (HVC) pin is discussed in this section. The serial interface works on 24-bit boundaries. The $\overline{\text{CS}}$ pin frames the SPI commands.

6.4.1 SERIAL DATA IN (SDI)

The Serial Data In (SDI) signal is the data signal in the device. The value on this pin is latched on the rising edge of the SCK signal.

6.4.2 SERIAL DATA OUT (SDO)

The Serial Data Out (SDO) signal is the data signal out of the device. The value on this pin is driven on the falling edge of the SCK signal.

Once the $\overline{\text{CS}}$ pin is forced to the active level (V_{IL}), the SDO pin is driven. The state of the SDO pin is determined by the serial bit's position in the command, the selected command and if there is a state of command error (CMDERR).

6.4.3 SERIAL CLOCK (SCK) (SPI FREQUENCY OF OPERATION)

The SPI interface is specified to operate up to 50 MHz for write commands and 25 MHz for read commands. The actual clock rate depends on the configuration of the system and the serial command used. The table below shows the SCK frequency for different configurations.

TABLE 6-1: SCK FREQUENCY

Memory Type Access		Command	
		Read	Write
Nonvolatile Memory	SDI, SDO	25 MHz	50 MHz(1)
Volatile Memory	SDI, SDO	25 MHz	50 MHz(1)

Note 1: After issuing a write command to the NV locations, the internal write cycle must be completed before the next SPI command addressing the NV locations is received (t_{WC}).

6.4.4 THE $\overline{\text{CS}}$ SIGNAL

The $\overline{\text{CS}}$ signal is used to select the device and frame a command sequence. To start a command, or sequence of commands, the $\overline{\text{CS}}$ signal must transition from the inactive state (V_{IH}) to an active state (V_{IL}).

After the $\overline{\text{CS}}$ signal goes active, the SDO pin is driven and the clock bit counter is reset.

Note: There is a required delay after the $\overline{\text{CS}}$ pin goes active to the 1st edge of the SCK pin.

If an error condition occurs for an SPI command, the Command byte's Command Error (CMDERR) bit (on the SDO pin) will be driven low (V_{IL}). To exit the error condition, the user must take the $\overline{\text{CS}}$ pin to the V_{IH} level.

When the $\overline{\text{CS}}$ pin returns to the inactive state (V_{IH}), the SPI module resets (including the address pointer). While the $\overline{\text{CS}}$ pin is in the inactive state (V_{IH}), the serial interface is ignored. This allows the Host Controller to interface to other SPI devices using the same SDI, SDO and SCK signals.

6.4.5 HVC SIGNAL

The high-voltage requirement of the HVC pin for programming MTP registers ensures that a device in normal operation does not corrupt the values.

6.5 Device Memory Address

The memory address is the 5-bit value that specifies the location in the device's memory that the specified command will operate on.

On a POR/BOR event, the device's memory address pointer is forced to 00h.

6.6 SPI Modes

The SPI module supports two (of the four) standard SPI modes. These are Mode `0,0` and `1,1`. The MCP48CXDX1/2's SPI mode is automatically determined based on the Host's configured mode.

6.6.1 OPERATION IN SPI MODE `0,0`

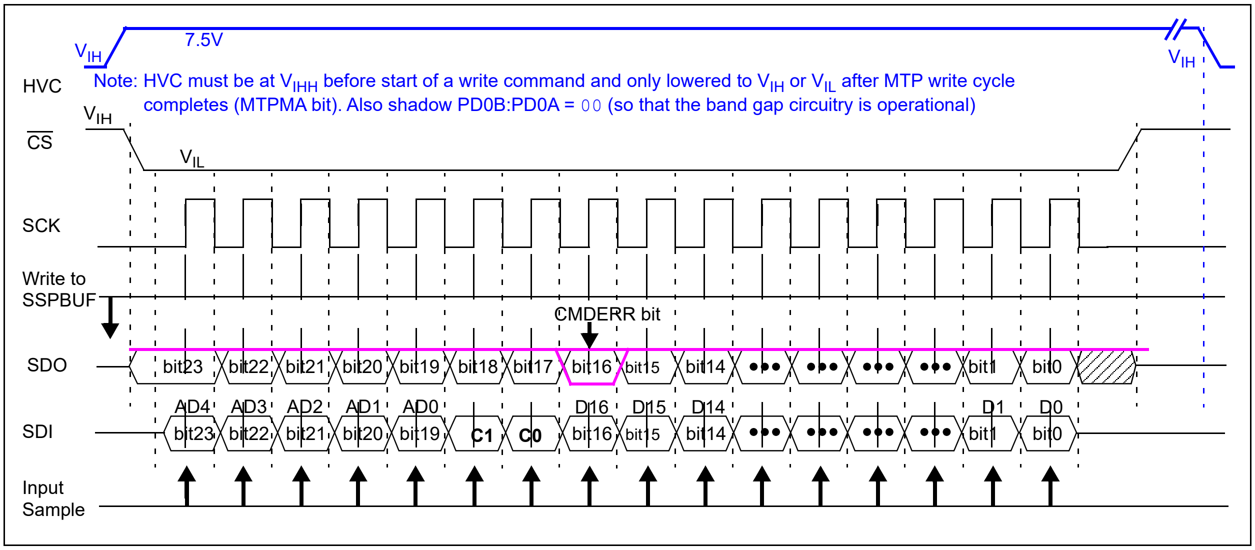
In SPI Mode `0,0`:

- SCK idle state = Low (V_{IL})
- Data are clocked in on the SDI pin on the rising edge of SCK
- Data are clocked out on the SDO pin on the falling edge of SCK

6.6.2 OPERATION IN SPI MODE `1,1`

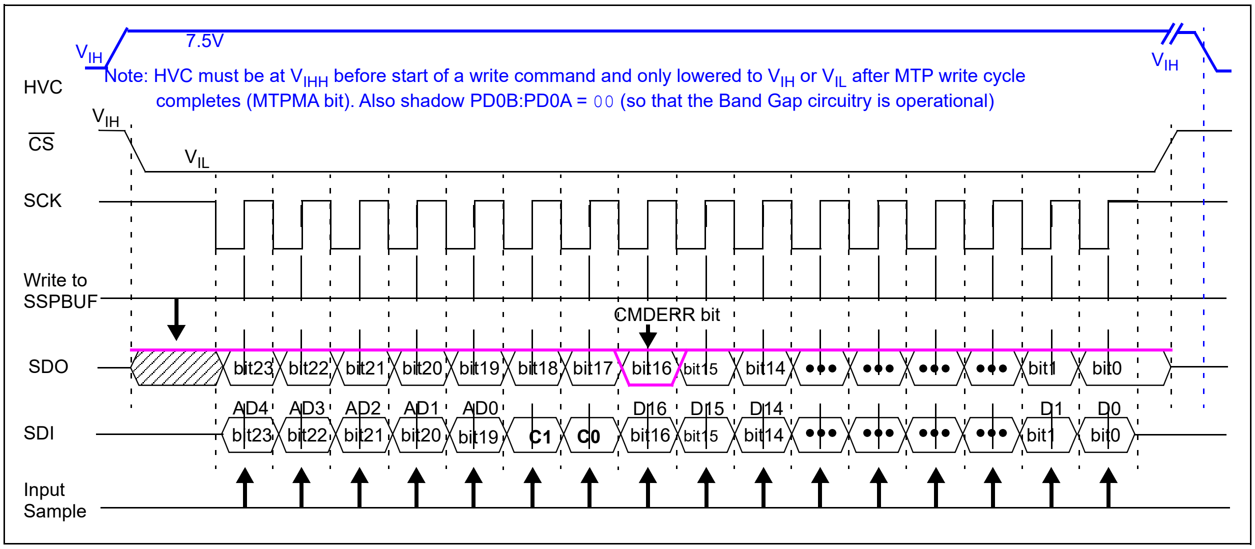
In SPI Mode `1,1`:

- SCK idle state = High (V_{IH})
- Data are clocked in on the SDI pin on the rising edge of SCK
- Data are clocked out on the SDO pin on the falling edge of SCK



Note: HVC must be at V_{IHH} before start of a write command and only lowered to V_{IH} or V_{IL} after MTP write cycle completes (MTPMA bit). Also shadow PD0B:PD0A = `00` (so that the band gap circuitry is operational)

FIGURE 6-2: *24-Bit Commands (Write, Read) – SPI Waveform (Mode `0,0`).*



Note: HVC must be at V_{IHH} before start of a write command and only lowered to V_{IH} or V_{IL} after MTP write cycle completes (MTPMA bit). Also shadow PD0B:PD0A = `00` (so that the Band Gap circuitry is operational)

FIGURE 6-3: *24-Bit Commands (Write, Read) – SPI Waveform (Mode `1,1`).*

NOTES:

7.0 DEVICE COMMANDS

The MCP48CXDX1/2's SPI command format supports 32 memory address locations and two commands. The command may have two modes:

- Normal Serial Commands
- MTP Programming (HV) Serial Commands

Normal Serial commands are those where the HVC pin is driven to either V_{IH} or V_{IL}. With High-Voltage Serial commands, the HVC pin is driven to 7.5V. These commands are shown in Table 7-1.

Table 7-2 shows an overview of all the SPI commands and their interaction with other device features.

The 24-bit commands (**Read Command** and **Write Command**) contain a Command byte and a Data Word. The Command byte contains one reserved bit, see Figure 7-1.

TABLE 7-1: COMMAND BITS OVERVIEW

Bit States C1:C0	Command	# of Bits	Normal or HV
11	Read Data	24-Bits	Normal only(1)
00	Write Data	24-Bits	Both
01	Reserved	—	—
10	Reserved	—	—

Note 1: Reading from the NV memory locations will return the shadow RAM value of the NV memory, not the NV memory contents. Once a write cycle starts, no other commands accessing NV memory locations are allowed.

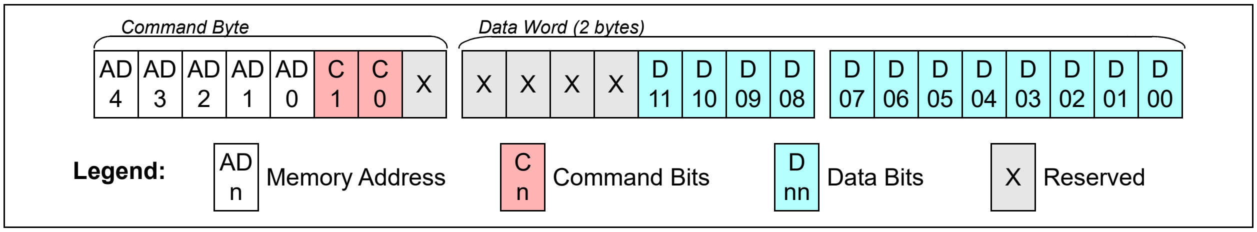


FIGURE 7-1: 24-bit SPI Command Format.

TABLE 7-2: SPI COMMANDS – NUMBER OF CLOCKS

Command					# of Bit Clocks(2)	Data Update Rate (8-bit/10-bit/12-bit) (Data Words/Second)			Comments
Operation	Code			Mode(1)					
	C1	C0	HV (4, 7)			1 MHz	10 MHz	50 MHz	
Write Command(3, 6)	0	0	Y	Single	24	41,666	416,666	2,083,333	—
	0	0	N	Continuous	24 * n	41,666	416,666	2,083,333	For 10 data words
Read Command(5)	1	1	N	Random	24	41,666	416,666	2,083,333	—
	1	1	N	Continuous	24 * n	41,666	416,666	2,083,333	For 10 data words

Note 1: Nonvolatile registers can only use the Single mode.

2: "n" indicates the number of times the command operation is to be repeated.

3: The registers are updated after the 24th clock bit or after the $\overline{CS}$ rising, depending on mode.

4: If the state of the HVC pin is V_{IHH}, the command is ignored, but a Command Error condition (CMDERR) will NOT be generated.

5: This command is useful to determine when an MTP programming cycle is complete.

6: This command can be either normal voltage or high voltage.

7: The MTP write cycle starts after the $\overline{CS}$ rising edge. A high-voltage command requires the HVC pin to be at V_{IHH} for the entire command, until the completion of the MTP write cycle.

7.1 Command Byte

The Command byte has three fields, the Address (5 bits), the Command (2 bits) and one Reserved bit (see Figure 7-1).

The device memory is accessed when the Host sends a proper Command byte to select the desired operation. The memory location getting accessed is contained in the Command byte's AD4:AD0 bits. The action desired is contained in the Command byte's C1:C0 bits, see Figure 7-5. C1:C0 determines if the desired memory location will be read or written.

As the Command byte is loaded into the device (on the SDI pin), the device's SDO pin drives. The SDO pin will output high bits for the first seven bits of that command. On the 8th bit, the SDO pin will output the CMDERR bit state.

7.2 Data Bytes

The read and write commands use Data bytes, see Figure 7-1. The D16 bit is currently unused and corresponds to the position on the SDO data of the CMDERR bit.

7.3 Error Condition

The CMDERR bit indicates if the five address bits received (AD4:AD0) and the two command bits received (C1:C0) are a valid combination. The CMDERR bit is high if the combination is valid and low if the combination is invalid.

The command error bit will also be low if a write to a nonvolatile address is specified and another SPI command occurs before the $\overline{\text{CS}}$ pin is driven inactive (V_{IH}).

SPI commands that do not have a multiple of 24 clocks are ignored.

Once an error condition has occurred, any following commands are ignored. All following SDO bits will be low until the CMDERR condition is cleared by forcing the $\overline{\text{CS}}$ pin to the Inactive state (V_{IH}) or doing a POR.

7.3.1 ABORTING A TRANSMISSION

All SPI transmissions must have the correct number of SCK pulses to be executed. The command is not executed until the complete number of clocks are received. Some commands also require the $\overline{\text{CS}}$ pin to be forced inactive (V_{IH}). If the $\overline{\text{CS}}$ pin is forced to the Inactive state (V_{IH}), the serial interface is reset. Partial commands are not executed.

SPI is more susceptible to noise than other bus protocols. The most likely case is that this noise corrupts the value of the data being clocked into the MCP48CXDX1/2 or the SCK pin is injected with extra clock pulses. This may cause data to be corrupted in the device or a command error to occur because the address and command bits were not a valid combination. The extra SCK pulse will also cause the SPI data (SDI) and clock (SCK) to be out of sync. Forcing the $\overline{\text{CS}}$ pin to the Inactive state (V_{IH}) resets the serial interface. The SPI interface will ignore activity on the SDI and SCK pins until the $\overline{\text{CS}}$ pin transition to the active state is detected (V_{IH} to V_{IL}).

Note 1: When the MCP48CXDX1/2 does not receive data, it is recommended that the $\overline{\text{CS}}$ pin be forced to the inactive level (V_{IL}).

7.4 Continuous Commands

The device supports the ability to execute commands continuously. While the $\overline{\text{CS}}$ pin is in Active state (V_{IL}), any sequence of valid commands may be received.

The following example is a valid sequence of events:

1. $\overline{\text{CS}}$ pin driven active (V_{IL})
2. Read command
3. Write command (volatile memory)
4. Write command (nonvolatile memory)
5. $\overline{\text{CS}}$ pin driven inactive (V_{IH})

Note 1: While the $\overline{\text{CS}}$ pin is active, only one type of command must be issued. When changing commands, it is recommended that the $\overline{\text{CS}}$ pin be made inactive, then forced back to the active state.

2: Long command strings must be broken down into shorter command strings. This reduces the probability of noise on the SCK pin corrupting the desired SPI command string.

7.5 Write Command

The write command is a 24-bit command. The write command can be issued to both the volatile and nonvolatile memory locations. The format of the command is shown in Figure 7-2.

A write command to a volatile memory location changes that location after a properly formatted write command (24-clock) is received.

A write command to a nonvolatile memory location will only start a write cycle after a properly formatted write command (24-clock) is received and the $\overline{\text{CS}}$ pin transitions to the Inactive state (V_{IH}).

Note: Writes to volatile memory locations depend on the state of the WiperLock™ Technology bits.

7.5.1 SINGLE WRITE TO VOLATILE MEMORY

The write operation requires that the $\overline{\text{CS}}$ pin be in the Active state (V_{IL}). Typically, the $\overline{\text{CS}}$ pin is in the Inactive state (V_{IH}) and is driven to the Active state (V_{IL}). The 24-bit write command (Command byte and Data bytes) is, then, clocked in on the SCK and SDI pins. Once all 24 bits are received, the specified volatile address is updated. A write will not occur if the write command is not exactly 24 clock pulses. This prevents system issues from corrupting the nonvolatile memory locations.

Figure 7-2 shows the waveform for a single write.

7.5.2 SINGLE WRITE TO NONVOLATILE MEMORY

The sequence to write to a single nonvolatile memory location is the same as a single write to volatile memory with the exception that before the command, the HVC pin must be driven to V_{IHH}. After the command, the $\overline{\text{CS}}$ pin is driven inactive (V_{IH}), which then starts the MTP write cycle (t_{wc}). The HVC pin must remain at the V_{IHH} level until the completion of the MTP write cycle.

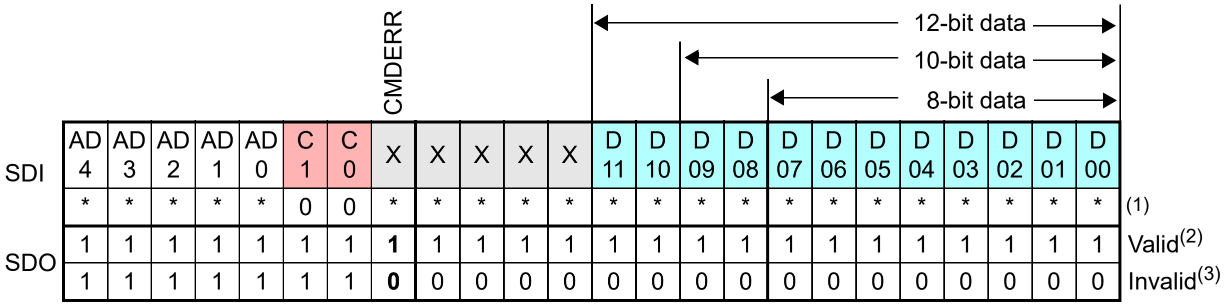
A write cycle will not start if the write command is not exactly 24 clock pulses. This protects against system issues from corrupting the nonvolatile memory locations.

After the $\overline{\text{CS}}$ pin is driven inactive (V_{IH}), the serial interface may immediately be re-enabled by driving the $\overline{\text{CS}}$ pin to the Active state (V_{IL}).

During an MTP write cycle, only serial commands to volatile memory are accepted. All other serial commands are ignored until the MTP write cycle (t_{wc}) is completed. The MTPMA bit in the Status register indicates the status of an MTP write cycle.

Once a write command to a nonvolatile memory location is received, no other SPI commands can be received before the $\overline{\text{CS}}$ pin transitions to the Inactive state (V_{IH}) or a CMDERR on the current SPI command occurs.

The write to a nonvolatile memory command has the same format as the write to a volatile memory command (see the figure below).



								CMDERR																	
SDI	AD 4	AD 3	AD 2	AD 1	AD 0	C 1	C 0	X	X	X	X	X	D 11	D 10	D 09	D 08	D 07	D 06	D 05	D 04	D 03	D 02	D 01	D 00	
	*	*	*	*	*	0	0	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	(1)
SDO	1	1	1	1	1	1	1	**1**	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	Valid$^{(2)}$
	1	1	1	1	1	1	1	**0**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Invalid$^{(3)}$

Note 1: For write commands addressing the DAC Wiper registers, the Data bits depend on the resolution of the device: 12-bit = D11:D00, 10-bit = D09:D00 and 8-bit = D07:D00.
Data are right justified for easy Host Controller operation (no data manipulation before transmitting the desired value). The unimplemented bits are ignored.

2: After a valid memory address and a write Command byte are received (CMDERR = `1`), all the following SDO bits will be output as ‘`1`’.

3: If an Error condition occurs (CMDERR = `0`), all the following SDO bits will be output as ‘`0`’ until the CMDERR condition is cleared (the $\overline{\text{CS}}$ pin is forced to the Inactive state).

FIGURE 7-2: *Write Single Memory Location Command – SDI and SDO States.*

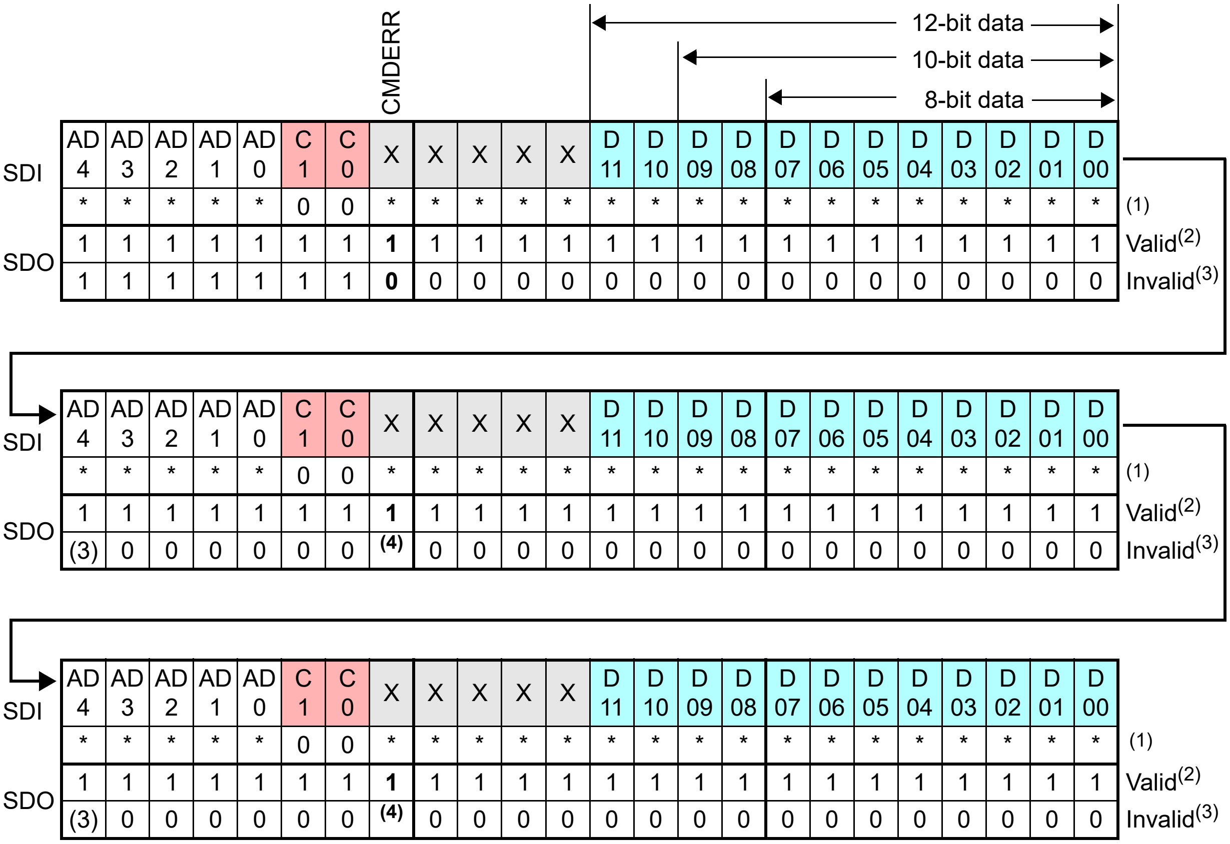
7.5.3 CONTINUOUS WRITES TO VOLATILE MEMORY

Continuous writes are possible only when writing to the volatile memory registers.

The figure below shows the sequence for three continuous writes. The writes do not need to be to the same volatile memory address.

7.5.4 CONTINUOUS WRITES TO NONVOLATILE MEMORY

Continuous writes to nonvolatile memory are not allowed, and attempts to do so will result in a CMDERR condition.



SDI	AD 4	AD 3	AD 2	AD 1	AD 0	C 1	C 0	X	X	X	X	X	D 11	D 10	D 09	D 08	D 07	D 06	D 05	D 04	D 03	D 02	D 01	D 00	
	*	*	*	*	*	0	0	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	(1)
SDO	1	1	1	1	1	1	1	**1**	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	Valid$^{(2)}$
	1	1	1	1	1	1	1	**0**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Invalid$^{(3)}$

SDI	AD 4	AD 3	AD 2	AD 1	AD 0	C 1	C 0	X	X	X	X	X	D 11	D 10	D 09	D 08	D 07	D 06	D 05	D 04	D 03	D 02	D 01	D 00	
	*	*	*	*	*	0	0	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	(1)
SDO	1	1	1	1	1	1	1	**1**	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	Valid$^{(2)}$
	(3)	0	0	0	0	0	0	**(4)**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Invalid$^{(3)}$

SDI	AD 4	AD 3	AD 2	AD 1	AD 0	C 1	C 0	X	X	X	X	X	D 11	D 10	D 09	D 08	D 07	D 06	D 05	D 04	D 03	D 02	D 01	D 00	
	*	*	*	*	*	0	0	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	(1)
SDO	1	1	1	1	1	1	1	**1**	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	Valid$^{(2)}$
	(3)	0	0	0	0	0	0	**(4)**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Invalid$^{(3)}$

Note 1: For write commands addressing the DAC Wiper registers, the Data bits depend on the resolution of the device: 12-bit = D11:D00, 10-bit = D09:D00 and 8-bit = D07:D00.
Data are right justified for easy Host Controller operation (no data manipulation before transmitting the desired value). The unimplemented bits are ignored.

2: After a valid memory address and a write Command byte are received (CMDERR = `1`), all the following SDO bits will be output as ‘`1`’.

3: If an Error condition occurs (CMDERR = `0`), all the following SDO bits will be output as ‘`0`’ until the CMDERR condition is cleared (the $\overline{\text{CS}}$ pin is forced to the Inactive state).

4: This CMDERR bit will be forced to ‘`0`’, regardless if this Address + Command combination is valid. This command will not be completed and requires the $\overline{\text{CS}}$ pin to return to V_{IH} to clear the CMDERR condition.

FIGURE 7-3: *Continuous Write Sequence (Volatile Memory Only).*

7.6 Read Command

The read command is a 24-bit command. The read command can be issued to both the volatile and nonvolatile memory locations. The format of the command is shown in the figure below.

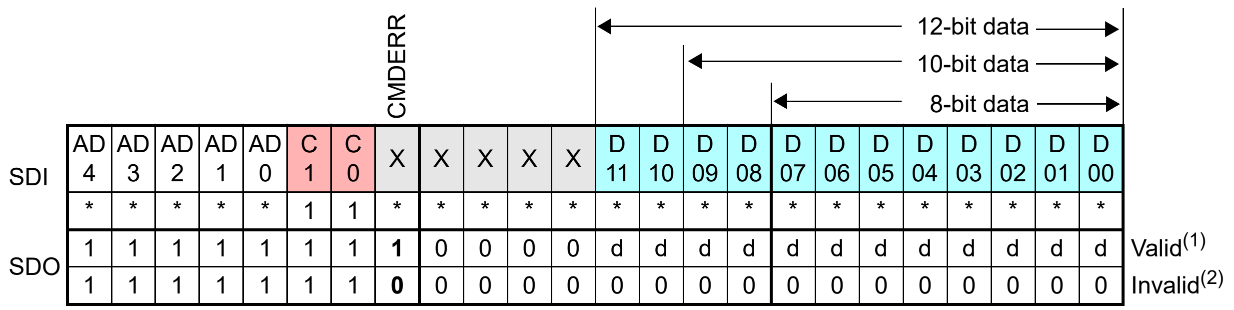
The first seven bits of the read command determine the address and the command. The 8th clock will output the CMDERR bit on the SDO pin. For the remaining 16 clocks, the device will transmit the data bits of the specified address (AD4:AD0).

The figure below shows the SDI and SDO information for a read command.

During an MTP write cycle, the read command can only be issued to the volatile memory locations. By reading the Status register, the Host Controller can determine when the write cycle is completed (via the state of the MTPMA bit).

7.6.1 SINGLE READ

The read operation requires that the $\overline{\text{CS}}$ pin be in the Active state (V_{IL}). Typically, the $\overline{\text{CS}}$ pin will be in the Inactive state (V_{IH}) and is driven to the Active state (V_{IL}). The 24-bit read command (Command byte and Data Word) is then clocked in on the SCK and $\overline{\text{SDI}}$ pins. The SDO pin starts driving high (V_{IH}) when the $\overline{\text{CS}}$ goes active and starts driving data on the 8th bit (CMDERR bit); the addressed data come out on the 9th through 24th clocks.



SDI	AD 4	AD 3	AD 2	AD 1	AD 0	C 1	C 0	X	X	X	X	X	D 11	D 10	D 09	D 08	D 07	D 06	D 05	D 04	D 03	D 02	D 01	D 00	
	*	*	*	*	*	1	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	
SDO	1	1	1	1	1	1	1	**1**	0	0	0	0	d	d	d	d	d	d	d	d	d	d	d	d	Valid$^{(1)}$
	1	1	1	1	1	1	1	**0**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Invalid$^{(2)}$

Note 1: The Data bits depend on the resolution of the device: 12-bit = D11:D00, 10-bit = D09:D00 and 8-bit = D07:D00.
The unimplemented bits are output as '0' and data are right justified for easy Host Controller operation (no data manipulation after reading the register value).

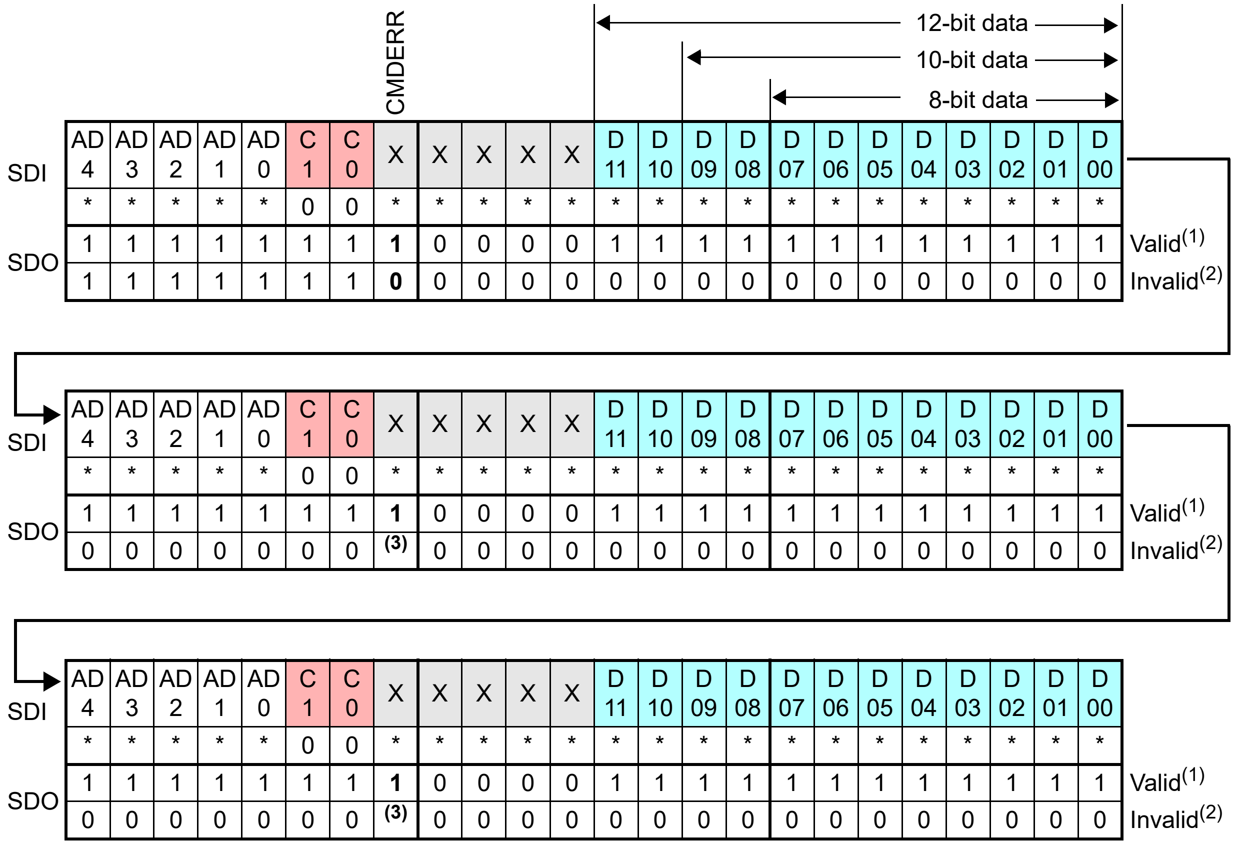
2: If an Error condition occurs (CMDERR = 0), all the following SDO bits will be output as '0' until the CMDERR condition is cleared (the $\overline{\text{CS}}$ pin is forced to the Inactive state).

FIGURE 7-4: *Read Single Memory Location Command – SDI and SDO States.*

7.6.2 CONTINUOUS READS

Continuous reads allow the device's memory to be read quickly. Continuous reads are possible to all memory locations. Read commands may only access volatile memory locations during an MTP write cycle.

The figure below shows the sequence for three continuous reads. The reads do not need to be to the same memory address.



	AD4	AD3	AD2	AD1	AD0	C1	C0	X	X	X	X	X	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	
SDI	*	*	*	*	*	0	0	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	
SDO	1	1	1	1	1	1	1	**1**	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	Valid(1)
	1	1	1	1	1	1	1	**0**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Invalid(2)

	AD4	AD3	AD2	AD1	AD0	C1	C0	X	X	X	X	X	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	
SDI	*	*	*	*	*	0	0	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	
SDO	1	1	1	1	1	1	1	**1**	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	Valid(1)
	0	0	0	0	0	0	0	**(3)**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Invalid(2)

	AD4	AD3	AD2	AD1	AD0	C1	C0	X	X	X	X	X	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	
SDI	*	*	*	*	*	0	0	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	
SDO	1	1	1	1	1	1	1	**1**	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	Valid(1)
	0	0	0	0	0	0	0	**(3)**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Invalid(2)

Note 1: The Data bits depend on the resolution of the device: 12-bit = D11:D00, 10-bit = D09:D00 and 8-bit = D07:D00. The unimplemented bits are output as '`0`' and data are right justified for easy Host Controller operation (no data manipulation after reading the register value).

2: If an Error condition occurs (CMDERR = `0`), all the following SDO bits will be output as '`0`' until the CMDERR condition is cleared (the $\overline{CS}$ pin is forced to the Inactive state).

3: This CMDERR bit will be forced to '`0`', regardless if this Address + Command combination is valid. This command will not be completed and requires the $\overline{CS}$ pin to return to V_{IH} to clear the CMDERR condition.

FIGURE 7-5: *Continuous Read Sequence.*

8.0 TYPICAL APPLICATIONS

The MCP48CXDX1/2 devices are general purpose, single/dual channel voltage output DACs for various applications where a precision operation with low power is needed.

Applications generally suited for the devices are:

- Set Point or Offset Trimming
- Sensor Calibration
- Portable Instrumentation (Battery-Powered)
- Motor Control

8.1 Design Considerations

In the design of a system with the MCP48CXDX1/2 devices, the following considerations must be taken into account:

- **Power Supply Considerations**
- **Layout Considerations**

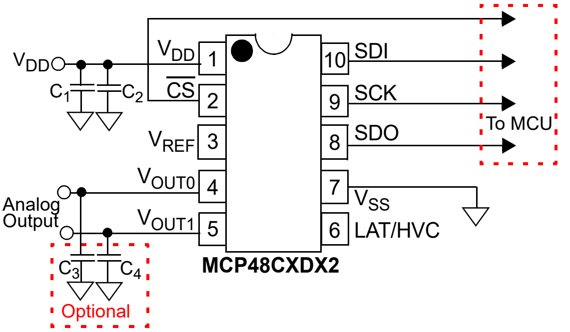
8.1.1 POWER SUPPLY CONSIDERATIONS

The power source supplying these devices must be as clean as possible. If the application circuit has separate digital and analog power supplies, V_{DD} and V_{SS} may reside on the analog plane.

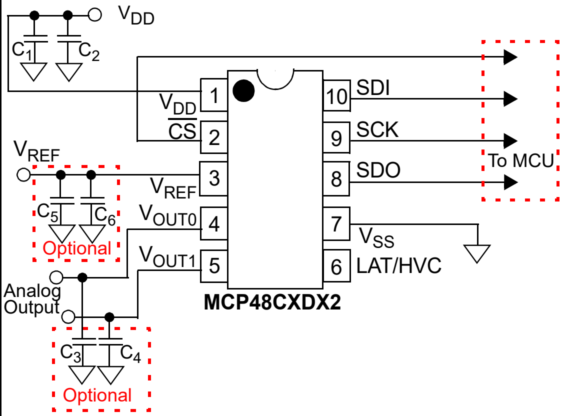
The power supply to the device is also used for the DAC voltage reference internally if the internal V_{DD} is selected as the resistor ladder's reference voltage.

The typical application requires a bypass capacitor in order to filter high-frequency noise, which can be induced onto the power supply's traces. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity.

Any noise induced on the V_{DD} line can affect the DAC performance. Typical applications require a bypass capacitor in order to filter out high-frequency noise on the V_{DD} line. The noise can be induced onto the power supply's traces or as a result of changes on the DAC output. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. The figure below shows an example of using two bypass capacitors (a 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor) in parallel on the V_{DD} line. These capacitors must be placed as close to the V_{DD} pin as possible (within 4 mm). If the application circuit has separate digital and analog power supplies, the V_{DD} and V_{SS} pins of the device must reside on the analog plane.



(a) Circuit when V_{DD} is selected as reference.
(Note: V_{DD} is connected to the reference circuit internally.)



(b) Circuit when external reference is used.

C_1:	0.1 µF capacitor	=	Ceramic
C_2:	10 µF capacitor	=	Tantalum (optional)
C_3:	~ 0.1 µF	=	Optional to reduce noise in the V_{OUT} pin
C_4:	0.1 µF capacitor	=	Ceramic
C_5:	10 µF capacitor	=	Tantalum
C_6:	0.1 µF capacitor	=	Ceramic

FIGURE 8-1: *Example Circuit.*

8.1.2 LAYOUT CONSIDERATIONS

Several layout considerations may be applicable to your application. These may include:

- **Noise**
- **PCB Area Requirements**

8.1.2.1 Noise

Inductively-coupled AC transients and digital switching noise can degrade the input and output signal integrity, potentially masking the MCP48CXDX1/2's performance. Careful board layout minimizes these effects and increases the Signal-to-Noise Ratio (SNR). Multi-layer boards utilizing a low-inductance ground plane, isolated inputs, isolated outputs and proper decoupling are critical to achieving the performance that the silicon is capable of providing. Particularly harsh environments may require shielding of critical signals.

Separate digital and analog ground planes are recommended. In this case, the V_{SS} pin and the ground pins of the V_{DD} capacitors must be terminated to the analog ground plane.

Note: Breadboards and wire-wrapped boards are not recommended.

8.1.2.2 PCB Area Requirements

In some applications, PCB area is a criteria for device selection. The table below shows the typical package dimensions and area for the different package options.

TABLE 8-1: PACKAGE FOOTPRINT[1]

Package			Package Footprint		
Pins	Type	Code	Dimensions (mm)		Area (mm^2)
			Length	Width	
10	MSOP	UN	3.00	4.90	14.70
10	DFN	MF	3.00	3.00	9.00
16	QFN	MG	3.00	3.00	9.00

Note 1: Does not include recommended land pattern dimensions. Dimensions are typical values.

8.2 Application Examples

The MCP48CXDX1/2 devices are rail-to-rail output DACs designed to operate with a V_{DD} range of 2.7V to 5.5V. The internal output amplifier is robust enough to drive common, small-signal loads directly, thus eliminating the cost and size of the external buffers for most applications. The user can select the gain of 1 or 2 of the output op amp by setting the Configuration register bits. The internal V_{DD} or an external reference can be used. There are various user options and easy-to-use features that make the devices suitable for various modern DAC applications.

Application examples include:

- Decreasing Output Step Size
- Building a "Window" DAC
- Bipolar Operation
- Selectable Gain and Offset Bipolar Voltage Output
- Designing a Double-Precision DAC
- Building Programmable Current Source
- Serial Interface Communication Times
- Development Support
- Power Supply Considerations
- Layout Considerations

8.2.1 DC SET POINT OR CALIBRATION

A common application for the devices is a digitally-controlled set point and/or calibration of variable parameters, such as sensor offset or slope. For example, the MCP48CVD2X provides 4096 output steps. If voltage reference is 4.096V (where GX = `0`), the LSb size is 1 mV. If a smaller output step size is desired, a lower external voltage reference is needed.

8.2.1.1 Decreasing Output Step Size

If the application calibrates the bias voltage of a diode or transistor, a bias voltage range of 0.8V may be desired with about 200 µV resolution per step. Two common methods to achieve a small step size are to use a lower V_{REF} pin voltage or a voltage divider on the DAC's output.

Using an external voltage reference (V_{REF}) is an option if the external reference is available with the desired output voltage range. However, when using a low-voltage reference voltage, occasionally the noise floor causes an SNR error that is intolerable. Using a voltage divider method is another option and provides some advantages when the external voltage reference needs to be very low, or when the desired output voltage is not available. In this case, a larger value reference voltage is used, while two resistors scale the output range down to the precise desired level.

The figure below illustrates this concept. A bypass capacitor on the output of the voltage divider plays a critical function in attenuating the output noise of the DAC and the induced noise from the environment.

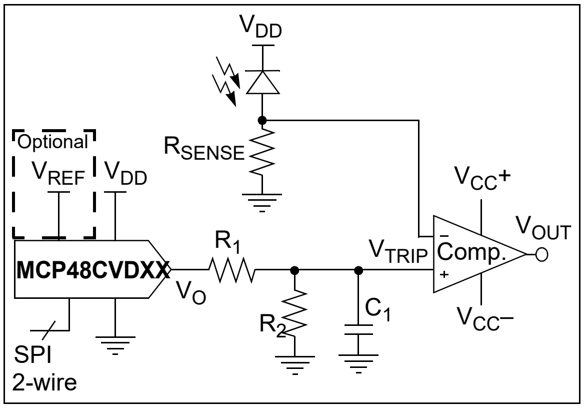


FIGURE 8-2: *Example Circuit Of Set Point or Threshold Calibration.*

EQUATION 8-1: V_{OUT} AND V_{TRIP} CALCULATIONS

$$V_{OUT} = V_{REF} \bullet G \bullet \frac{DAC\ Register\ Value}{2^N}$$

$$V_{trip} = V_{OUT}\left(\frac{R_2}{R_1 + R_2}\right)$$

8.2.1.2 Building a "Window" DAC

When calibrating a set point or threshold of a sensor, typically only a small portion of the DAC output range is utilized. If the LSb size is adequate enough to meet the application's accuracy needs, the unused range is sacrificed without consequences. If greater accuracy is needed, the output range will need to be reduced to increase the resolution around the desired threshold.

If the threshold is not near V_{REF}, 2 • V_{REF} or V_{SS}, then creating a "window" around the threshold has several advantages. One simple method to create this "window" is to use a voltage divider network with a pull-up and pull-down resistor. The figure below and Figure 8-5 illustrate this concept.

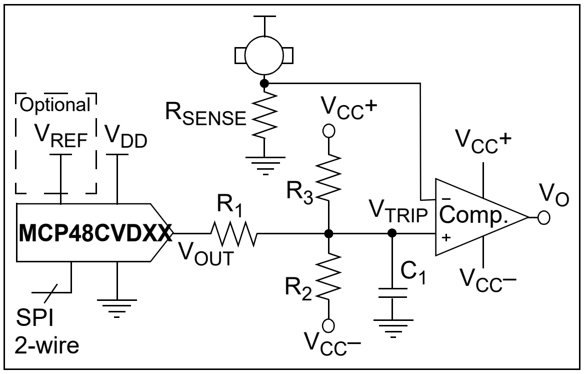


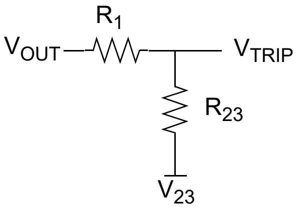
FIGURE 8-3: *Single Supply "Window" DAC.*

EQUATION 8-2: V_{OUT} AND V_{TRIP} CALCULATIONS

$$V_{OUT} = V_{REF} \bullet G \bullet \frac{DAC\ Register\ Value}{2^N}$$

$$V_{TRIP} = \frac{V_{OUT}R_{23} + V_{23}R_1}{R_1 + R_{23}}$$

$$\text{Thevenin Equivalent}\left\{\begin{array}{l} R_{23} = \dfrac{R_2 R_3}{R_2 + R_3} \\[2ex] V_{23} = \dfrac{(V_{CC+}R_2) + (V_{CC-}R_3)}{R_2 + R_3} \end{array}\right.$$



8.3 Bipolar Operation

Bipolar operation is achievable by utilizing an external operational amplifier. This configuration is desirable due to the wide variety and availability of op amps. This allows a general purpose DAC, with its cost and availability advantages, to meet almost any desired output voltage range, power and noise performance.

The figure below illustrates a simple bipolar voltage source configuration. R_1 and R_2 allow the gain to be selected, while R_3 and R_4 shift the DAC's output to a selected offset. Note that R4 can be tied to V_{DD} instead of V_{SS} if a higher offset is desired.

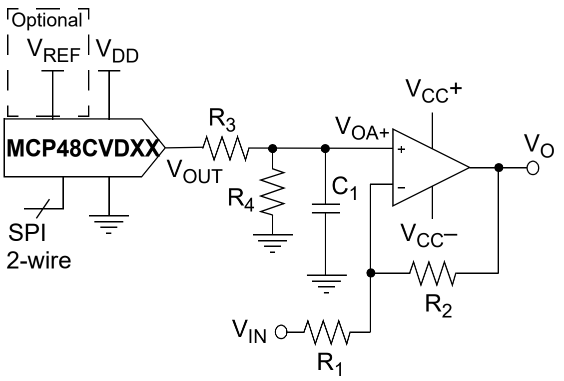


FIGURE 8-4: *Digitally-Controlled Bipolar Voltage Source Example Circuit.*

EQUATION 8-3: V_{OUT}, V_{OA+} AND V_O CALCULATIONS

$$V_{OUT} = V_{REF} \bullet G \bullet \frac{DAC\ Register\ Value}{2^N}$$

$$V_{OA+} = \frac{V_{OUT} \bullet R_4}{R_3 + R_4}$$

$$V_O = V_{OA+} \bullet \left(1 + \frac{R_2}{R_1}\right) - V_{DD} \bullet \left(\frac{R_2}{R_1}\right)$$

8.4 Selectable Gain and Offset Bipolar Voltage Output

In some applications, precision digital control of the output range is desirable. Figure 8-5 illustrates how to use the DAC devices to achieve this in a bipolar or single supply application.

This circuit is typically used for linearizing a sensor whose slope and offset vary.

The equation to design a bipolar “window” DAC is utilized if R_3, R_4 and R_5 are populated.

8.4.1 BIPOLAR DAC EXAMPLE

An output step size of 1 mV, with an output range of ±2.05V, is desired for a particular application.

Step 1: Calculate the range: +2.05V – (-2.05V) = 4.1V

Step 2: Calculate the resolution needed:

4.1V/1 mV = 4100

2^{12} = 4096; therefore, 12-bit resolution is desired.

Step 3: The amplifier gain (R_2/R_1), multiplied by full-scale V_{OUT} (4.096V), must be equal to the desired minimum output to achieve bipolar operation. Any gain can be realized by choosing resistor values ($R_1 + R_2$); therefore, the V_{REF} value must be selected first. If a V_{REF} of 4.096V is used, solve the amplifier's gain by setting the DAC to 0, knowing that the output needs to be -2.05V.

The equation can be simplified to:

EQUATION 8-4:

$$\frac{-R_2}{R_1} = \frac{-2.05}{4.096V} \qquad \frac{R_2}{R_1} = \frac{1}{2}$$

If R_1 = 20 kΩ and R_2 = 10 kΩ, the gain will be 0.5.

Step 4: Next, solve for R_3 and R_4 by setting the DAC to 4096, knowing that the output needs to be +2.05V.

EQUATION 8-5:

$$\frac{R_4}{(R_3 + R_4)} = \frac{2.05V + (0.5 \cdot 4.096V)}{1.5 \cdot 4.096V} = \frac{2}{3}$$

If R_4 = 20 kΩ, then R_3 = 10 kΩ

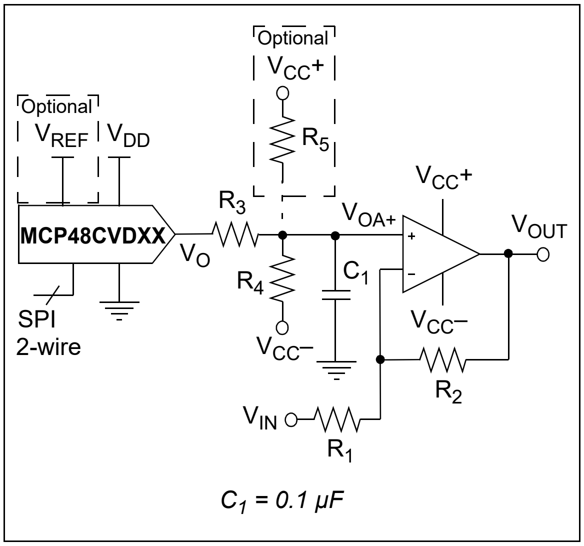


FIGURE 8-5: *Bipolar Voltage Source with Selectable Gain and Offset.*

EQUATION 8-6: V_{OUT}, V_{OA+} AND V_O CALCULATIONS

$$V_{OUT} = V_{REF} \bullet G \bullet \frac{DAC\ Register\ Value}{2^N}$$

$$V_{OA+} = \frac{V_{OUT} \bullet R_4 + V_{CC-} \bullet R_5}{R_3 + R_4}$$

$$V_O = \underbrace{V_{OA+} \bullet \left(1 + \frac{R_2}{R_1}\right)}_{\text{Offset Adjust}} - \underbrace{V_{IN} \bullet \left(\frac{R_2}{R_1}\right)}_{\text{Gain Adjust}}$$

EQUATION 8-7: BIPOLAR "WINDOW" DAC USING R_4 AND R_5

$$\text{Thevenin Equivalent} \left\{ V_{45} = \frac{V_{CC+}R_4 + V_{CC-}R_5}{R_4 + R_5} \right.$$

$$V_{IN+} = \frac{V_{OUT}R_{45} + V_{45}R_3}{R_3 + R_{45}}$$

$$R_{45} = \frac{R_4 R_5}{R_4 + R_5}$$

$$V_O = \underbrace{V_{IN+}\left(1 + \frac{R_2}{R_1}\right)}_{\text{Offset Adjust}} - \underbrace{V_A\left(\frac{R_2}{R_1}\right)}_{\text{Gain Adjust}}$$

8.5 Designing a Double-Precision DAC

The figure below shows an example design of a single supply voltage output capable of up to a 24-bit resolution. This requires two 12-bit DACs. This design is simply a voltage divider with a buffered output.

As an example, if a similar application to the one developed in **Section 8.4.1 "Bipolar DAC Example"** required a resolution of 1 µV, instead of 1 mV, and a range of 0V to 4.1V, then a 12-bit resolution would not be adequate.

Step 1: Calculate the resolution needed:
4.1V/1 µV = 4.1 x 10^6
2^{22} = 4.2 x 10^6; therefore, a 22-bit resolution is desired. DNL = ±1.0 LSb; therefore, this design can be attempted with the 12-bit DAC.

Step 2: DAC1's V_{OUT1} has a resolution of 1 mV; therefore, its output only needs to be "pulled" 1/1000 to meet the 1 µV target. Dividing V_{OUT0} by 1000 would allow the application to compensate for DAC1's DNL error.

Step 3: If R_2 is 100Ω, then R_1 needs to be 100 kΩ.

Step 4: The resulting transfer function is shown in Equation 8-8.

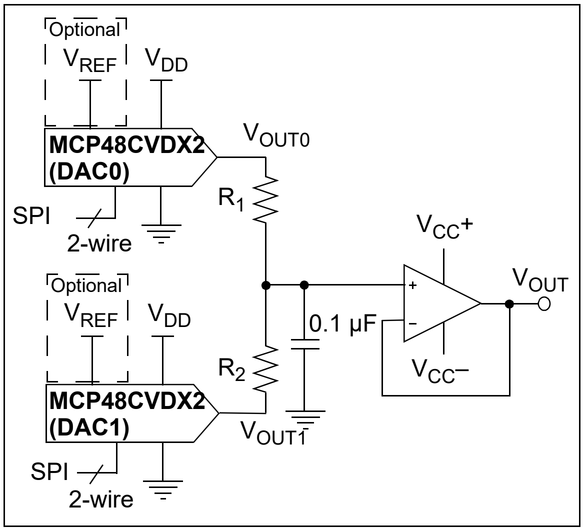


FIGURE 8-6: *Simple Double Precision DAC Using MCP48CVDX2.*

EQUATION 8-8: V_{OUT} CALCULATION

$$V_{OUT} = \frac{V_{OUT0} * R_2 + V_{OUT1} * R_1}{R_1 + R_2}$$

Where:

V_{OUT0} = (V_{REF} ∗ G ∗ DAC0 register value)/4096

V_{OUT1} = (V_{REF} ∗ G ∗ DAC1 register value)/4096

GX = Selected Op Amp Gain

8.6 Building Programmable Current Source

The figure below shows an example of building a programmable current source using a voltage follower. The current sensor resistor is used to convert the DAC voltage output into a digitally-selectable current source.

The smaller R_{SENSE} is, the less power is dissipated across it. However, this also reduces the resolution that the current can be controlled at.

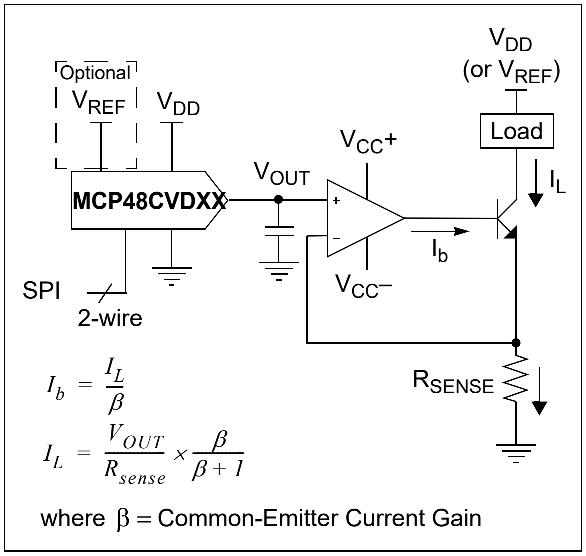


FIGURE 8-7: *Digitally-Controlled Current Source.*

8.7 Serial Interface Communication Times

Table 7-2 shows the time/frequency of the supported operations of the SPI serial interface for the different serial interface operational frequencies. This, along with the V_{OUT} output performance (such as slew rate), would be used to determine your application's volatile DAC register update rate.

9.0 DEVELOPMENT SUPPORT

Development support can be classified into two groups:

- Development Tools
- Technical Documentation

9.1 Development Tools

Several development tools are available to assist in the design and evaluation of the MCP48CXDX1/2 devices. The currently available tools display in the table below.

Figure 9-1 shows how the ADM00309 bond-out PCB can be populated to easily evaluate the MCP48CXDX1/2 devices. Device evaluation can use the PICkit™ Serial Analyzer to control the DAC output registers and state of the Configuration, Control and Status registers.

The ADM00309 boards may be purchased directly from the Microchip website at www.microchip.com.

9.2 Technical Documentation

Several additional technical documents for design and development are available. These technical documents include Application Notes, Technical Briefs and Design Guides. Table 9-2 lists some of these documents.

TABLE 9-1: DEVELOPMENT TOOLS (Note 1)

Board Name	Part #	Comment
MSOP-8 and MSOP-10 Evaluation Board	ADM00309	The MSOP-10 and MSOP-8 Evaluation Board is a bond-out board that allows the system designer to quickly evaluate the operation of Microchip Technology’s devices in any of the following packages: • MSOP (8/10-pin) • DIP (10-pin)

Note 1: Supports the PICkit™ Serial Analyzer. See the User’s Guide for additional information and requirements.

TABLE 9-2: TECHNICAL DOCUMENTATION

Application Note Number	Title	Literature #
AN1326	Using the MCP4728 12-Bit DAC for LDMOS Amplifier Bias Control Applications	DS01326
—	Signal Chain Design Guide	DS21825
—	Analog Solutions for Automotive Applications Design Guide	DS01005

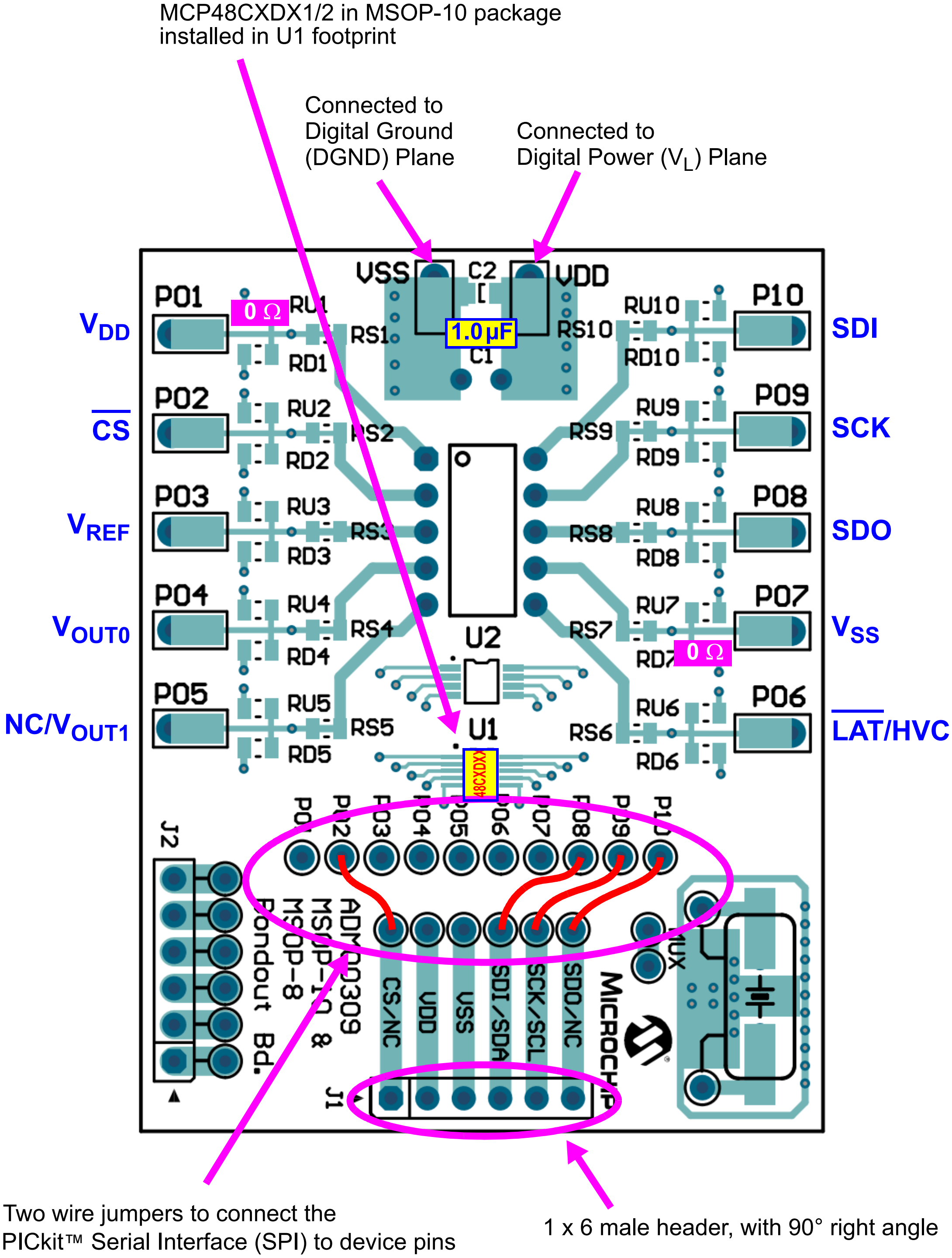
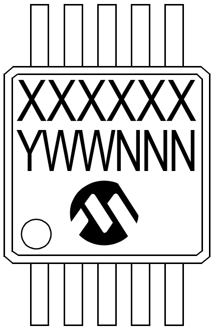


FIGURE 9-1: MCP48CXDX1/2 Evaluation Board Circuit Using ADM00309.

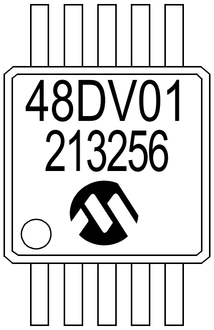
10.0 PACKAGING INFORMATION

10.1 Package Marking Information

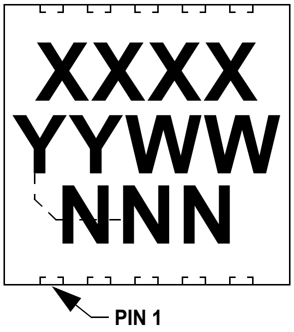
10-Lead MSOP



Example



10-Lead DFN (3 x 3 mm)



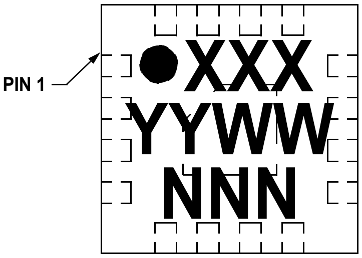
Part Number	Code
MCP48CVD01-E/MF	DAKH
MCP48CVD11-E/MF	DAKL
MCP48CVD21-E/MF	DAKN
MCP48CVD02-E/MF	DAKJ
MCP48CVD12-E/MF	DAKM
MCP48CVD22-E/MF	DAKP
MCP48CMD01-E/MF	DAKD
MCP48CMD11-E/MF	DAKD
MCP48CMD21-E/MF	DAKF
MCP48CMD02-E/MF	DAKC
MCP48CMD12-E/MF	DAKE
MCP48CMD22-E/MF	DAKG

Example

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

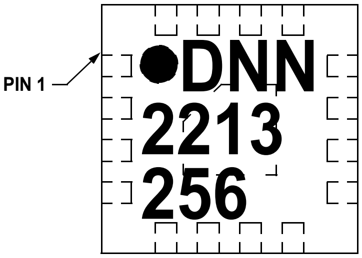
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

16-Lead QFN (3 x 3 mm)



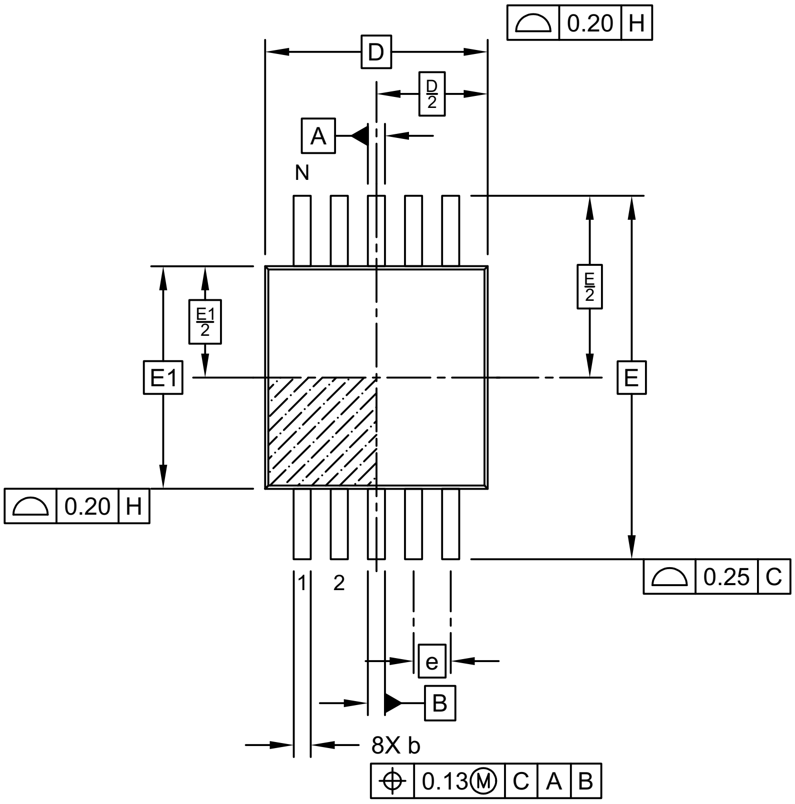
Part Number	Code
MCP48CVD01-E/MG	DNN
MCP48CVD11-E/MG	DPP
MCP48CVD21-E/MG	DRR
MCP48CVD02-E/MG	DAK
MCP48CVD12-E/MG	DAL
MCP48CVD22-E/MG	DAM
MCP48CMD01-E/MG	DKK
MCP48CMD11-E/MG	DLL
MCP48CMD21-E/MG	DMM
MCP48CMD02-E/MG	DAG
MCP48CMD12-E/MG	DAH
MCP48CMD22-E/MG	DAJ

Example

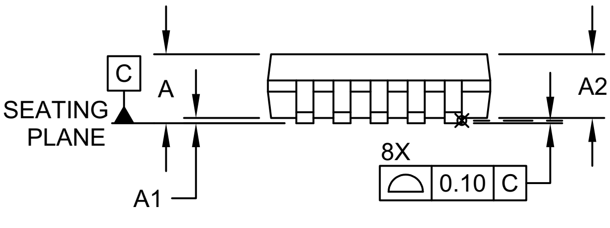


10-Lead Plastic Micro Small Outline Package (UN) - 3x3 mm Body [MSOP]

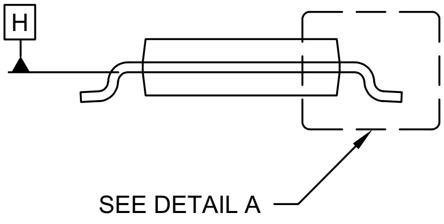
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

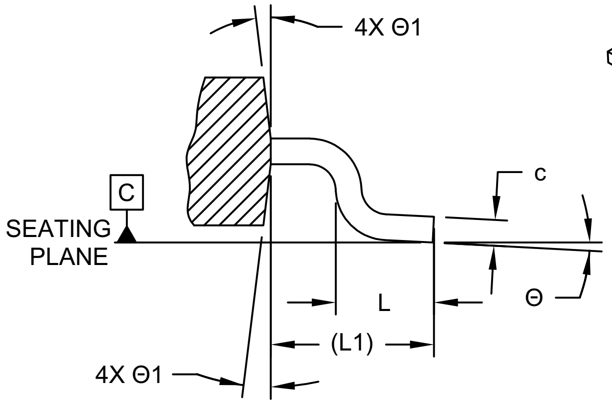


END VIEW

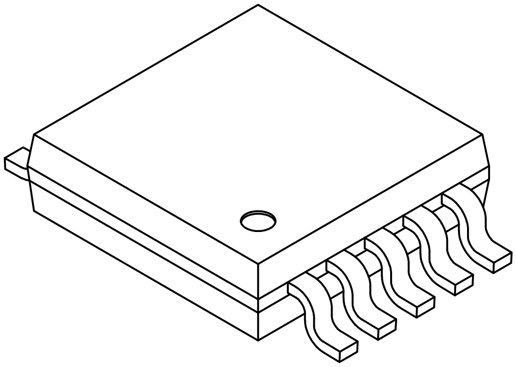
Microchip Technology Drawing C04-021-UN Rev F Sheet 1 of 2

10-Lead Plastic Micro Small Outline Package (UN) - 3x3 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL A



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	10		
Pitch	e	0.50 BSC		
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E	4.90 BSC		
Molded Package Width	E1	3.00 BSC		
Overall Length	D	3.00 BSC		
Foot Length	L	0.40	0.60	0.80
Footprint	L1	0.95 REF		
Foot Angle	Θ	0°	-	8°
Mold Draft Angle	Θ1	5°	-	15°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.15	-	0.33

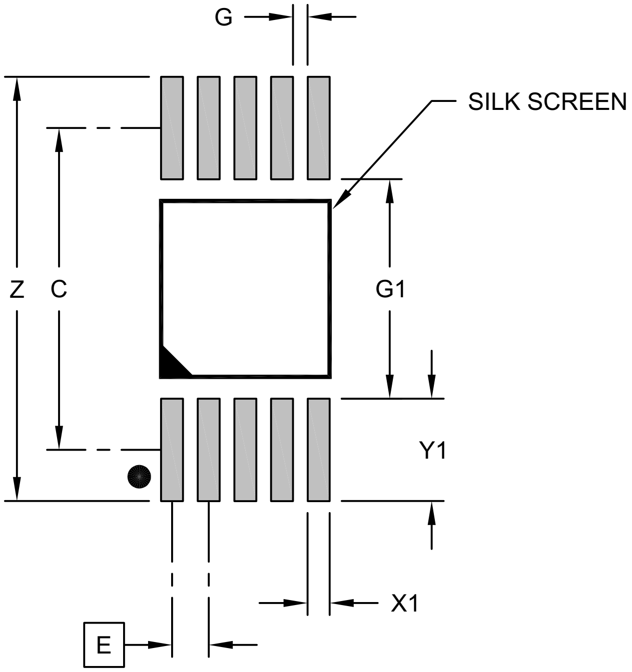
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
    BSC: Basic Dimension. Theoretically exact value shown without tolerances.
    REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-021-UN Rev F Sheet 2 of 2

10-Lead Plastic Micro Small Outline Package (UN) - 3x3 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.80
Contact Pad Width (X10)	X1			0.30
Contact Pad Length (X10)	Y1			1.40
Distance Between Pads (X5)	G1	3.00		
Distance Between Pads (X8)	G	0.20		

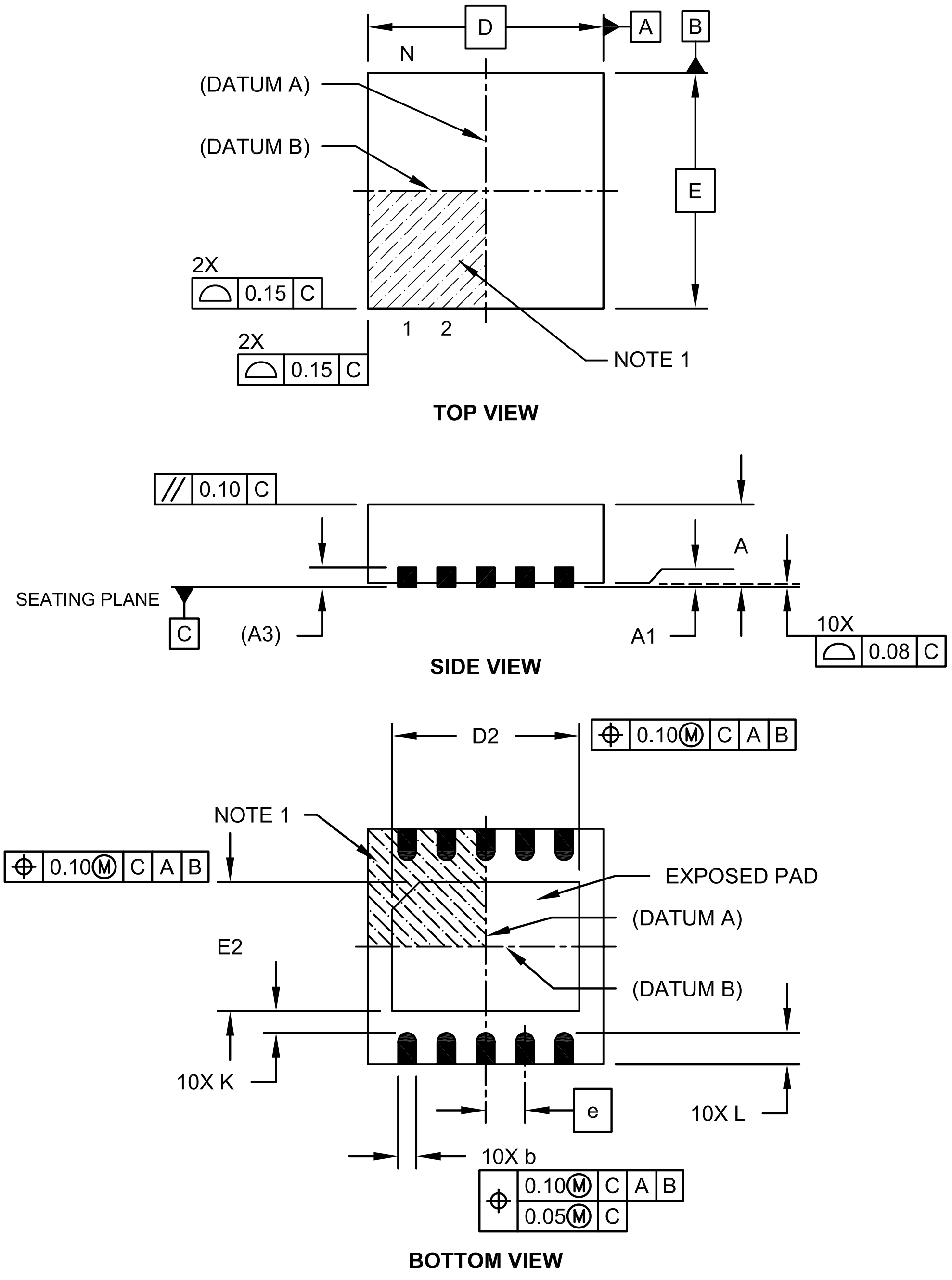
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2021-UN Rev F

10-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

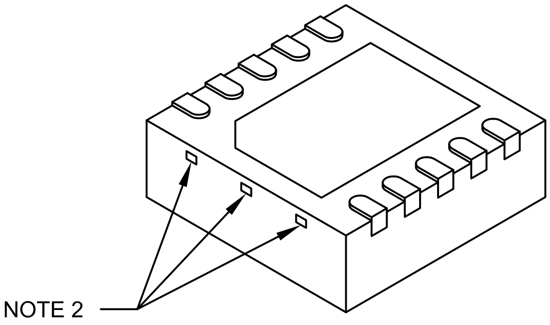
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-063C Sheet 1 of 2

10-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	10		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	3.00 BSC		
Exposed Pad Length	D2	2.15	2.35	2.45
Overall Width	E	3.00 BSC		
Exposed Pad Width	E2	1.40	1.50	1.75
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

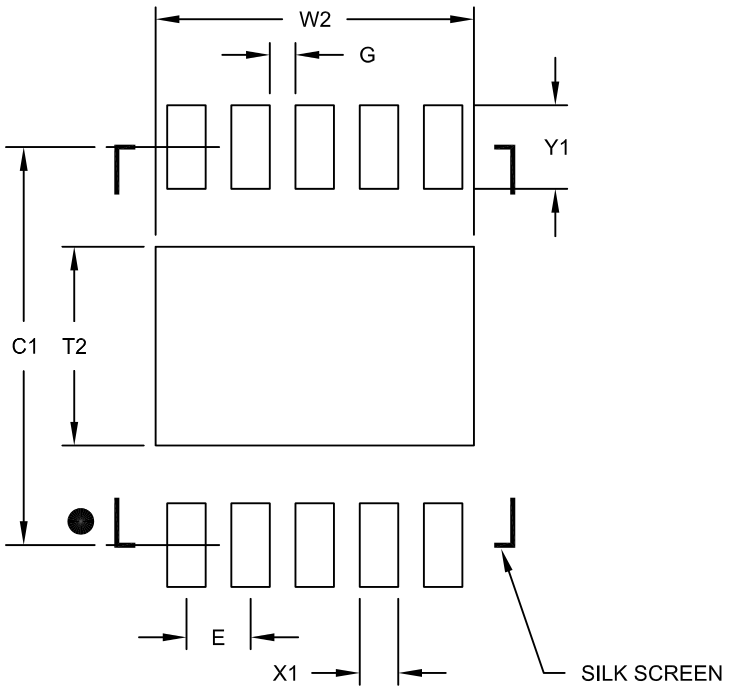
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-063C Sheet 2 of 2

10-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			2.48
Optional Center Pad Length	T2			1.55
Contact Pad Spacing	C1		3.10	
Contact Pad Width (X10)	X1			0.30
Contact Pad Length (X10)	Y1			0.65
Distance Between Pads	G	0.20		

Notes:

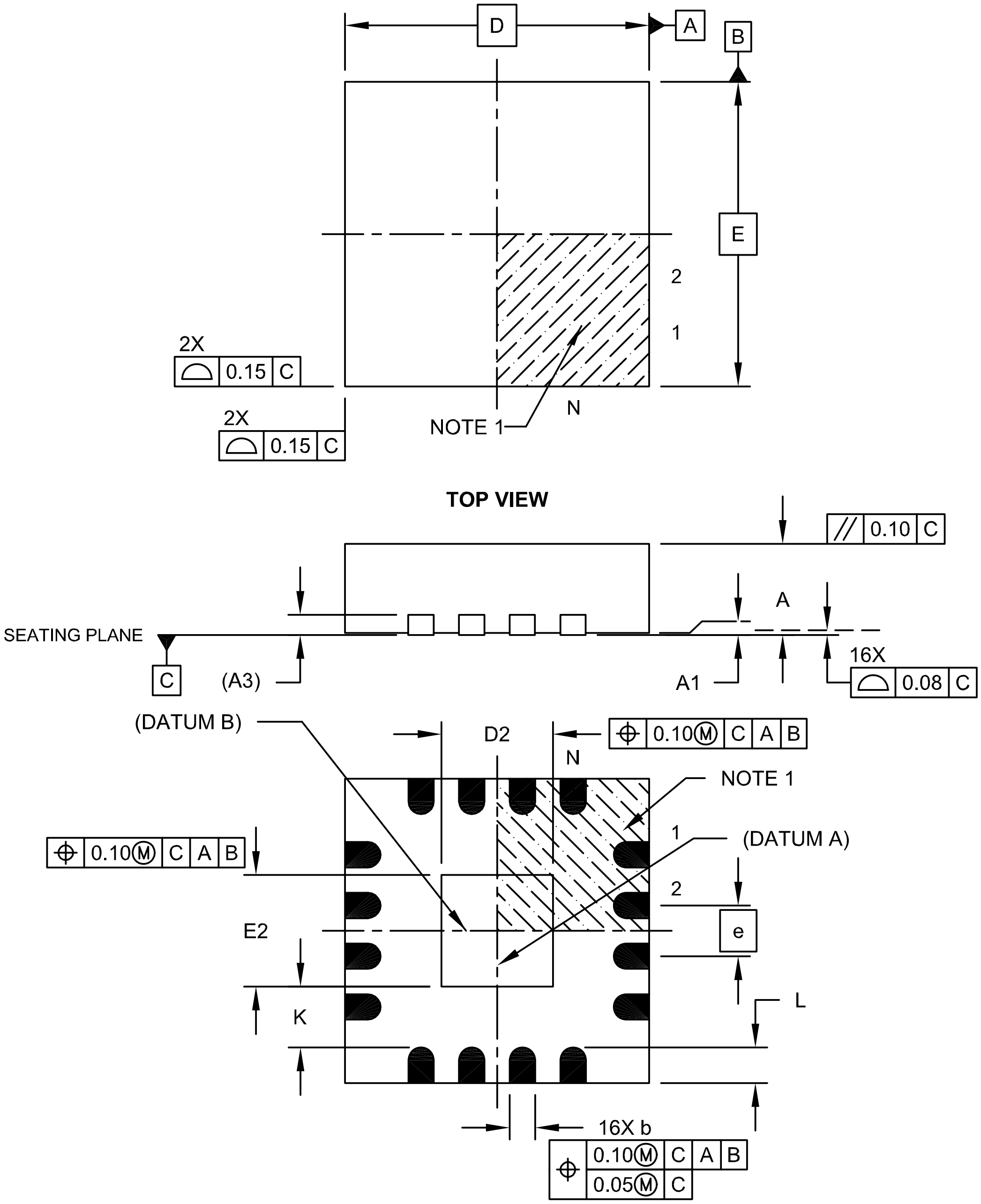
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2063B

16-Lead Plastic Quad Flat, No Lead Package (MG) - 3x3x0.9 mm Body [QFN]

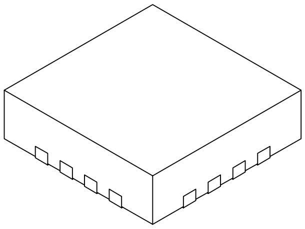
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-142A Sheet 1 of 2

16-Lead Plastic Quad Flat, No Lead Package (MG) - 3x3x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.00	1.10	1.50
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	1.00	1.10	1.50
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.25	0.35	0.45
Contact-to-Exposed Pad	K	0.20	-	-

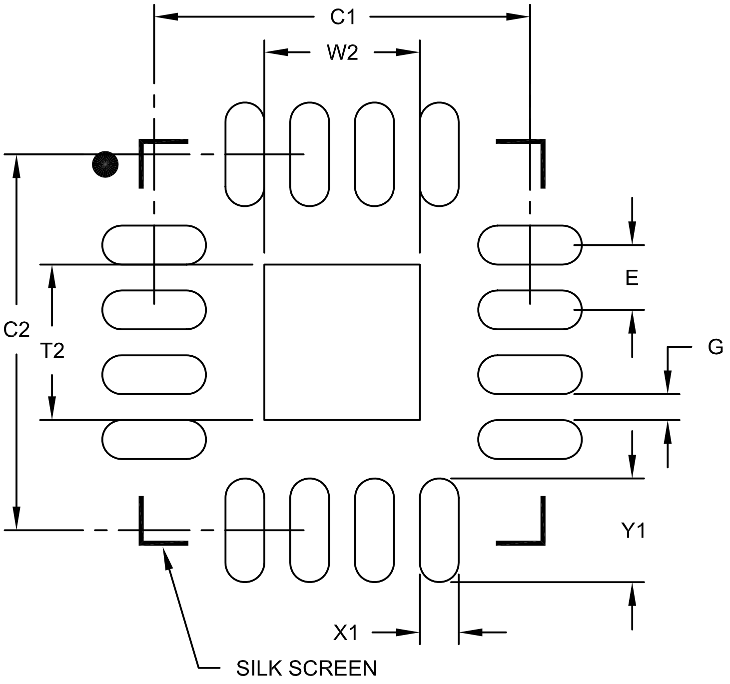
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-142A Sheet 2 of 2

16-Lead Plastic Quad Flat, No Lead Package (MG) – 3x3x0.9 mm Body [QFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			1.20
Optional Center Pad Length	T2			1.20
Contact Pad Spacing	C1		2.90	
Contact Pad Spacing	C2		2.90	
Contact Pad Width (X16)	X1			0.30
Contact Pad Length (X16)	Y1			0.80
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2142A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (April 2022)

- Original release of this document

Note: The SPI standard uses the terminology "Master" and "Slave". The equivalent Microchip terminology used in this document is "Host" and "Client", respectively.

NOTES:

APPENDIX B: TERMINOLOGY

B.1 Resolution

The resolution is the number of DAC output states that divide the full-scale range. For the 12-bit DAC, the resolution is 2^{12}, meaning the DAC code ranges from 0 to 4095.

Note:	When there are 2^N resistors in the resistor ladder and 2^N tap points, the full-scale DAC register code is the resistor element (1 LSb) from the source reference voltage (V_{DD} or V_{REF}).

B.2 Least Significant Bit (LSb)

This is the voltage difference between two successive codes. For a given output voltage range, it is divided by the resolution of the device (see the equation below). The range may be V_{DD} (or V_{REF}) to V_{SS} (ideal), the DAC register codes across the linear range of the output driver (Measured 1) or full-scale to zero-scale (Measured 2).

EQUATION B-1: LSb VOLTAGE CALCULATION

Ideal:

$$V_{LSb(IDEAL)} = \frac{V_{DD}}{2^N} \text{ or } \frac{V_{REF}}{2^N}$$

Measured 1 (12-bit device):

$$V_{LSb(Measured)} = \frac{V_{OUT(@4032)} - V_{OUT(@64)}}{(4032 - 64)}$$

Measured 2:

$$V_{LSb} = \frac{V_{OUT(@FS)} - V_{OUT(@ZS)}}{2^N - 1}$$

2^N = 4096 (MCP48CXD2X)
= 1024 (MCP48CXD1X)
= 256 (MCP48CXD0X)

B.3 Monotonic Operation

The monotonic operation means that the device's output voltage (V_{OUT}) increases with every 1 code step (LSb) increment (from V_{SS} to the DAC's reference voltage (V_{DD} or V_{REF})).

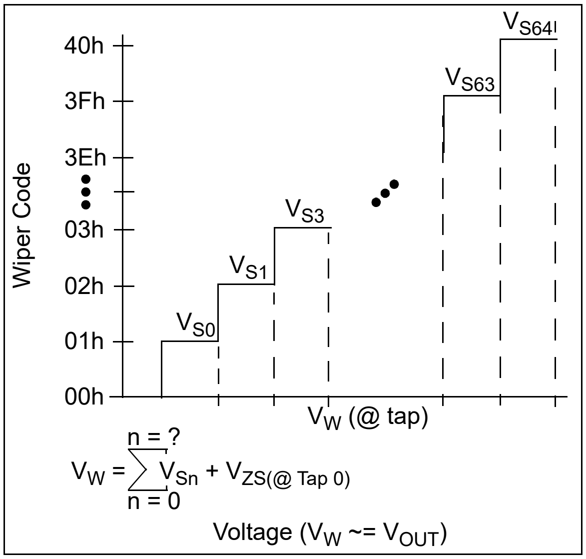


FIGURE B-1: ***V_W (V_{OUT}).***

B.4 Full-Scale Error (E_{FS})

The full-scale error (see Figure B-3) is the error on the V_{OUT} pin relative to the expected V_{OUT} voltage (theoretical) for the maximum device DAC register code (code FFFh for 12-bit, code 3FFh for 10-bit and code FFh for 8-bit) (see the equation below). The error depends on the resistive load on the V_{OUT} pin (and where that load is tied to, such as V_{SS} or V_{DD}). For loads (to V_{SS}) greater than specified, the full-scale error will be greater.

The error in bits is determined by the theoretical voltage step size to give an error in LSb.

EQUATION B-2: FULL-SCALE ERROR

$$E_{FS} = \frac{V_{OUT(@FS)} - V_{IDEAL(@FS)}}{V_{LSb(IDEAL)}}$$

Where:

E_{FS} is expressed in LSb.

$V_{OUT(@FS)}$ = the V_{OUT} voltage when the DAC register code is at full scale

$V_{IDEAL(@FS)}$ = the ideal output voltage when the DAC register code is at full scale

$V_{LSb(IDEAL)}$ = the theoretical voltage step size

B.5 Zero-Scale Error (E_{ZS})

The zero-scale error (see Figure B-2) is the difference between the ideal and measured V_{OUT} voltage with the DAC register code equal to 000h (see the equation below). The error depends on the resistive load on the V_{OUT} pin (and where that load is tied to, such as V_{SS} or V_{DD}). For loads (to V_{DD}) greater than specified, the zero-scale error is greater.

The error in bits is determined by the theoretical voltage step size to give an error in LSb.

EQUATION B-3: ZERO SCALE ERROR

$$E_{ZS} = \frac{V_{OUT(@ZS)}}{V_{LSb(IDEAL)}}$$

Where:

E_{ZS} is expressed in LSb.

$V_{OUT(@ZS)}$ = the V_{OUT} voltage when the DAC register code is at zero scale

$V_{LSb(IDEAL)}$ = the theoretical voltage step size

B.6 Total Unadjusted Error (E_T)

The total unadjusted error (E_T) is the difference between the ideal and the measured V_{OUT} voltage. Typically, calibration of the output voltage is implemented to improve the system's performance.

The error in bits is determined by the theortical voltage step size to give an error in LSb.

The equation below shows the total unadjusted error calculation

EQUATION B-4: TOTAL UNADJUSTED ERROR CALCULATION

$$E_T = \frac{(V_{OUT\_Actual(@code)} - V_{OUT\_Ideal(@code)})}{V_{LSb(Ideal)}}$$

Where:

E_T is expressed in LSb.

$V_{OUT\_Actual(@code)}$ = the measured DAC output voltage at the specified code

$V_{OUT\_Ideal(@code)}$ = the calculated DAC output voltage at the specified code (code * $V_{LSb(Ideal)}$)

$V_{LSb(Ideal)}$ = V_{REF}/# Steps
12-bit = V_{REF}/4096
10-bit = V_{REF}/1024
8-bit = V_{REF}/256

B.7 Offset Error (E_{OS})

The offset error is the delta voltage of the V_{OUT} voltage from the ideal output voltage at the specified code. This code is specified where the output amplifier is in the linear operating range; for the MCP48CXDX1/2, we specify code 64 (decimal). The offset error does not include gain error, which is illustrated in the figure below.

This error is expressed in mV. The offset error can be negative or positive. The error can be calibrated by software in application circuits.

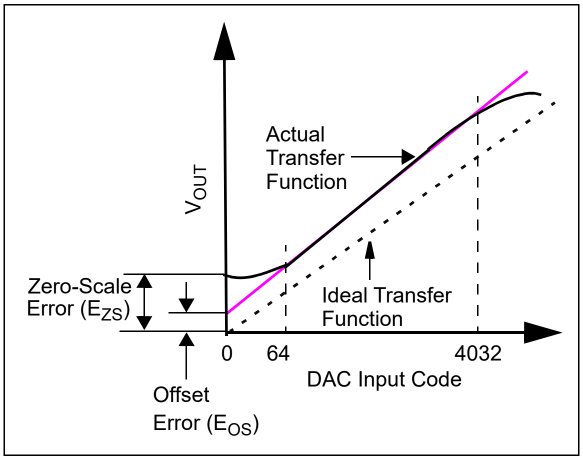


FIGURE B-2: OFFSET ERROR (ZERO GAIN ERROR).

B.8 Offset Error Drift (E_{OSD})

The offset error drift is the variation in offset error due to a change in ambient temperature. The offset error drift is typically expressed in ppm/°C or µV/°C.

B.9 Gain Error (E_G)

Gain error is a calculation based on the ideal slope using the voltage boundaries for the linear range of the output driver (e.g., code 64 and code 4032) (see the figure below). The gain error calculation nullifies the device's offset error.

The gain error indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. The gain error is usually expressed as a percentage of full-scale range (% of FSR) or in LSb. FSR is the ideal full-scale voltage of the DAC (see the equation below).

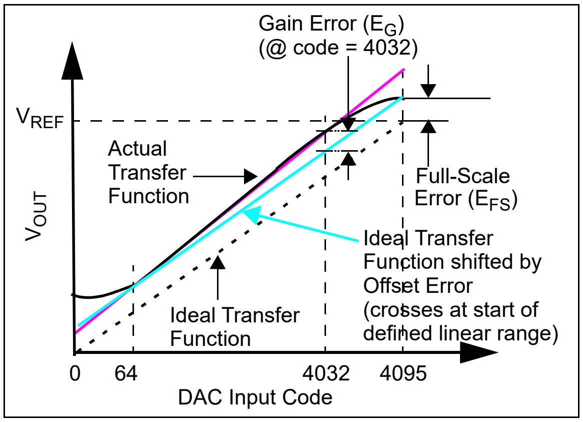


FIGURE B-3: GAIN ERROR AND FULL-SCALE ERROR EXAMPLE.

EQUATION B-5: GAIN ERROR EXAMPLE

$$E_G = \frac{(V_{OUT(@4032)} - V_{OS} - V_{OUT\_Ideal(@4032)})}{V_{Full\text{-}Scale\ Range}} * 100$$

Where:

E_G is expressed in % of FSR.

$V_{OUT(@4032)}$ = the measured DAC output voltage at the specified code

$V_{OUT\_Ideal(@4032)}$ = the calculated DAC output voltage at the specified code (4032 * $V_{LSb(Ideal)}$)

V_{OS} = measured offset voltage

$V_{Full\text{-}Scale\ Range}$ = Expected full-scale output value (such as the V_{REF} voltage)

B.10 Gain Error Drift (E_{GD})

The gain error drift is the variation in gain error due to a change in ambient temperature. The gain error drift is typically expressed in ppm/°C (of FSR).

B.11 Integral Nonlinearity (INL)

The integral nonlinearity (INL) error is the maximum deviation of an actual transfer function from an ideal transfer function (straight line) passing through the defined end-points of the DAC transfer function (after offset and gain errors are removed).

For the MCP48CXDX1/2, INL is calculated using the defined end-points, DAC code 64 and code 4032. INL can be expressed as a percentage of FSR or in LSb. INL is also called relative accuracy. The equation below shows how to calculate the INL error in LSb, and the figure below shows an example of INL accuracy.

Positive INL means a V_{OUT} voltage higher than the ideal one. Negative INL means a V_{OUT} voltage lower than the ideal one.

EQUATION B-6: INL ERROR

$$E_{INL} = \frac{(V_{OUT} - V_{Calc\_Ideal})}{V_{LSb(Measured)}}$$

Where:

INL is expressed in LSb.

V_{Calc_Ideal} = Code * $V_{LSb(Measured)}$ + V_{OS}

V_{OUT} = the measured DAC output voltage with a given DAC register code

$V_{LSb(Measured)}$ = for measured: ($V_{OUT(4032)}$ - $V_{OUT(64)}$)/3968

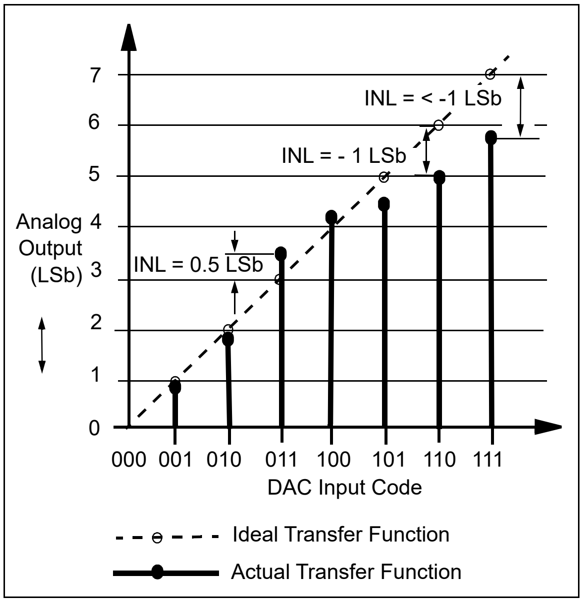


FIGURE B-4: INL ACCURACY.

B.12 Differential Nonlinearity (DNL)

The differential nonlinearity (DNL) error (see Figure B-5) is the measure of step size between codes in actual transfer function. The ideal step size between codes is 1 LSb. A DNL error of zero would imply that every code is exactly 1 LSb wide. If the DNL Error is less than 1 LSb, the DAC guarantees monotonic output and no missing codes. The equation below shows how to calculate the DNL Error between any two adjacent codes in LSb.

EQUATION B-7: DNL ERROR

$$E_{DNL} = \frac{(V_{OUT(code = n+1)} - V_{OUT(code = n)})}{V_{LSb(Measured)}} - 1$$

Where:

DNL is expressed in LSb.

$V_{OUT(Code = n)}$ = the measured DAC output voltage with a given DAC register code

$V_{LSb(Measured)}$ = for measured: $(V_{OUT(4032)} - V_{OUT(64)})/3968$

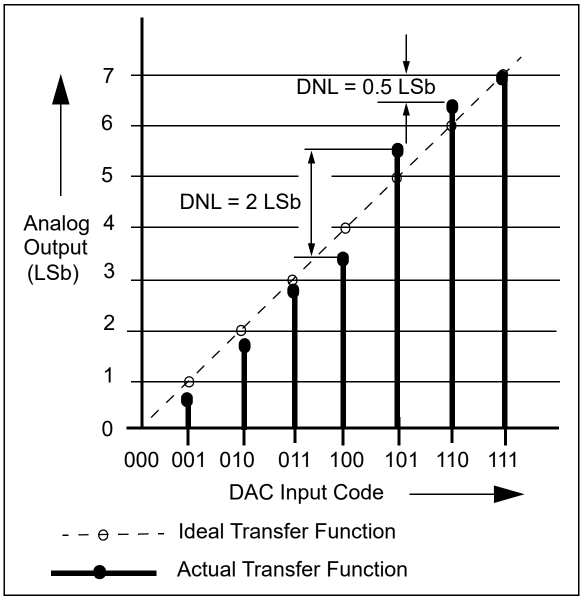


FIGURE B-5: DNL ACCURACY.

B.13 Settling Time

The settling time is the time delay required for the V_{OUT} voltage to settle into its new output value. This time is measured from the start of the code transition to when the V_{OUT} voltage is within the specified accuracy.

For the MCP48CXDX1/2, the settling time is a measure of the time delay until the V_{OUT} voltage reaches within 0.5 LSb of its final value, when the volatile DAC register changes from 1/4 to 3/4 of the FSR (12-bit device: 400h to C00h).

B.14 Major-Code Transition Glitch

Major-Code transition glitch is the impulse energy injected into the DAC analog output when the code in the DAC register changes the state. It is normally specified as the area of the glitch in nV-Sec and is measured when the digital code is changed by 1 LSb at the major carry transition (Example: `011...111` to `100... 000` or `100... 000` to `011... 111`).

B.15 Digital Feed-Through

The digital feed-through is the glitch that appears at the analog output caused by coupling from the digital input pins of the device. The area of the glitch is expressed in nV-Sec and is measured with a full-scale change (example: all `0`s to all `1`s and vice versa) on the digital input pins. The digital feed-through is measured when the DAC is not being written to the output register.

B.16 -3 dB Bandwidth

This is the frequency of the signal at the V_{REF} pin that causes the voltage at the V_{OUT} pin to fall to -3 dB from a static value on the V_{REF} pin. The output decreases due to the RC characteristics of the resistor ladder and the characteristics of the output buffer.

B.17 Power-Supply Sensitivity (PSS)

PSS indicates how the output of the DAC is affected by changes in the supply voltage. PSS is the ratio of the change in V_{OUT} to a change in V_{DD} for mid-scale output of the DAC. The V_{OUT} is measured while the V_{DD} is varied from 5.5V to 2.7V as a step (V_{REF} voltage held constant) and expressed in %/%, which is the % change of the DAC output voltage with respect to the % change of the V_{DD} voltage.

EQUATION B-8: PSS CALCULATION

$$PSS = \frac{(V_{OUT(@5.5V)} - V_{OUT(@2.7V)})/V_{OUT(@5.5V)}}{(5.5V - 2.7V)/(5.5V)}$$

Where:

PSS is expressed in %/%.

$V_{OUT(@5.5V)}$ = the measured DAC output voltage with V_{DD} = 5.5V

$V_{OUT(@2.7V)}$ = the measured DAC output voltage with V_{DD} = 2.7V

B.18 Power-Supply Rejection Ratio (PSRR)

PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. The V_{OUT} is measured while the V_{DD} is varied +/-10% (V_{REF} voltage held constant) and expressed in dB or µV/V.

B.19 V_{OUT} Temperature Coefficient

The V_{OUT} temperature coefficient quantifies the error in the resistor ladder's resistance ratio (DAC register code value) and the output buffer due to temperature drift.

B.20 Absolute Temperature Coefficient

The absolute temperature coefficient quantifies the error in the end-to-end output voltage (nominal output voltage V_{OUT}) due to temperature drift. For a DAC, this error is typically not an issue due to the ratiometric aspect of the output.

B.21 Noise Spectral Density

The noise spectral density is a measurement of the device's internally generated random noise and is characterized as a spectral density (voltage per √Hz). It is measured by loading the DAC to the mid-scale value and measuring the noise at the V_{OUT} pin. It is measured in nV/√Hz.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X [(1)]	—	X	/XX
Device	Tape and Reel		Temperature Range	Package

Device: MCP48CXDX1/2:1 LSb INL Voltage Output Digital-to-Analog Converters, with SPI Interface, 8/10/12-bit Resolution, Single/Dual Outputs and Volatile/MTP Memory

Tape and Reel: T = Tape and Reel

Temperature Range: E = -40°C to +125°C (Extended)

Package:
MF = Plastic Dual Flat, No Lead Package (DFN), 3 x 3 x 0.9 mm, 10-Lead
MG = Plastic Quad Flat, No Lead Package (QFN), 3 x 3 x 0.9 mm, 16-Lead
UN = Plastic Micro Small Outline Package (MSOP), 10-Lead

Examples:

a) MCP48CVD01-E/MF:	1 LSb INL Voltage Output Digital-to-Analog Converter, 8-bit Resolution, Extended Temperature, 10LD DFN, with volatile memory.
b) MCP48CVD01T-E/MF:	1 LSb INL Voltage Output Digital-to-Analog Converter, 8-bit Resolution, Tape and Reel, Extended Temperature, 10LD DFN, with volatile memory
a) MCP48CVD12-E/MG:	1 LSb INL Voltage Output Digital-to-Analog Converter, 10-bit Resolution, Extended Temperature, 16LD QFN, with volatile memory.
b) MCP48CVD12T-E/MG:	1 LSb INL Voltage Output Digital-to-Analog Converter, 10-bit Resolution, Tape and Reel, Extended Temperature, 16LD QFN, with volatile memory.
a) MCP48CMD21-E/UN:	1 LSb INL Voltage Output Digital-to-Analog Converter, 12-bit Resolution, Extended Temperature, 10LD MSOP, with nonvolatile memory.
b) MCP48CMD21T-E/UN:	1 LSb INL Voltage Output Digital-to-Analog Converter, 12-bit Resolution, Tape and Reel, Extended Temperature, 10LD MSOP, with nonvolatile memory.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at https://www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

For information regarding Microchip’s Quality Management Systems, please visit www.microchip.com/quality.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AnyRate, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, APT, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, IntelliMOS, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, Temux, TimeCesium, TimeHub, TimePictra, TimeProvider, TrueTime, WinPath, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, GridTime, IdealBridge, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, Inter-Chip Connectivity, JitterBlocker, Knob-on-Display, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, NVM Express, NVMe, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SmartHLS, SMART-I.S., storClad, SQI, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, TSHARC, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, Symmcom, and Trusted Time are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2022, Microchip Technology Incorporated and its subsidiaries.

All Rights Reserved.

ISBN: 978-1-6683-0099-2

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4485-5910
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820