

## Quad, Parallel Input, Voltage Output, 12-/10-Bit Digital-to-Analog Converter

### FEATURES

- ▶ 12-bit linearity and monotonic [AD5582](#)
- ▶ 10-bit linearity and monotonic [AD5583](#)
- ▶ Wide operating range: single 5 V to 15 V or dual  $\pm 5$  V supply
- ▶ Unipolar or bipolar operation
- ▶ Double buffered registers enable independent or simultaneous multichannel updates
- ▶ 4 independent rail-to-rail reference inputs
- ▶ 20 mA high current output drive
- ▶ Parallel interface
- ▶ Data readback capability
- ▶ 5  $\mu$ s settling time
- ▶ Built-in matching resistor simplifies negative reference
- ▶ Unconditionally stable under any capacitive loading
- ▶ Compact footprint: [TSSOP-48](#)
- ▶ Extended temperature range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$

### APPLICATIONS

- ▶ Process control equipment
- ▶ Closed-loop servo control
- ▶ Data acquisition systems
- ▶ Digitally controlled calibration
- ▶ Optical network control loops
- ▶ 4 mA to 20 mA current transmitter

### GENERAL DESCRIPTION

The AD5582/AD5583 family of quad, 12-/10-bit, voltage output digital-to-analog converters is designed to operate from a single 5 V to 15 V or dual  $\pm 5$  V supply. It offers the user ease of use in single- or dual-supply systems. Built using an advance BiCMOS process, this high performance DAC is dynamically stable, capable of high current drive, and in a small form factor.

The applied external reference  $V_{REF}$  determines the full-scale output voltage ranges from  $V_{SS}$  to  $V_{DD}$ , resulting in a wide selection of full-scale outputs. For multiplying and wide dynamic applications, ac reference inputs can be as high as  $|V_{DD} - V_{SS}|$ . Two built-in precision trimmed resistors are available and can be configured easily to provide four-quadrant multiplications.

A doubled-buffered parallel interface offers a fast settling time. A common level sensitive load DAC strobe (LDAC) input allows

### FUNCTIONAL BLOCK DIAGRAM

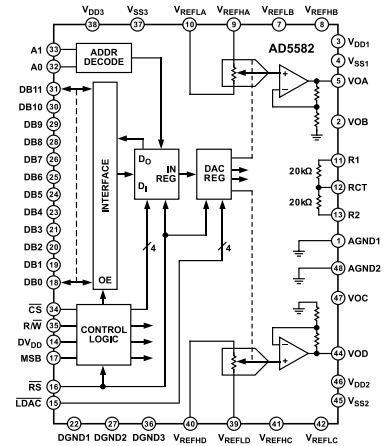
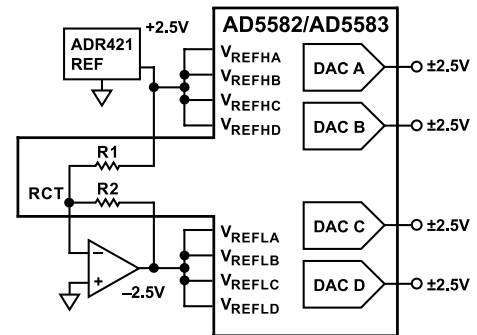


Figure 1. AD5582 Functional Block Diagram



DIGITAL CIRCUITRY OMITTED FOR CLARITY

Figure 2. Using Built-In Matching Resistors to Generate a Negative Voltage Reference

additional simultaneous update of all DAC outputs. An external asynchronous reset (RS) forces all registers to the zero code state when the MSB = 0 or to midscale when the MSB = 1.

Both parts are offered in the same pinout and package to allow users to select the appropriate resolution for a given application without PCB layout changes. The [AD5582](#) is well suited for [DAC8412](#) replacement in medium voltage applications in new designs, as well as any other general purpose multichannel 10- to 12-bit applications.

The AD5582/AD5583 are specified over the extended industrial ( $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ) temperature range and offered in a thin and compact [1.1 mm TSSOP-48 package](#).

Rev. B

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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**TABLE OF CONTENTS**

Features.....	1	Power Supplies.....	19
Applications.....	1	Reference Input.....	19
Functional Block Diagram.....	1	Digital I/O.....	19
General Description.....	1	Reset.....	20
Specifications.....	3	Output Amplifiers.....	20
Electrical Characteristics.....	3	Glitch.....	20
Timing Characteristics.....	5	Layout and Power Supply Bypassing.....	20
Absolute Maximum Ratings.....	7	Applications Information.....	21
ESD Caution.....	7	Programmable Current Source.....	21
Pin Configuration and Function Descriptions.....	8	Boosted Programmable Voltage Source.....	22
Timing Diagrams.....	11	Programmable PGA.....	23
Typical Performance Characteristics.....	13	Outline Dimensions.....	24
Test Circuit.....	18	Ordering Guide.....	24
Theory of Operation.....	19		

**REVISION HISTORY****1/2023—Rev. A to Rev. B**

Updated Format (Universal).....	1
Changes to Gain Error Parameter, Table 1.....	3
Change to Table 7.....	9
Changes to Ordering Guide.....	24

## SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

$V_{DD} = +5\text{ V}$ ,  $V_{SS} = -5\text{ V}$ ,  $DV_{DD} = +5\text{ V} \pm 10\%$ ,  $V_{REFH} = +2.5\text{ V}$ ,  $V_{REFL} = -2.5\text{ V}$ ,  $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Condition	Min	Typ <sup>1</sup>	Max	Unit
STATIC PERFORMANCE						
Resolution <sup>2</sup>	N	AD5582		12		Bits
		AD5583		10		Bits
Relative Accuracy <sup>3</sup>	INL		-1		+1	LSB
Differential Nonlinearity <sup>3</sup>	DNL	Monotonic	-1			LSB
Zero-Scale Error	$V_{ZSE}$	Data = 000 <sub>H</sub> for AD5582 and AD5583	-2		+2	LSB
Gain Error	$V_{GE}$	Data = 0xFFF <sub>H</sub> for AD5582	-2.5		+2.5	LSB
	$V_{GE}$	Data = 0x3FF <sub>H</sub> for AD5583	-4		+4	LSB
	$V_{GE}$	$V_{DD} = 2.7\text{ V to }4.5\text{ V}$	-4		+4	LSB
Full-Scale Tempco <sup>4</sup>	$TCV_{FS}$			1.5		ppm/°C
REFERENCE INPUT						
$V_{REFH}$ Input Range	$V_{REFH}$		$V_{REFL} + 0.5$		$V_{DD}$	V
$V_{REFL}$ Input Range <sup>5</sup>	$V_{REFL}$		$V_{SS}$		$V_{REFH} - 0.5$	V
Input Resistance	$R_{REF}$	Data = 555 <sub>H</sub> (minimum $R_{REF}$ ) for AD5582 and 155 <sub>H</sub> for AD5583	12	20		k $\Omega$ <sup>1</sup>
Input Capacitance <sup>4</sup>	$C_{REF}$			80		pF
REF Input Current	$I_{REF}$	Data = 555 <sub>H</sub> for AD5582			500	$\mu\text{A}$
REF Multiplying Bandwidth	$BW_{REF}$	Code = full scale			1.3	MHz
R1–R2 Matching	R1/R2	AD5582			$\pm 0.025$	%
		AD5583			$\pm 0.100$	%
ANALOG OUTPUT						
Output Current <sup>6</sup>	$I_{OUT}$	Data = 800 <sub>H</sub> for AD5582 and 200 <sub>H</sub> for AD5583, $\Delta V_{OUT} \leq 2\text{ mV}$			$\pm 2$	mA
	$I_{OUT}$	Data = 800 <sub>H</sub> for AD5582 and 200 <sub>H</sub> for AD5583, $\Delta V_{OUT} \leq  -8\text{ mV} $			+20	mA
		$\Delta V_{OUT} \leq \pm 15\text{ mV}$			-20	mA
Capacitive Load <sup>4,7</sup>	$C_L$	No oscillation		Note <sup>7</sup>		pF
LOGIC INPUTS						
Logic Input Low Voltage	$V_{IL}$	$DV_{DD} = 5\text{ V} \pm 10\%$			0.8	V
		$DV_{DD} = 3\text{ V} \pm 10\%$			0.4	V
Logic Input High Voltage	$V_{IH}$	$DV_{DD} = 5\text{ V} \pm 10\%$	2.4			V
		$DV_{DD} = 3\text{ V} \pm 10\%$	2.1			V
Input Leakage Current	$I_{IL}$			0.01	1	$\mu\text{A}$
Input Capacitance <sup>4</sup>	$C_{IL}$			5		pF
Output Voltage High	$V_{OH}$	$I_{OH} = -0.8\text{ mA}$	2.4			V
Output Voltage Low	$V_{OL}$	$I_{OL} = 1.2\text{ mA}$ , $T_A = 85^\circ\text{C}$ , $I_{OL} = 0.6\text{ mA}$ , $DV_{DD} = 3\text{ V}$			0.4	V
		$I_{OL} = 1.0\text{ mA}$ , $T_A = 125^\circ\text{C}$ , $I_{OL} = 0.5\text{ mA}$ , $DV_{DD} = 3\text{ V}$			0.4	V
AC CHARACTERISTICS						
Output Slew Rate	SR	Data = zero scale to full scale to zero scale		2		V/ $\mu\text{s}$
Settling Time <sup>8</sup>	$t_S$	To $\pm 0.1\%$ of full scale		5		$\mu\text{s}$
DAC Glitch	Q	To 1FF <sub>H</sub> for AD5583		100		nV-s
Digital Feedthrough	$V_{OUT}/t_{CS}$	Data = midscale, $\overline{CS}$ toggles at $f = 16\text{ MHz}$		5		nV-s
Analog Crosstalk	$V_{OUT}/V_{REF}$	$V_{REF} = 1.5\text{ V dc} + 1\text{ V p-p}$ , data = 000 <sub>H</sub> , $f = 100\text{ kHz}$		-80		dB
Output Noise	$e_N$	$f = 1\text{ kHz}$		33		nV/ $\sqrt{\text{Hz}}$

## SPECIFICATIONS

Table 1. (Continued)

Parameter	Symbol	Condition	Min	Typ <sup>1</sup>	Max	Unit
SUPPLY CHARACTERISTICS						
Single-Supply Voltage Range	V <sub>DD</sub>	V <sub>SS</sub> = 0 V	3		18	V
Dual-Supply Voltage Range	V <sub>DD</sub> /V <sub>SS</sub>	V <sub>DD</sub> = +2.7 V to +6.5 V, V <sub>SS</sub> = -6.5 V to -2.7 V	-9		+9	V
Digital Logic Supply	DV <sub>DD</sub>		2.7		8	V
Positive Supply Current <sup>6</sup>	I <sub>DD</sub>	V <sub>IL</sub> = 0 V, no load		1.7	3	mA
Negative Supply Current	I <sub>SS</sub>	V <sub>IL</sub> = 0 V, no load		1.5	3	mA
Power Dissipation	P <sub>DISS</sub>	V <sub>IL</sub> = 0 V, no load		16	30	mW
Power Supply Sensitivity	P <sub>SS</sub>	ΔV <sub>DD</sub> = ±5%		30		ppm/V

<sup>1</sup> Typical specifications represent average readings measured at 25°C.

<sup>2</sup> DAC output equation:  $V_{OUT} = V_{REFL} + [(V_{REFH} - V_{REFL}) \times D/2^N]$ , where D = data loaded in corresponding DAC Register A, B, C, D, and N equals the number of bits; AD5582 = 12 bits, AD5583 = 10 bits. One LSB step voltage =  $(V_{REFH} - V_{REFL})/4096$  V and  $(V_{REFH} - V_{REFL})/1024$  V for the AD5582 and the AD5583, respectively.

<sup>3</sup> The first two codes (000H, 001H) of the AD5583 and the first four codes (000H, 001H, 002H, 003H) of the AD5582 are excluded from the linearity error measurement in single-supply operation.

<sup>4</sup> These parameters are guaranteed by design and not subject to production testing.

<sup>5</sup> Dual-supply operation, V<sub>REFL</sub> = V<sub>SS</sub>, exclude the lowest eight codes for the AD5582 and two codes for the AD5583 for INL and DNL errors.

<sup>6</sup> Short circuit output and supply currents are 24 mA and 25 mA, respectively.

<sup>7</sup> Part is stable under any capacitive loading conditions.

<sup>8</sup> The settling time specification does not apply for negative-going transitions within the last 3 LSBs of ground in single-supply operation.

V<sub>DD</sub> = 15 V, V<sub>SS</sub> = 0 V, DV<sub>DD</sub> = 5 V ± 10%, V<sub>REFH</sub> = 10 V, V<sub>REFL</sub> = 0 V, -40°C < T<sub>A</sub> < +125°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Condition	Min	Typ <sup>1</sup>	Max	Unit
STATIC PERFORMANCE						
Resolution <sup>2</sup>	N	AD5582		12		Bits
		AD5583		10		Bits
Relative Accuracy <sup>3</sup>	INL		-1		+1	LSB
Differential Nonlinearity <sup>3</sup>	DNL	Monotonic	-1			LSB
Zero-Scale Error	V <sub>ZSE</sub>	Data = 000 <sub>H</sub> for AD5582 and AD5583	-2		+2	LSB
Gain Error	V <sub>GE</sub>	Data = 0xFFFF <sub>H</sub> for AD5582	-2		+2	LSB
	V <sub>GE</sub>	Data = 0x3FFF <sub>H</sub> for AD5583	-4		+4	LSB
Full-Scale Tempco <sup>4</sup>	TCV <sub>FS</sub>			1.5		ppm/°C
REFERENCE INPUT						
V <sub>REFH</sub> Input Range	V <sub>REFH</sub>		V <sub>REFL</sub> + 0.5		V <sub>DD</sub>	V
V <sub>REFL</sub> Input Range <sup>5</sup>	V <sub>REFL</sub>		V <sub>SS</sub>		V <sub>REFH</sub> - 0.5	V
Input Resistance	R <sub>REF</sub>	Data = 555 <sub>H</sub> (minimum R <sub>REF</sub> ) for AD5582 and 155 <sub>H</sub> for AD5583	12	20		kΩ <sup>1</sup>
Input Capacitance <sup>4</sup>	C <sub>REF</sub>			80		pF
REF Input Current	I <sub>REF</sub>	Data = 555 <sub>H</sub> for AD5582			1000	mA
REF Multiplying Bandwidth	BW <sub>REF</sub>	Code = full scale			1.3	MHz
R1-R2 Matching	R1/R2	AD5582			±0.025	%
		AD5583			±0.100	%
ANALOG OUTPUT						
Output Current <sup>6</sup>	I <sub>OUT</sub>	Data = 800 <sub>H</sub> for AD5582 and 200 <sub>H</sub> for AD5583, ΔV <sub>OUT</sub> ≤ 2 mV			2	mA
	I <sub>OUT</sub>	Data = 800 <sub>H</sub> for AD5582 and 200 <sub>H</sub> for AD5583, ΔV <sub>OUT</sub> ≤  -8 mV			+20	mA
		ΔV <sub>OUT</sub> ≤ 15 mV			-20	mA

## SPECIFICATIONS

Table 2. (Continued)

Parameter	Symbol	Condition	Min	Typ <sup>1</sup>	Max	Unit
Capacitive Load <sup>4,7</sup>	$C_L$	No oscillation		Note 7		pF
<b>LOGIC INPUTS/OUTPUTS</b>						
Logic Input Low Voltage	$V_{IL}$	$DV_{DD} = 3 V \pm 10\%$			0.8	V
Logic Input High Voltage	$V_{IH}$	$DV_{DD} = 3 V \pm 10\%$	2.4		0.4	V
Input Leakage Current	$I_{IL}$		2.1			V
Input Capacitance <sup>4</sup>	$C_{IL}$					$\mu A$
Output Voltage High	$V_{OH}$	$I_{OH} = -0.8 \text{ mA}$	2.4			pF
Output Voltage Low	$V_{OL}$	$I_{OL} = 1.2 \text{ mA}, T_A = 85^\circ\text{C}, I_{OL} = 0.6 \text{ mA}, DV_{DD} = 3 \text{ V}$			0.4	V
	$V_{OL}$	$I_{OL} = 1.0 \text{ mA}, T_A = 125^\circ\text{C}, I_{OL} = 0.5 \text{ mA}, DV_{DD} = 3 \text{ V}$			0.4	V
<b>AC CHARACTERISTICS</b>						
Output Slew Rate	SR	Data = zero scale to full scale to zero scale		2		V/ $\mu s$
Settling Time <sup>8</sup>	$t_S$	To $\pm 0.1\%$ of full scale		14		$\mu s$
DAC Glitch	Q	Code 7FF <sub>H</sub> to 800 <sub>H</sub> to 7FF <sub>H</sub> for AD5582 and 1FF <sub>H</sub> to 200 <sub>H</sub> to 1FF <sub>H</sub> for AD5583		100		nV-s
Digital Feedthrough	$V_{OUT}/t_{CS}$	Data = midscale, $\overline{CS}$ toggles at $f = 16 \text{ MHz}$		5		nV-s
Analog Crosstalk	$V_{OUT}/V_{REF}$	$V_{REF} = 1.5 \text{ V dc} + 1 \text{ V p-p}$ , data = 000 <sub>H</sub> , $f = 100 \text{ kHz}$		-80		dB
Output Noise	$e_N$	$f = 1 \text{ kHz}$		33		nV/ $\sqrt{\text{Hz}}$
<b>SUPPLY CHARACTERISTICS</b>						
Single-Supply Voltage Range	$V_{DD}$	$V_{SS} = 0 \text{ V}$	3		16.5	V
Dual-Supply Voltage Range	$V_{DD}/V_{SS}$	$V_{DD} = +2.7 \text{ V to } +6.5 \text{ V}, V_{SS} = -6.5 \text{ V to } -2.7 \text{ V}$	-6.5		+6.5	V
Digital Logic Supply	$DV_{DD}$		2.7		6.5	V
Positive Supply Current <sup>6</sup>	$I_{DD}$	$V_{IL} = 0 \text{ V}$ , no load		2.3	3.5	mA
Power Dissipation	$P_{DISS}$	$V_{IL} = 0 \text{ V}$ , no load		34.5	52.5	mW
Power Supply Sensitivity	PSS	$\Delta V_{DD} = \pm 5\%$		30		ppm/V

<sup>1</sup> Typical specifications represent average readings measured at 25°C.

<sup>2</sup> DAC output equation:  $V_{OUT} = V_{REFL} + [(V_{REFH} - V_{REFL}) \times D/2^N]$ , where D = data in decimal loaded in corresponding DAC Register A, B, C, D, and N equals the number of bits; AD5582 = 12 bits, AD5583 = 10 bits. One LSB step voltage =  $(V_{REFH} - V_{REFL})/4096 \text{ V}$  and  $(V_{REFH} - V_{REFL})/1024 \text{ V}$  for the AD5582 and the AD5583, respectively.

<sup>3</sup> The first two codes (000H, 001H) of the AD5583 and the first four codes (000H, 001H, 002H, 003H) of the AD5582 are excluded from the linearity error measurement in single-supply operation.

<sup>4</sup> These parameters are guaranteed by design and not subject to production testing.

<sup>5</sup> Dual-supply operation,  $V_{REFL} = V_{SS}$ , exclude the lowest eight codes for the AD5582 and two codes for the AD5583 for INL and DNL errors.

<sup>6</sup> Short circuit output and supply currents are 24 mA and 25 mA, respectively.

<sup>7</sup> Part is stable under any capacitive loading conditions.

<sup>8</sup> The settling time specification does not apply for negative-going transitions within the last 3 LSBs of ground in single-supply operation.

## TIMING CHARACTERISTICS

$V_{DD} = 15 \text{ V}$  or  $5 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ,  $DV_{DD} = 5 \text{ V} \pm 10\%$ ,  $V_{REFH} = 10 \text{ V}$ ,  $V_{REFL} = 0 \text{ V}$ ,  $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ , unless otherwise noted.

Table 3.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>INTERFACE TIMING<sup>1</sup></b>						
Chip Select Write Pulse Width	$t_{WCS}$		20			ns
Chip Select Read Pulse Width	$t_{RCS}$		130			ns
Write Setup	$t_{WS}$		35			ns

## SPECIFICATIONS

Table 3. (Continued)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Write Hold	$t_{WH}$		0			ns
Address Setup	$t_{AS}$		35			ns
Address Hold	$t_{AH}$		0			ns
Load Setup	$t_{LS}$		0			ns
Load Hold	$t_{LH}$		0			ns
Write Data Setup	$t_{WDS}$		35			ns
Write Data Hold	$t_{WDH}$		0			ns
Load Data Pulse Width	$t_{LDW}$		20			ns
Reset Pulse Width	$t_{RESET}$		20			ns
Read Data Hold	$t_{RDH}$		0			ns
Read Data Setup	$t_{RDS}$		0			ns
Data to Hi-Z	$t_{DZ}$	$C_L = 10 \text{ pF}$			100	ns
Chip Select to Data	$t_{CSD}$	$C_L = 10 \text{ pF}$			100	ns
Chip Select Repetitive Pulse Width	$t_{CSP}$		10			ns
Load Setup in Double Buffer Mode	$t_{LDS}$		20			ns
Load Data Hold	$t_{LDH}$		0			ns

<sup>1</sup> All input control signals are specified with  $t_R = t_F = 2 \text{ ns}$  (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

$V_{DD} = 15 \text{ V}$  or  $5 \text{ V}$ ,  $V_{SS} = 0 \text{ V}$ ,  $DV_{DD} = 3 \text{ V} \pm 10\%$ ,  $V_{REFH} = 10 \text{ V}$ ,  $V_{REFL} = 0 \text{ V}$ ,  $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ , unless otherwise noted.

Table 4.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
INTERFACE TIMING <sup>1</sup>						
Chip Select Write Pulse Width	$t_{WCS}$		35			ns
Chip Select Read Pulse Width	$t_{RCS}$		130			ns
Write Setup	$t_{WS}$		50			ns
Write Hold	$t_{WH}$		0			ns
Address Setup	$t_{AS}$		50			ns
Address Hold	$t_{AH}$		0			ns
Load Setup	$t_{LS}$		0			ns
Load Hold	$t_{LH}$		0			ns
Write Data Setup	$t_{WDS}$		50			ns
Write Data Hold	$t_{WDH}$		0			ns
Load Data Pulse Width	$t_{LDW}$		35			ns
Reset Pulse Width	$t_{RESET}$		35			ns
Read Data Hold	$t_{RDH}$		0			ns
Read Data Setup	$t_{RDS}$		0			ns
Data to Hi-Z	$t_{DZ}$	$C_L = 10 \text{ pF}$	80		100	ns
Chip Select to Data	$t_{CSD}$	$C_L = 10 \text{ pF}$	80		100	ns
Chip Select Repetitive Pulse Width	$t_{CSP}$		20			ns
Load Setup in Double Buffer Mode	$t_{LDS}$		35			ns
Load Data Hold	$t_{LDH}$		0			ns

<sup>1</sup> All input control signals are specified with  $t_R = t_F = 2 \text{ ns}$  (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

## ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Values
$V_{DD}$ to $V_{SS}$	-0.3 V to +18 V
$V_{DD}$ to GND	-0.3 V to +18 V
$V_{SS}$ to GND	+0.3 V to -9 V
$V_{DD}$ to $V_{REF+}$	-0.3 V to +18 V
$V_{REF-}$ to $V_{SS}$	-0.3 V to +18 V
$V_{REFH}$ to $V_{REFL}$	-0.3 V to +18 V
$DV_{DD}$ to GND	8 V
Logic Inputs to GND	$V_{SS} - 0.3$ V, $V_{DD} + 0.3$ V
$V_{OUT}$ to GND	$V_{SS} - 0.3$ V, $V_{DD} + 0.3$ V
$I_{OUT}$ Short Circuit to GND	24 mA
Thermal Resistance Junction to Ambient, $\theta_{JA}$	115°C/W
Thermal Resistance Junction to Case, $\theta_{JC}$	42°C/W
Maximum Junction Temperature ( $T_J$ Max)	150°C
Package Power Dissipation = $(T_J \text{ Max} - T_A)/\theta_{JA}$	
Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature	
RV-48 (Soldering, 60 secs)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

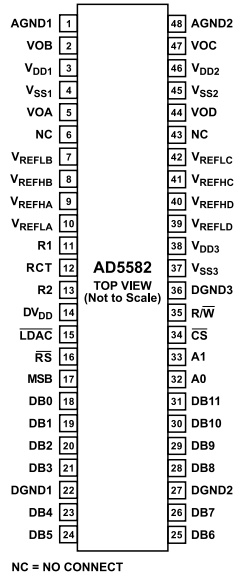


Figure 3. AD5582 Pin Configuration

Table 6. AD5582 Pin Function Descriptions

Pin No.	Mnemonic	Description <sup>1</sup>
1	AGND1	Analog Ground for DAC A and B
2	VOB	DAC B Output
3	V <sub>DD1</sub>	Positive Power Supply for DAC A and B
4	V <sub>SS1</sub>	Negative Power Supply for DAC A and B
5	VOA	DAC A Output
6	NC	No Connect
7	V <sub>REFLB</sub>	DAC B Voltage Reference Low Terminal
8	V <sub>REFHB</sub>	DAC B Voltage Reference High Terminal
9	V <sub>REFHA</sub>	DAC A Voltage Reference High Terminal
10	V <sub>REFLA</sub>	DAC A Voltage Reference Low Terminal
11	R1	R1 Terminal (for Negative Reference)
12	RCT	Center Tap Terminal (for Negative Reference)
13	R2	R2 Terminal (for Negative Reference)
14	DV <sub>DD</sub>	Power Supply for Digital Circuits
15	$\overline{\text{LDAC}}$	DAC Register Load, Active Low Level Sensitive
16	$\overline{\text{RS}}$	Reset Strobe
17	MSB	MSB = 0, Reset to 000 <sub>H</sub> . MSB = 1, Reset to 800 <sub>H</sub>
18	DB0	Data Bit 0
19	DB1	Data Bit 1
20	DB2	Data Bit 2
21	DB3	Data Bit 3
22	DGND1	Digital Ground 1
23	DB4	Data Bit 4
24	DB5	Data Bit 5
25	DB6	Data Bit 6
26	DB7	Data Bit 7
27	DGND2	Digital Ground 2
28	DB8	Data Bit 8
29	DB9	Data Bit 9



## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 6. AD5582 Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description <sup>1</sup>
30	DB10	Data Bit 10
31	DB11	Data Bit 11
32	A0	Address Input 0
33	A1	Address Input 1
34	$\overline{\text{CS}}$	Chip Select, Active Low
35	R/ $\overline{\text{W}}$	Read/Write Mode Select
36	DGND3	Digital Ground 3
37	V <sub>SS3</sub>	Negative Power Supply for Analog Switches
38	V <sub>DD3</sub>	Positive Power Supply for Analog Switches
39	V <sub>REFLD</sub>	DAC D Voltage Reference Low Terminal
40	V <sub>REFHD</sub>	DAC D Voltage Reference High Terminal
41	V <sub>REFHC</sub>	DAC C Voltage Reference High Terminal
42	V <sub>REFLC</sub>	DAC C Voltage Reference Low Terminal
43	NC	No Connect
44	VOD	DAC D Output
45	V <sub>SS2</sub>	Negative Power Supply for DAC C and D
46	V <sub>DD2</sub>	Positive Power Supply for DAC C and D
47	VOC	DAC C Output
48	AGND2	Analog Ground for DAC C and D

<sup>1</sup> The AD5582 optimizes internal layout design to reduce die area so that all supply voltage pins are required to be connected externally. See Figure 38.

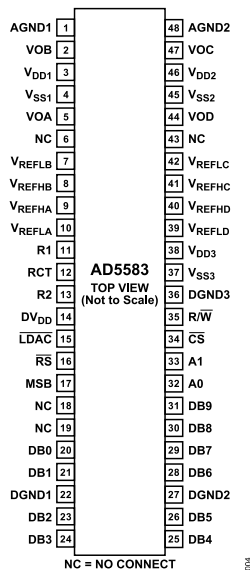


Figure 4. AD5583 Pin Configuration

Table 7. AD5583 Pin Function Descriptions

Pin No.	Mnemonic	Description <sup>1</sup>
1	AGND1	Analog Ground for DAC A and B
2	VOB	DAC B Output
3	V <sub>DD1</sub>	Positive Power Supply for DAC A and B
4	V <sub>SS1</sub>	Negative Power Supply for DAC A and B
5	VOA	DAC A Output
6	NC	No Connect (Do Not Connect Anything Other than Dummy Pad)

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 7. AD5583 Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description <sup>1</sup>
7	V <sub>REFLB</sub>	DAC B Voltage Reference Low Terminal
8	V <sub>REFHB</sub>	DAC B Voltage Reference High Terminal
9	V <sub>REFHA</sub>	DAC A Voltage Reference High Terminal
10	V <sub>REFLA</sub>	DAC A Voltage Reference Low Terminal
11	R1	R1 Terminal (for Negative Reference)
12	RCT	Center Tap Terminal (for Negative Reference)
13	R2	R2 Terminal (for Negative Reference)
14	DV <sub>DD</sub>	Power Supply for Digital Circuits
15	$\overline{\text{LDAC}}$	DAC Register Load, Active Low Level Sensitive
16	$\overline{\text{RS}}$	Reset Strobe
17	MSB	MSB = 0, Reset to 000 <sub>H</sub> MSB = 1, Reset to 200 <sub>H</sub>
18	NC	No Connect (Do Not Connect Anything Other than Dummy Pad)
19	NC	No Connect (Do Not Connect Anything Other than Dummy Pad)
20	DB0	Data Bit 0
21	DB1	Data Bit 1
22	DGND1	Digital Ground 1
23	DB2	Data Bit 2
24	DB3	Data Bit 3
25	DB4	Data Bit 4
26	DB5	Data Bit 5
27	DGND2	Digital Ground 2
28	DB6	Data Bit 6
29	DB7	Data Bit 7
30	DB8	Data Bit 8
31	DB9	Data Bit 9
32	A0	Address Input 0
33	A1	Address Input 1
34	$\overline{\text{CS}}$	Chip Select, Active Low
35	R/ $\overline{\text{W}}$	Read/Write Mode Select
36	DGND3	Digital Ground 3
37	V <sub>SS3</sub>	Negative Power Supply for Analog Switches
38	V <sub>DD3</sub>	Positive Power Supply for Analog Switches
39	V <sub>REFLD</sub>	DAC D Voltage Reference Low Terminal
40	V <sub>REFHD</sub>	DAC D Voltage Reference High Terminal
41	V <sub>REFHC</sub>	DAC C Voltage Reference High Terminal
42	V <sub>REFLC</sub>	DAC C Voltage Reference Low Terminal
43	NC	No Connect (Do Not Connect Anything Other than Dummy Pad)
44	VOD	DAC D Output
45	V <sub>SS2</sub>	Negative Power Supply for DAC C and D
46	V <sub>DD2</sub>	Positive Power Supply for DAC C and D
47	VOC	DAC C Output
48	AGND2	Analog Ground for DAC C and D

<sup>1</sup> The AD5583 optimizes internal layout design to reduce die area so that all supply voltage pins are required to be connected externally. See Figure 38.

TIMING DIAGRAMS

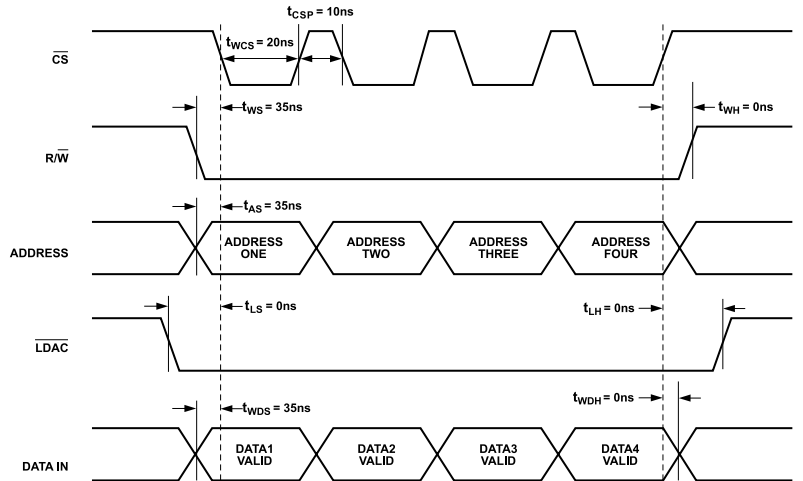


Figure 5. Single Buffer Mode, Output Updated Individually,  $DV_{DD} = 5\text{ V}$

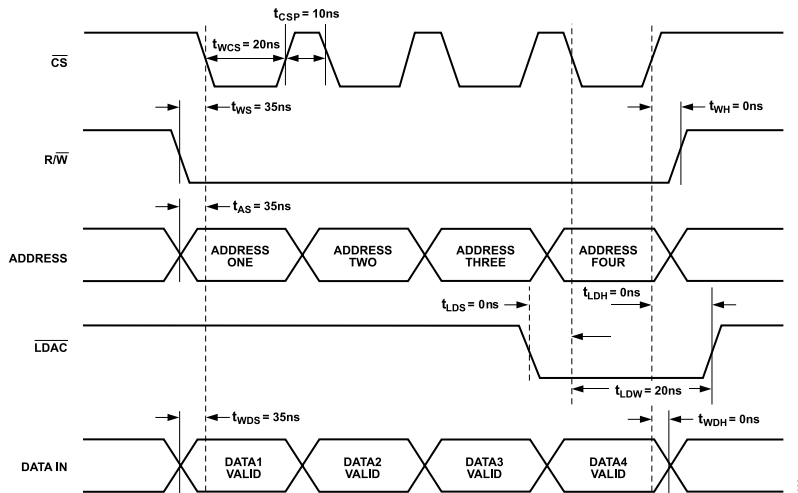


Figure 6. Double Buffer Mode, Output Updated Simultaneously,  $DV_{DD} = 5\text{ V}$

TIMING DIAGRAMS

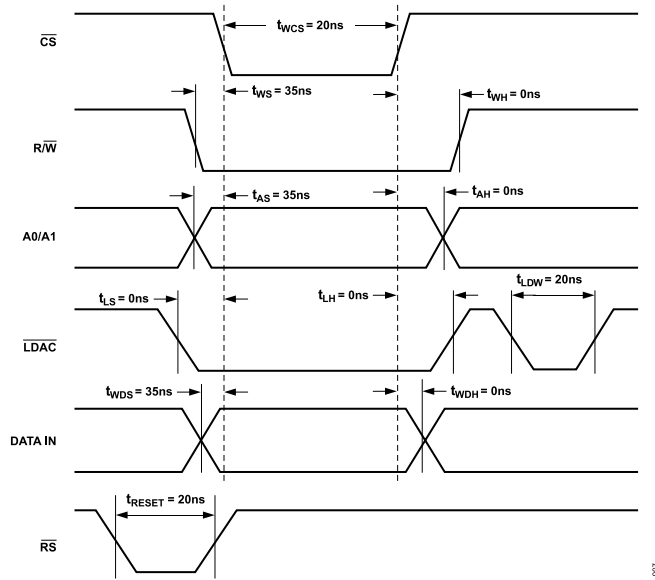


Figure 7. Data Write (Input and Output Registers) Timing

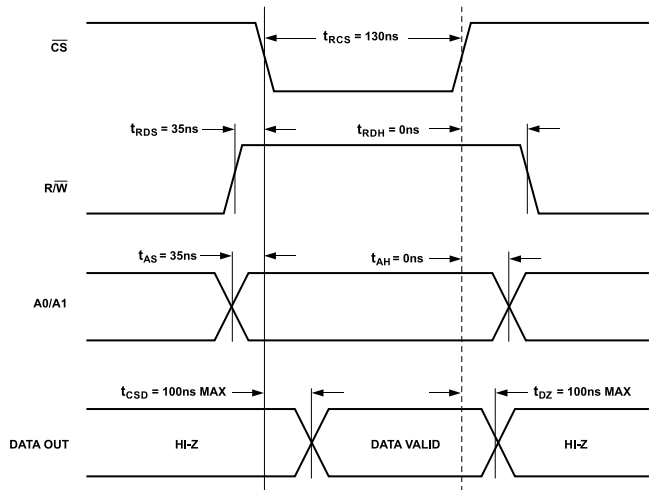


Figure 8. Data Output (Read Timing)

TYPICAL PERFORMANCE CHARACTERISTICS

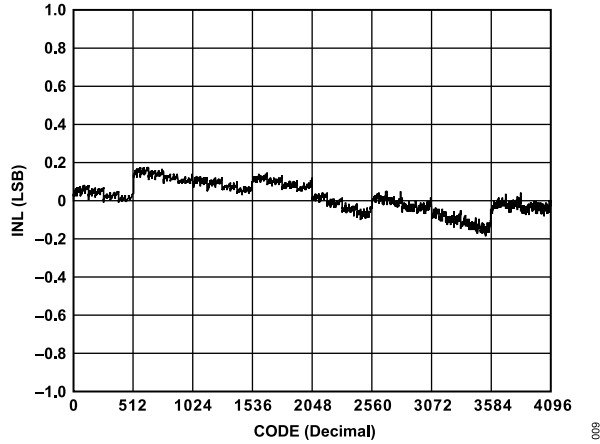


Figure 9. AD5582 Integral Nonlinearity Error

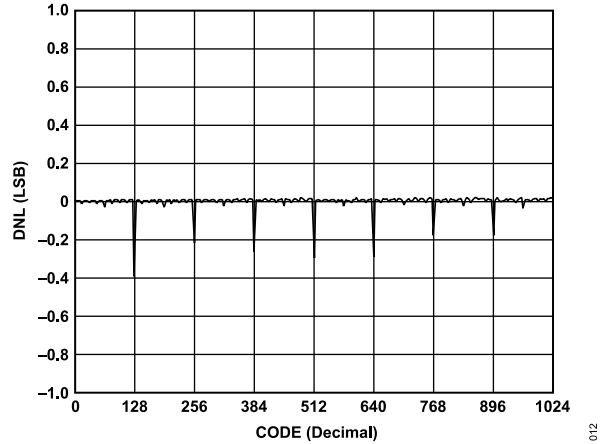


Figure 12. AD5583 Differential Nonlinearity Error

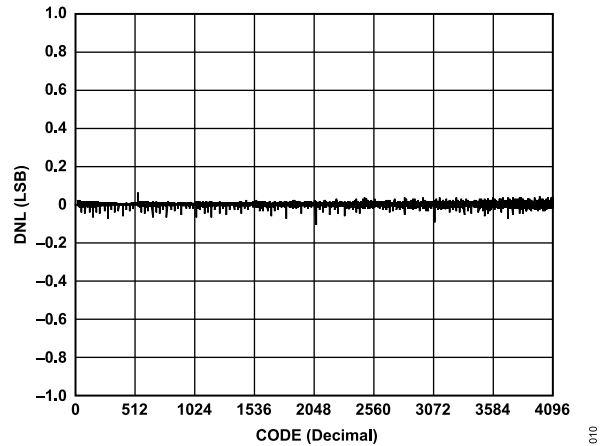


Figure 10. AD5582 Differential Nonlinearity Error

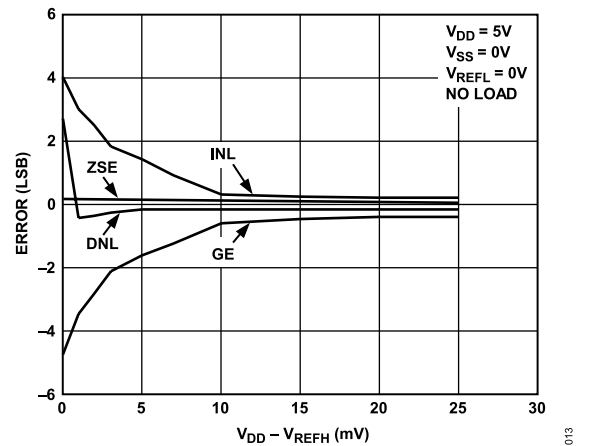


Figure 13. AD5582 INL, DNL, ZSE, and GE at Positive Rail-to-Rail Operation

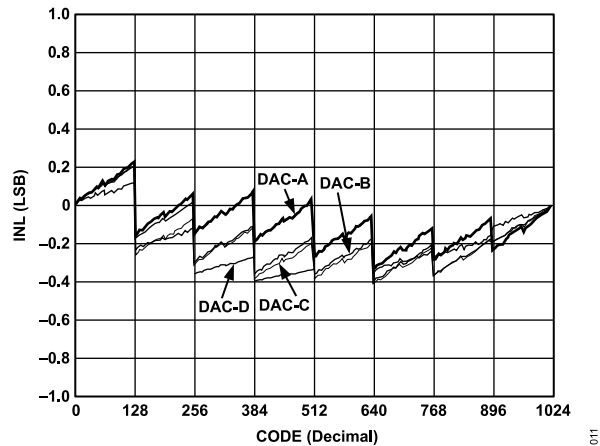


Figure 11. AD5583 Integral Nonlinearity Error

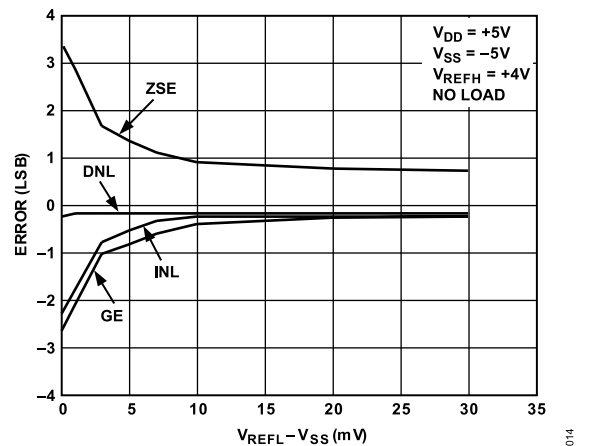


Figure 14. AD5582 INL, DNL, GE, and ZSE at Negative Rail-to-Rail Operation

TYPICAL PERFORMANCE CHARACTERISTICS

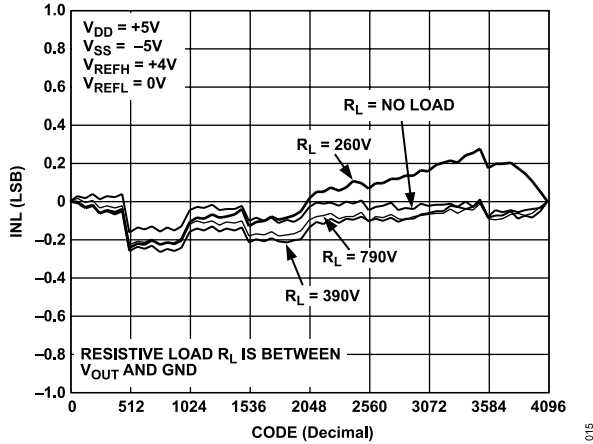


Figure 15. AD5582 INL at Various Resistive Loads

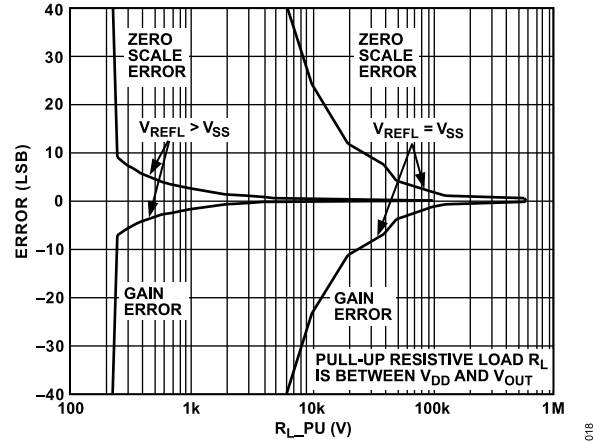


Figure 18. AD5582 Gain and Zero-Scale Error vs. Pull-Up Resistive Loads

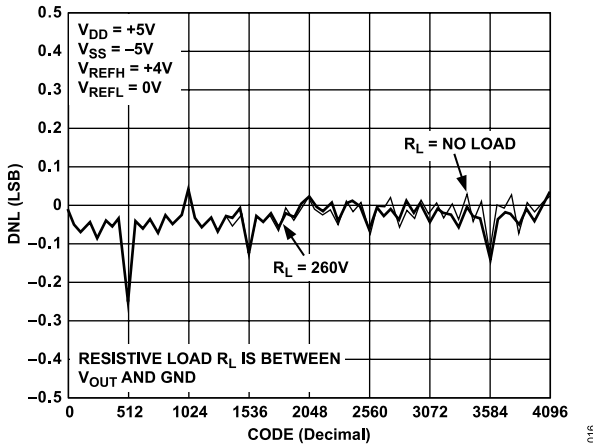


Figure 16. AD5582 DNL at Various Resistive Loads

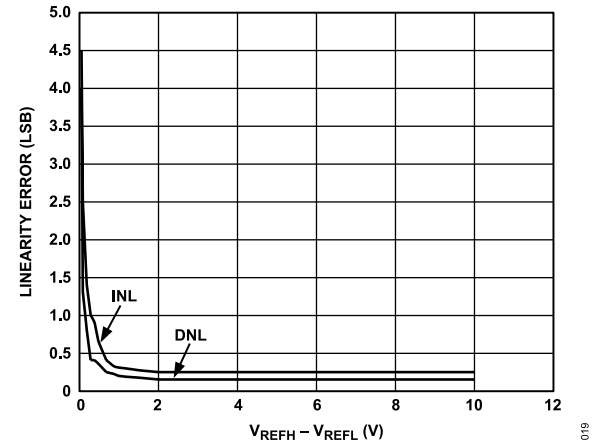


Figure 19. AD5582 Linearity Errors vs. Differential Reference Ranges

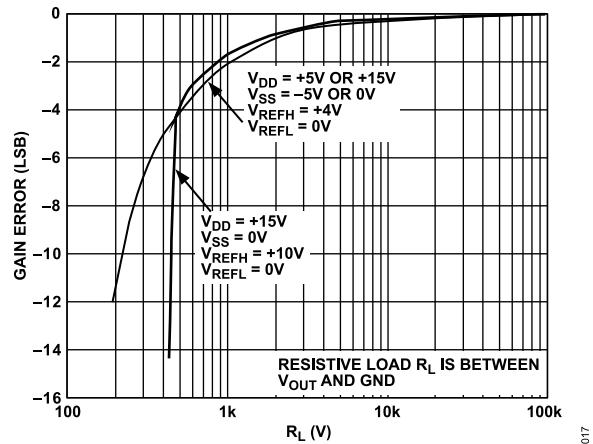


Figure 17. AD5582 Gain Error vs. Resistive Load

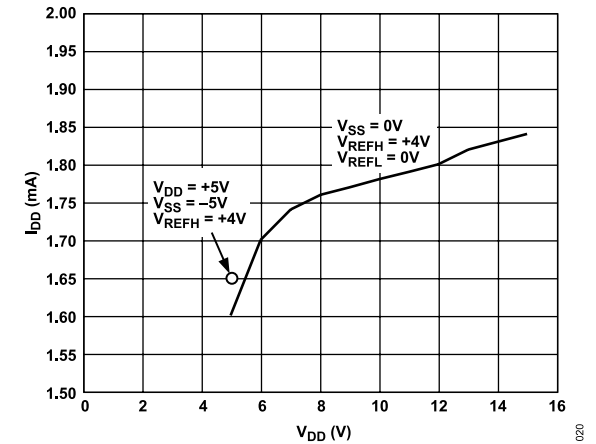


Figure 20. AD5582 Supply Current vs. Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

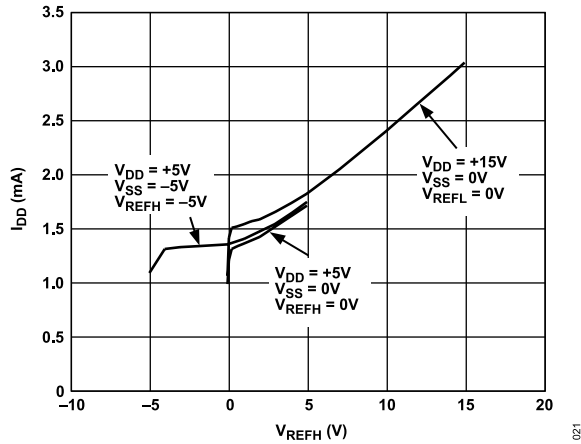


Figure 21. AD5582 Supply Current vs. Reference Voltage

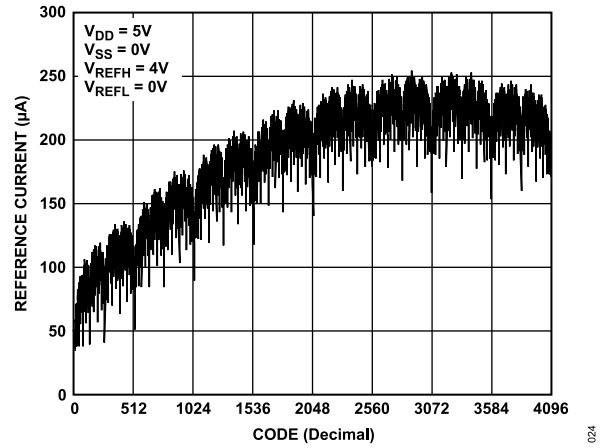


Figure 24. AD5582 Reference Current

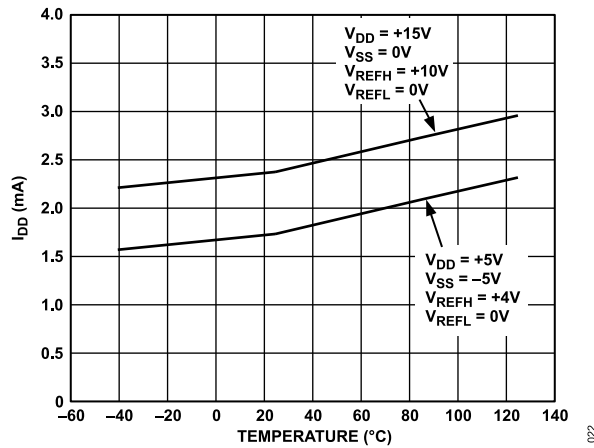


Figure 22. AD5582 Supply Current vs. Temperature

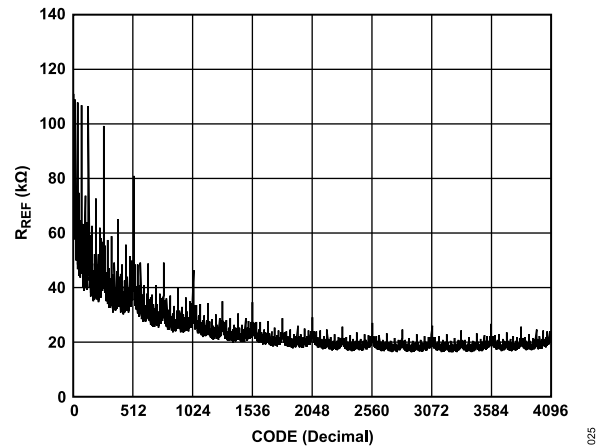


Figure 25. AD5582 Referenced Input Resistance

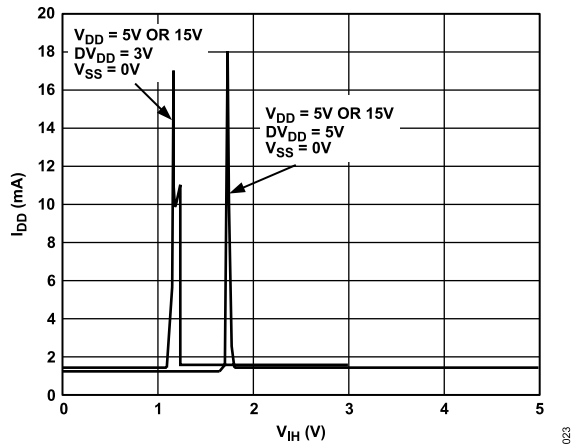


Figure 23. AD5582 Supply Current vs. Logic Input Voltage

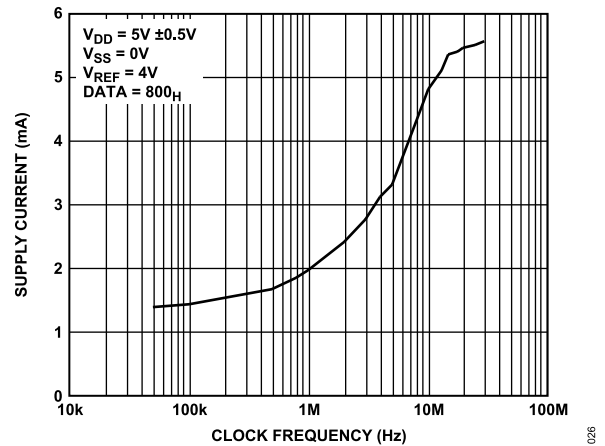


Figure 26. AD5582 Supply Current vs. Clock Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

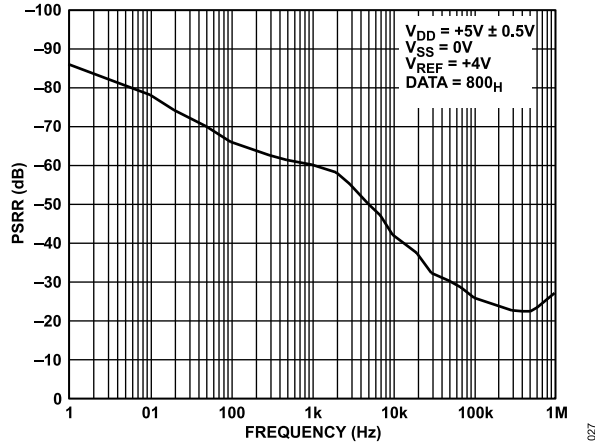


Figure 27. AD5582 PSRR vs. Frequency

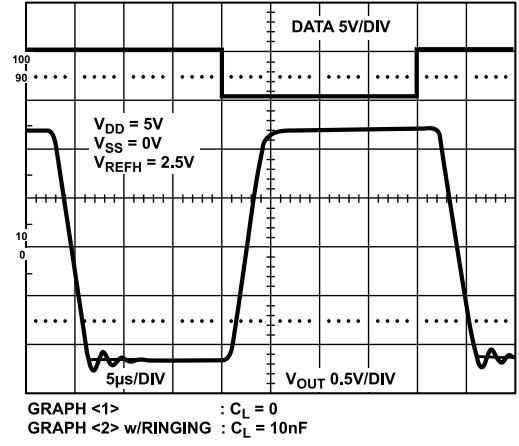


Figure 30. Large Signal Settling When Loaded (See Figure 35)

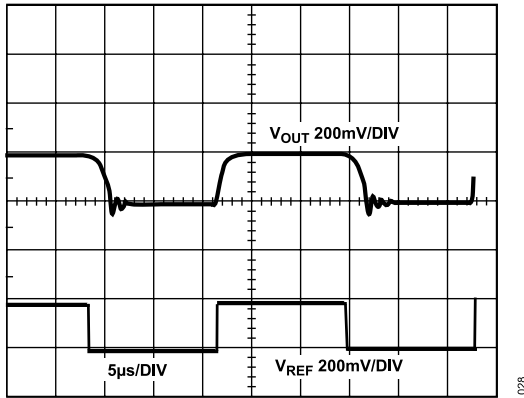


Figure 28. Small Signal Response Operating at Near Rail,  $C_L = 2 \text{ nF}$  (See Figure 35)

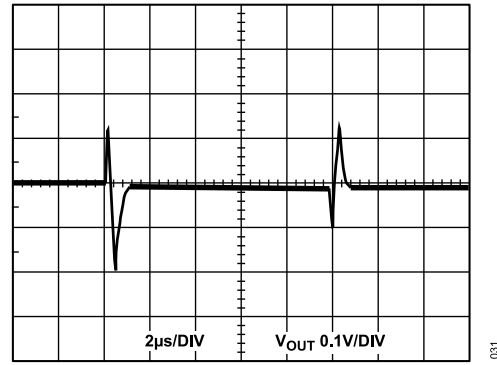


Figure 31. Midscale Transition Glitch

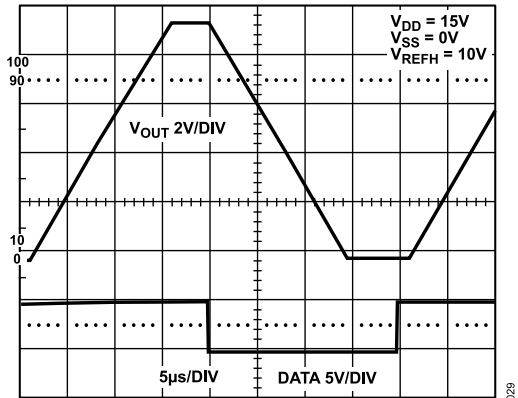


Figure 29. Large Signal Settling

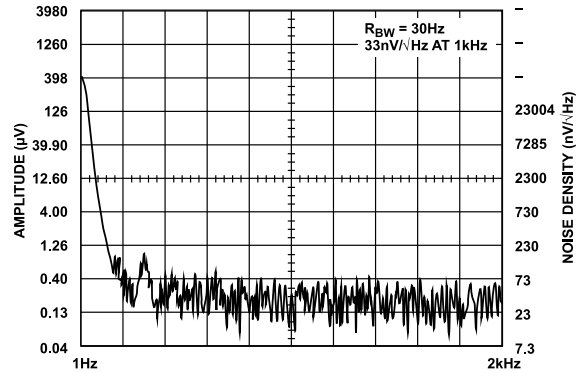


Figure 32. AD5582 Output Noise Density



TYPICAL PERFORMANCE CHARACTERISTICS

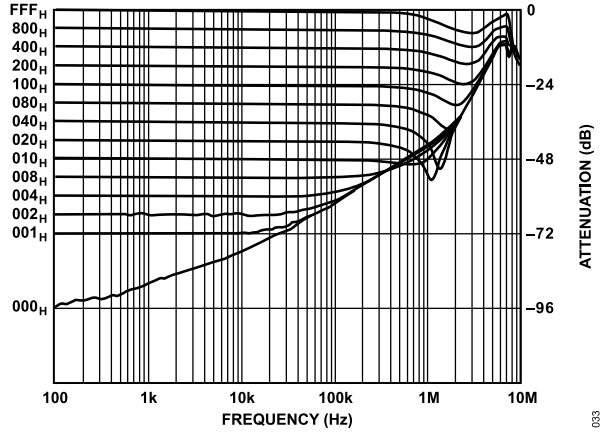


Figure 33. AD5582 Multiplying Bandwidth

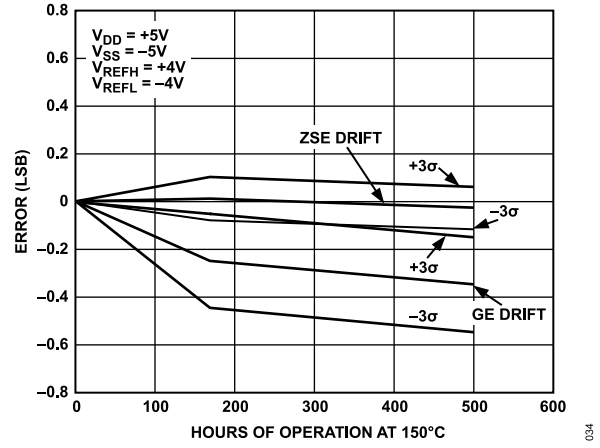


Figure 34. AD5582 Long-Term Drift

## TEST CIRCUIT

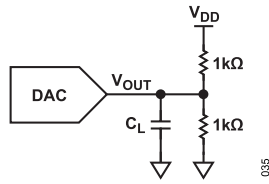


Figure 35. Test Circuit 1

## THEORY OF OPERATION

The AD5582/AD5583 are quad, voltage output, 12-/10-bit parallel input DACs in compact TSSOP-48 packages.

Each DAC is a voltage switching, high impedance ( $R = 20 \text{ k}\Omega$ ), R-2R ladder configuration with segmentation to optimize die area and precision. Figure 36 shows a simplified R-2R structure without the segmentation. The 2R resistances are switched between  $V_{REFH}$  and  $V_{REFL}$ , and the output is obtained from the rightmost ladder node. As the code is sequenced through all possible states, the voltage of this node changes in steps of  $(2/3 V_{REFH} - V_{REFL})/(2N - 1)$  starting from the lowest  $V_{REFL}$  and going to the highest  $V_{REFH} - \text{DUTLSB}$ . Buffering it with an amplifier with a gain of 1.5 brings the output to:

$$V_{OUT} = \frac{D}{2^N - 1} (V_{REFH} - V_{REFL}) + V_{REFL} \quad (1)$$

where  $D$  is the decimal equivalent of the data bits and  $N$  is the numbers of bits.

If  $-V_{REFL}$  is equal to  $V_{REFH}$  as  $V_{REF}$ ,  $V_{OUT}$  is simplified to:

(For AD5582)

$$V_{OUT} = \left( \frac{2D}{4095} - 1 \right) V_{REF} \quad (2)$$

(For AD5583)

$$V_{OUT} = \left( \frac{2D}{1023} - 1 \right) V_{REF} \quad (3)$$

The advantage of this scheme is that it allows the DAC to interpolate between two voltages for differential references or a single-ended reference.

These DACs feature double buffers, which allow both synchronous and asynchronous channels update with additional data readback capability. These parts can be reset to zero scale or midscale controlled by the  $\overline{RS}$  and MSB pins. When  $\overline{RS}$  is activated, the MSB of 0 resets the DACs to zero scale and the MSB of 1 resets the DACs to midscale. The ability to operate from wide supply voltages, +5 V to +15 V or  $\pm 5 \text{ V}$ , with multiplying bipolar references is another key feature of these DACs.

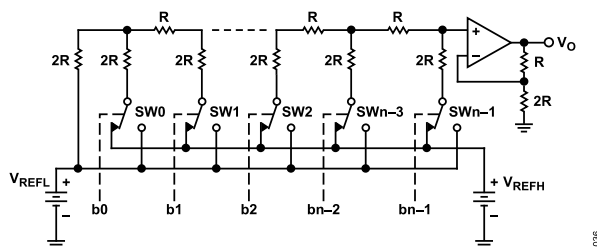


Figure 36. Simplified R-2R Architecture (Segmentation Not Shown)

## POWER SUPPLIES

There are three separate power supplies needed for the operation of the DACs. For dual supply,  $V_{SS}$  can be set from  $-6.5 \text{ V}$  to  $-2.7 \text{ V}$  and  $V_{DD}$  can be set from  $+2.7 \text{ V}$  to  $+6.5 \text{ V}$ . For single supply,  $V_{SS}$

should be set at  $0 \text{ V}$  while  $V_{DD}$  is set from  $3 \text{ V}$  to  $16.5 \text{ V}$ . However, setting the single supply of  $V_{DD}$  below  $4.5 \text{ V}$  can impact the overall accuracy of the device.

Since these DACs can be operated at high voltages, the digital signal levels are therefore controlled separately by the provision of  $DV_{DD}$ .  $DV_{DD}$  can be set as low as  $2.7 \text{ V}$  but no greater than  $6.5 \text{ V}$ . This allows the DAC to be operable from low level digital signals generated from a wide range of microcontrollers, FPGA, and signal processors.

## REFERENCE INPUT

All four channels of DACs allow independent and differential reference voltages. The flexibility of independent references allows users to apply a unique reference voltage to each channel. Similarly, bipolar references can be applied across the differential references. To maintain optimum accuracy, the difference between  $V_{REFH}$  and  $V_{REFL}$  should be greater than  $1 \text{ V}$ . See Figure 19.

The voltages applied to these reference inputs set the output voltage limits of all four channels of the DACs, and  $V_{REFH}$  must always be higher than  $V_{REFL}$ .  $V_{REFH}$  can be set at any voltage from  $V_{REFL} + 0.5 \text{ V}$  to  $V_{DD}$ , while  $V_{REFL}$  can be set at any voltage from  $V_{SS}$  to  $V_{REFH} - 0.5 \text{ V}$ . In addition, a symmetrical negative reference can be generated easily by an external op amp in an inverting mode with a pair of built-in precision resistors, R1 and R2. These resistors are matched within  $\pm 0.025\%$  for the AD5582 and  $0.1\%$  for the AD5583, which is equivalent to less than 1 LSB mismatch. Figure 37 shows a simple configuration.

Common reference or references can be applied to all four channels, but each reference pin should be decoupled with a  $0.1 \mu\text{F}$  ceramic capacitor mounted close to the pin.

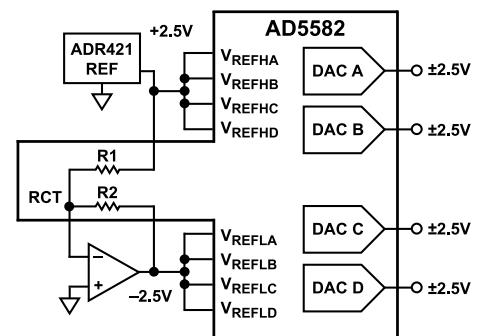


Figure 37. Using On-Board Matching Resistors to Generate a Negative Voltage REF

## DIGITAL I/O

Digital I/O consists of a 12-/10-bit bidirectional data bus, two register select inputs, A0 and A1, an R/W input, a reset ( $\overline{WR}$ ), a chip select ( $\overline{CS}$ ), and a load DAC (LDAC) input. Control of the DACs and the bus direction is determined by these inputs as shown in Table 8. All digital pins are TTL/CMOS compatible and all internal registers are level triggered.

## THEORY OF OPERATION

The register selects inputs A0 and A1. Decoding of the registers is enabled by the  $\overline{CS}$  input. When  $\overline{CS}$  is high, no decoding is taking place and neither the writing nor the reading of the input registers is enabled. The loading of the second bank of registers is controlled by the asynchronous  $\overline{LDAC}$  input. By taking  $\overline{LDAC}$  low while  $\overline{CS}$  is enabled, the individual channel is updated as single buffer mode (see Figure 5). If  $\overline{CS}$  is enabled sequentially to load data into all input registers, then a subsequent  $\overline{LDAC}$  pulse will allow all channels to be updated simultaneously as double buffer mode (see Figure 6).

$\overline{RW}$  controls the writing to and reading from the input register.

## RESET

The  $\overline{RS}$  function can be used either at power-up or at any time during operation. The  $\overline{RS}$  function has priority over any other digital inputs. This pin is active low and sets the DAC output registers to either zero scale or midscale, determined by the state of the MSB. The reset to midscale is useful when the DAC is configured for bipolar references and the output will be reset to 0 V.

## OUTPUT AMPLIFIERS

Unlike many voltage output DACs, the AD5582/AD5583 feature buffered voltage outputs with high output current driving capability. Each output is capable of both sourcing and sinking  $\pm 20$  mA, eliminating the need for external buffers when driving any capacitive loads without oscillation. These amplifiers also have short circuit protection.

## GLITCH

The worst-case glitch of the AD5582 occurs at the transitions between midscale ( $1000\ 0000\ 0000_B$ ) to midscale minus 1 ( $0111\ 1111\ 1111_B$ ), or vice versa. The glitch energy is measured as  $100\ \text{mV} \times 1\ \mu\text{s}$  or equivalent to  $100\ \text{nV}\cdot\text{s}$ . Such glitch occurs in a shorter duration than the settling time and therefore most applications will be immune to such an effect without a deglitcher.

## LAYOUT AND POWER SUPPLY BYPASSING

It is a good practice to employ compact, minimum lead length PCB layout design. The leads to the input should be as short as possible to minimize IR drop and stray inductance.

It is also essential to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with  $0.01\ \mu\text{F}$  to  $0.1\ \mu\text{F}$  disc or chip ceramics capacitors. Low ESR  $1\ \mu\text{F}$  to  $10\ \mu\text{F}$  tantalum or electrolytic capacitors should also be applied at the supplies to minimize transient disturbance. The AD5582/AD5583 optimize internal layout design to reduce die area so that all analog supply pins are required to be connected externally. See Figure 38.

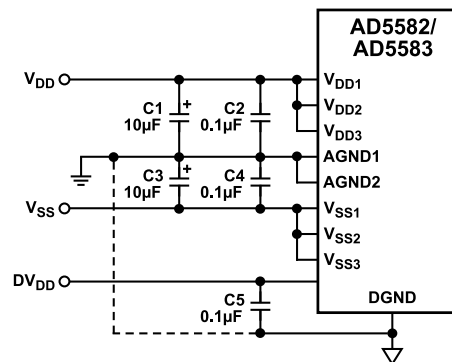


Figure 38. Power Supply Configurations

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## APPLICATIONS INFORMATION

## PROGRAMMABLE CURRENT SOURCE

The high current capability of the AD5582/AD5583 allows them to be used directly in programmable current source applications, such as 4 mA to 20 mA current transmitters and other general purpose applications. For higher compliance voltage that is higher than 15 V, Figure 39 shows a versatile V-I conversion circuit using

an improved Howland Current Pump. In addition to the precision current conversion it provides, this circuit enables a bidirectional current flow and high voltage compliance. The voltage compliance is mainly limited by the op amp supply voltages. This circuit can be used in 4 mA to 20 mA current transmitters with up to 500  $\Omega$  of load.

Table 8. AD5582/AD5583 Logic Table

A1	A0	R/W	CS	LDAC	RS	Input Register	DAC Register	Operation Mode	Selected DAC
0	0	0	0	0	1	Write	Transparent	Transparent <sup>1</sup>	A
0	1	0	0	0	1	Write	Transparent	Transparent <sup>1</sup>	B
1	0	0	0	0	1	Write	Transparent	Transparent <sup>1</sup>	C
1	1	0	0	0	1	Write	Transparent	Transparent <sup>1</sup>	D
0	0	0	0	1	1	Write	Hold	Write Input	A
0	1	0	0	1	1	Write	Hold	Write Input	B
1	0	0	0	1	1	Write	Hold	Write Input	C
1	1	0	0	1	1	Write	Hold	Write Input	D
0	0	1	0	1	1	Read	Hold	Readback to D0 to DN	A
0	1	1	0	1	1	Read	Hold	Readback to D0 to DN	B
1	0	1	0	1	1	Read	Hold	Readback to D0 to DN	C
1	1	1	0	1	1	Read	Hold	Readback to D0 to DN	D
X <sup>2</sup>	X <sup>2</sup>	X <sup>2</sup>	1	0	1	Hold	Update All Registers	Update All Registers	All
X <sup>2</sup>	X <sup>2</sup>	X <sup>2</sup>	1	1	1	Hold	Hold	Hold	All
X <sup>2</sup>	X <sup>2</sup>	X <sup>2</sup>	X <sup>2</sup>	X <sup>2</sup>	0	All registers reset to midscale or zero scale. <sup>3</sup>			All
X <sup>2</sup>	X <sup>2</sup>	X <sup>2</sup>	1	X <sup>2</sup>	↑	All registers latched to midscale or zero scale.			All

<sup>1</sup> Input and output registers are transparent when asserted.

<sup>2</sup> X: Don't care.

<sup>3</sup> MSB = 0 resets to zero scale, MSB = 1 resets to midscale.

## APPLICATIONS INFORMATION

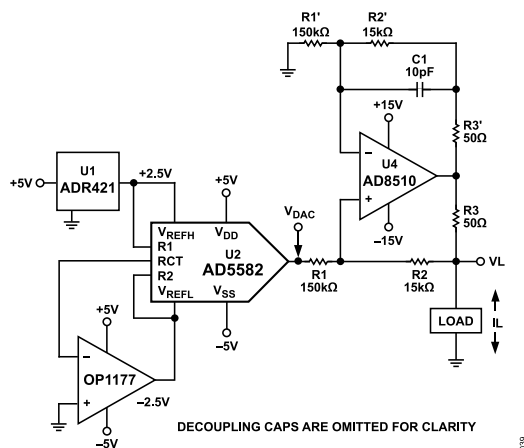


Figure 39. Programmable Current Source with Bidirectional Current Control and High Voltage Compliance Capabilities

Figure 39 shows that if the resistor network is matched, the load current is:

$$I_L = \frac{(R_2 + R_3)/R_1}{R_3} V_{DAC} \quad (4)$$

$R_3$  in theory can be made small to achieve the current needed within the U4 output current driving capability. In this circuit, the AD8510 can deliver  $\pm 20$  mA in both directions and the voltage compliance approaches  $\pm 15$  V.

This circuit is versatile, but users must pay attention to the compensation. Without C1, it can be shown that the output impedance becomes:

$$Z_O = \frac{R_1' R_3 (R_1 + R_2)}{R_1 (R_2' + R_3') - R_1' (R_2 + R_3)} \quad (5)$$

If the resistors are perfectly matched,  $Z_O$  is infinite, which is highly desirable. On the other hand, if they are not matched,  $Z_O$  can either be positive or negative. The latter, because of the pole in the right S-plane, can cause oscillation. As a result, C1 in the range of a few pF is needed to prevent the oscillation. For critical applications, C1 should be found empirically without overcompensating.

## BOOSTED PROGRAMMABLE VOLTAGE SOURCE

For users who need higher than 20 mA current driving capability, they can add an external op amp and power transistors. The capacitive loading capability will change, but it can still drive 100 nF capacitive load without oscillation in this circuit. Figure 40 shows a programmable power supply with 200 mA capability.

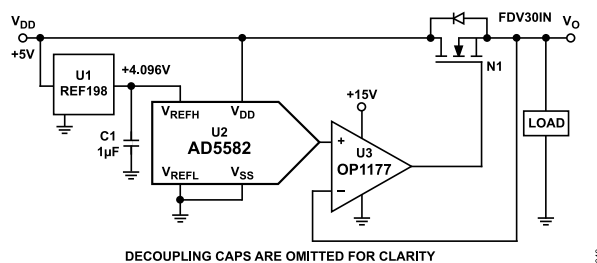
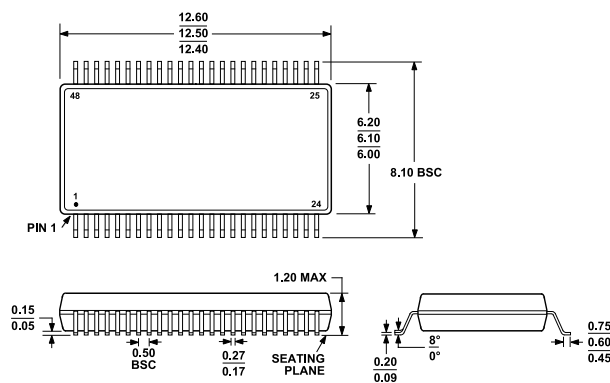


Figure 40. Boosted Programmable Voltage Source

In this circuit, the inverting input of the op amp forces the  $V_O$  to be equal to the DAC output. The load current is then delivered by the supply via the N-Ch FET N1. U3 needs to be a rail-to-rail input type. With a  $V_{DD}$  of 5 V, this circuit can source a maximum of 200 mA at 4.096 V full scale, 100 mA at midscale, and 50 mA near zero-scale outputs. Higher current can be achieved with N1 in a larger package mounted on a heat sink.



## OUTLINE DIMENSIONS



**Figure 42. 48-Lead Thin Shrink Small Outline Package [TSSOP]  
(RV-48)**

*Dimensions shown in millimeters*

Updated: January 04, 2023

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
AD5582YRVZ	-40°C to +125°C	48-Lead TSSOP	RV-48
AD5583YRVZ	-40°C to +125°C	48-Lead TSSOP	RV-48

<sup>1</sup> Z = RoHS Compliant Part.