

FEATURES

- Two Matched 12-Bit DACs on One Chip
- Direct Parallel Load of All 12 Bits for High Data Throughput
- Double-Buffered Digital Inputs
- 12-Bit Endpoint Linearity ($\pm 1/2$ LSB) Over Temperature
- +5V to +15V Single Supply Operation
- DACs Matched to 1% Max
- Four-Quadrant Multiplication
- Improved ESD Resistance
- Packaged in a Narrow 0.3" 24-Pin DIP and 0.3" 24-Pin SOL package
- Available in Die Form

APPLICATIONS

- Automatic Test Equipment
- Robotics/Process Control/Automation
- Digital Gain/Attenuation Control
- Ideal for Battery-Operated Equipment

ORDERING INFORMATION [†]

RELATIVE ACCURACY (+5V or +15V)	GAIN ERROR (+5V or +15V)	PACKAGE		
		MILITARY* TEMPERATURE -55°C to +125°C	INDUSTRIAL TEMPERATURE -40°C to +85°C	COMMERCIAL TEMPERATURE 0°C to +70°C
$\pm 1/2$ LSB	± 1 LSB	DAC8222AW	DAC8222EW	-
$\pm 1/2$ LSB	± 2 LSB	-	-	DAC8222GP
± 1 LSB	± 4 LSB	-	DAC8222FW	DAC8222HP
± 1 LSB	± 4 LSB	-	DAC8222FP	DAC8222HS

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

[†] Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages.

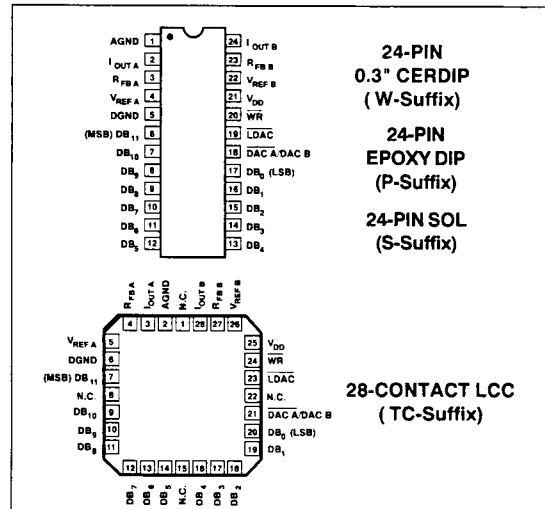
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

GENERAL DESCRIPTION

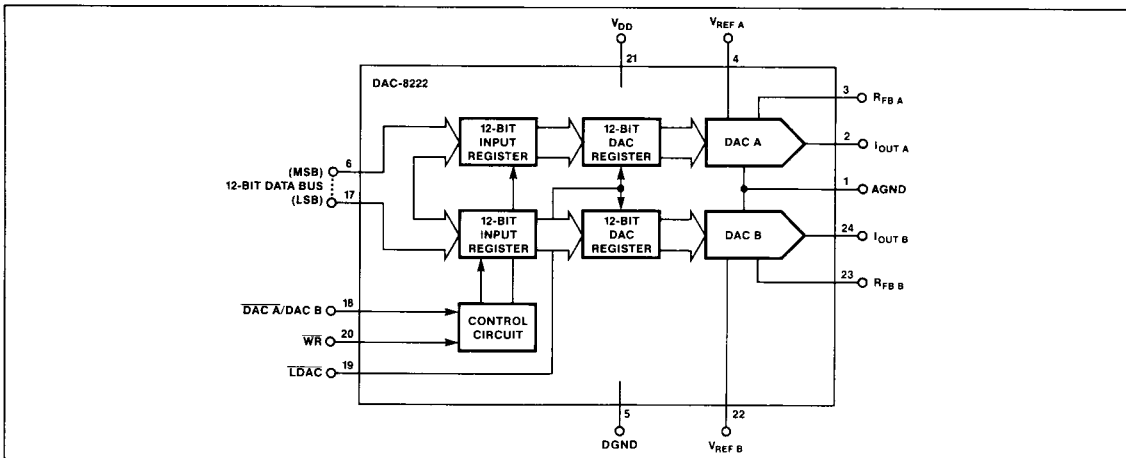
The DAC-8222 is a dual 12-bit, double-buffered, CMOS digital-to-analog converter. It has a 12-bit wide data port that allows a 12-bit word to be loaded directly. This achieves faster throughput time in stand-alone systems or when interfacing to a 16-bit processor. A common 12-bit input TTL/CMOS compatible data port is used to load the 12-bit word into either of the two DACs. This port, whose data loading is similar to that of a RAM's write cycle, interfaces directly with most 12-bit and 16-bit bus systems. (See PMI's DAC-8248 for a complete 8-bit data bus interface product.) A common bus allows the DAC-8222 to be packaged in a narrow 24-pin 0.3" DIP and save PCB space.

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PIN CONNECTIONS



FUNCTIONAL DIAGRAM



DAC-8222

The DAC is controlled with two signals, \overline{WR} and \overline{LDAC} . With logic low at these inputs, the DAC registers become transparent. This allows direct unbuffered data to flow directly to either DAC output selected by $\overline{DAC A}/\overline{DAC B}$. Also, the DAC's double-buffered digital inputs will allow both DACs to be updated simultaneously.

DAC-8222's monolithic construction offers excellent DAC-to-DAC matching and tracking over the full operating temperature range. The chip consists of two thin-film R-2R resistor ladder networks, four 12-bit registers, and DAC control logic circuitry. The device has separate reference-input and feedback resistors for each DAC and operates on a single supply from +5V to +15V. Maximum power dissipation at +5V using zero or V_{DD} logic levels is less than 0.5mW.

The DAC-8222 is manufactured with PMI's highly stable thin-film resistors on an advanced oxide-isolated, silicon-gate, CMOS technology. PMI's improved latch-up resistant design eliminates the need for external protective Schottky diodes.

ABSOLUTE MAXIMUM RATINGS

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

V_{DD} to AGND	0V, +17V
V_{DD} to DGND	0V, +17V
AGND to DGND	-0.3V, $V_{DD} + 0.3V$
Digital Input Voltage to DGND	-0.3V, $V_{DD} + 0.3V$
$I_{OUT A}$, $I_{OUT B}$ to AGND	-0.3V, $V_{DD} + 0.3V$

ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$ or $+15V$, $V_{REF A} = V_{REF B} = +10V$, $V_{OUT A} = V_{OUT B} = 0V$; AGND = DGND = 0V; T_A = Full Temp Range Specified in Absolute Maximum Ratings; unless otherwise noted. Specifications apply for DAC A and DAC B.

PARAMETER	SYMBOL	CONDITIONS	DAC-8222			UNITS
			MIN	TYP	MAX	
STATIC ACCURACY						
Resolution	N		12	—	—	Bits
Relative Accuracy	INL	Endpoint Linearity Error				
			DAC-8222A/E/G	—	—	$\pm 1/2$
			DAC-8222F/H	—	—	± 1
Differential Nonlinearity	DNL	All Grades are Guaranteed Monotonic	—	—	± 1	LSB
Full Scale Gain Error (Note 1)	G_{FSE}	DAC-8222A/E DAC-8222G DAC-8222F/H	—	—	± 1 ± 2 ± 4	LSB
Gain Temperature Coefficient $\Delta\text{Gain}/\Delta\text{Temperature}$	TCG_{FS}	(Notes 2, 7)	—	± 2	± 5	ppm/ $^\circ\text{C}$
Output Leakage Current $I_{OUT A}$ (Pin 2), $I_{OUT B}$ (Pin 24)	I_{LKG}	All Digital Inputs = 0000 0000 0000	$T_A = +25^\circ\text{C}$ $T_A = \text{Full Temp. Range}$	± 5 —	± 10 ± 50	nA
Input Resistance ($V_{REF A}$, $V_{REF B}$)	R_{REF}	(Note 9)	8	11	15	k Ω
Input Resistance Match	$\frac{\Delta R_{REF}}{R_{REF}}$		—	± 0.2	± 1	%
DIGITAL INPUTS						
Digital Input High	V_{INH}	$V_{DD} = +5V$ $V_{DD} = +15V$	2.4 13.5	—	—	V
Digital Input Low	V_{INL}	$V_{DD} = +5V$ $V_{DD} = +15V$	—	—	0.8 1.5	V
Input Current	I_{IN}	$V_{IN} = 0V$ or V_{DD} and V_{INL} or V_{INH}	$T_A = +25^\circ\text{C}$ $T_A = \text{Full Temp. Range}$	± 0.001 —	± 1 ± 10	μA
Input Capacitance (Note 2)	C_{IN}	DB0-DB11 \overline{WR} , \overline{LDAC} , $\overline{DAC A}/\overline{DAC B}$	—	—	10 15	pF

$V_{REF A}$, $V_{REF B}$ to AGND	$\pm 25V$
$V_{RFB A}$, $V_{RFB B}$ to AGND	$\pm 25V$
Operating Temperature Range	
AW Version	-55°C to $+125^\circ\text{C}$
EW, FW, FP Versions	-40°C to $+85^\circ\text{C}$
GP, HP, HS Versions	-0°C to $+70^\circ\text{C}$
Junction Temperature	$+150^\circ\text{C}$
Storage Temperature	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec.)	$+300^\circ\text{C}$

PACKAGE TYPE	θ_{JA} (NOTE 1)	θ_{JC}	UNITS
24-Pin Hermetic DIP (W)	89	10	$^\circ\text{C}/\text{W}$
24-Pin Plastic DIP (P)	62	32	$^\circ\text{C}/\text{W}$
24-Pin SOL (S)	72	24	$^\circ\text{C}/\text{W}$

NOTES:

1. θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for CerDIP, and P-DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOL package.

CAUTION:

- Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and R_{FB} .
- The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
- Do not insert this device into powered sockets; remove power before insertion or removal.
- Use proper anti-static handling procedures.
- Devices can suffer permanent damage and/or reliability degradation if stressed above the limits listed under Absolute Maximum Ratings for extended periods.

ELECTRICAL CHARACTERISTICS at $V_{DD} = +5V$ or $+15V$, $V_{REF A} = V_{REF B} = +10V$, $V_{OUT A} = V_{OUT B} = 0V$; $AGND = DGND = 0V$;
 $T_A =$ Full Temp Range specified in Absolute Maximum Ratings; unless otherwise noted. Specifications apply for DAC A and DAC B.
Continued

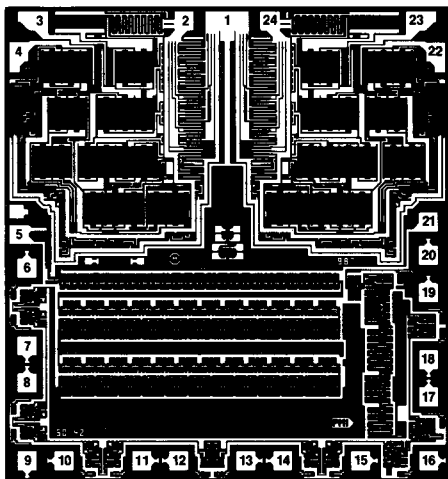
PARAMETER	SYMBOL	CONDITIONS	DAC-8222			UNITS
			MIN	TYP	MAX	
POWER SUPPLY						
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH}	-	-	2	mA
		All Digital Inputs $0V$ or V_{DD}	-	10	100	μA
DC Power Supply Rejection Ratio (Gain/ ΔV_{DD})	PSRR	$\Delta V_{DD} = \pm 5\%$	-	-	0.002	%/%
AC PERFORMANCE CHARACTERISTICS (Note 2)						
Propagation Delay (Notes 4, 5)	t_{PD}	$T_A = +25^\circ C$	-	-	350	ns
Current Settling Time (Notes 5, 6)	t_s	$T_A = +25^\circ C$	-	-	1	μs
Output Capacitance	C_O	Digital Inputs = All 0s $C_{OUT A}, C_{OUT B}$	-	-	90	pF
		Digital Inputs = All 1s $C_{OUT A}, C_{OUT B}$	-	-	120	
AC Feedthrough at $I_{OUT A}$ or $I_{OUT B}$	FT_A	$V_{REF A}$ to $I_{OUT A}$; $V_{REF A} = 20V_{P-P}$; $f = 100kHz$; $T_A = +25^\circ C$	-	-	-70	dB
	FT_B	$V_{REF B}$ to $I_{OUT B}$; $V_{REF B} = 20V_{P-P}$; $f = 100kHz$; $T_A = +25^\circ C$	-	-	-70	
SWITCHING CHARACTERISTICS (Notes 2, 3)			$V_{DD} = +5V$		$V_{DD} = +15V$	
			+25°C	-40°C TO +85°C (Note 8)	-55°C TO +125°C	ALL TEMPS (Note 10)
DAC Select to Write Set-Up Time	t_{AS}		150	180	210	60 ns MIN
DAC Select to Write Hold Time	t_{AH}		0	0	0	0 ns MIN
LDAC to Write Set-Up Time	t_{LS}		80	100	120	60 ns MIN
LDAC to Write Hold Time	t_{LH}		20	20	20	20 ns MIN
Data Valid to Write Set-Up Time	t_{DS}		220	240	260	100 ns MIN
Data Valid to Write Hold Time	t_{DH}		0	0	0	10 ns MIN
Write Pulse Width	t_{WR}		130	160	170	90 ns MIN
LDAC Pulse Width	t_{LWD}		100	120	130	60 ns MIN

NOTES:

- Measured using internal $R_{FB A}$ and $R_{FB B}$. Both DAC digital inputs = 1111 1111 1111.
- Guaranteed and not tested.
- See timing diagram.
- From 50% of digital input to 90% of final analog output current. $V_{REF A} = V_{REF B} = +10V$; $OUT A, OUT B$ load = 100Ω , $C_{EXT} = 13pF$.
- WR, LDAC = $0V$; DB0 - DB11 = $0V$ to V_{DD} or V_{DD} to $0V$.
- Settling time is measured from 50% of the digital input change to where the output voltage settles within 1/2 LSB of full scale.
- Gain TC is measured from $+25^\circ C$ to T_{MIN} or from $+25^\circ C$ to T_{MAX} .
- These limits apply for the commercial and industrial grade products.
- Absolute temperature coefficient is approximately $+50ppm/^\circ C$.
- These limits also apply as typical values for $V_{DD} = +12V$ with $+5V$ CMOS logic levels and $T_A = +25^\circ C$.

DAC-8222

DICE CHARACTERISTICS



DIE SIZE 0.124 × 0.132 Inch, 16,368 sq. mils
(3.15 × 3.55 mm, 10.56 sq. mm)

- | | |
|-----------------------|------------------------|
| 1. AGND | 13. DB4 |
| 2. I _{OUT A} | 14. DB3 |
| 3. R _{FB A} | 15. DB2 |
| 4. V _{REF A} | 16. DB1 |
| 5. DGND | 17. DB0(LSB) |
| 6. DB11(MSB) | 18. DAC A/DAC B |
| 7. DB10 | 19. LDAC |
| 8. DB9 | 20. WR |
| 9. DB8 | 21. V _{DD} |
| 10. DB7 | 22. V _{REF B} |
| 11. DB6 | 23. R _{FB B} |
| 12. DB5 | 24. I _{OUT B} |

Substrate (die backside) is internally connected to V_{DD}.

WAFER TEST LIMITS at V_{DD} = +5V or +15V, V_{REF A} = V_{REF B} = +10V, V_{OUT A} = V_{OUT B} = 0V; AGND = DGND = 0V; T_A = 25°C.

PARAMETER	SYMBOL	CONDITIONS	DAC-8222G	
			LIMIT	UNITS
Relative Accuracy	INL	Endpoint Linearity Error	±1	LSB MAX
Differential Nonlinearity	DNL	All Grades are Guaranteed Monotonic	±1	LSB MAX
Full Scale Gain Error (Note 1)	G _{FSE}	Digital Inputs = 1111 1111 1111	±4	LSB MAX
Output Leakage (I _{OUT A} , I _{OUT B})	I _{LKG}	Digital Inputs = 0000 0000 0000 Pad 2 and 24	±50	nA MAX
Input Resistance (V _{REF A} , V _{REF B})	R _{REF}	Pad 4 and 22	8/15	kΩ MIN/ kΩ MAX
Input Resistance Match	$\frac{\Delta R_{REF}}{R_{REF}}$		±1	% MAX
Digital Input High	V _{INH}	V _{DD} = +5V V _{DD} = +15V	2.4 13.5	V MIN
Digital Input Low	V _{INL}	V _{DD} = +5V V _{DD} = +15V	0.8 1.5	V MAX
Digital Input Current	I _{IN}	V _{IN} = 0V or V _{DD} ; V _{INL} or V _{INH}	±1	μA MAX
Supply Current	I _{DD}	All Digital Inputs V _{INL} or V _{INH} All Digital Inputs 0V or V _{DD}	2 0.1	mA MAX
DC Supply Rejection (ΔGain/ΔV _{DD})	PSR	ΔV _{DD} = ±5%	0.002	%/% MAX

NOTES:

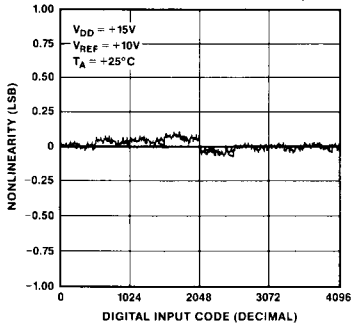
1. Measured using internal R_{FB A} and R_{FB B}.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

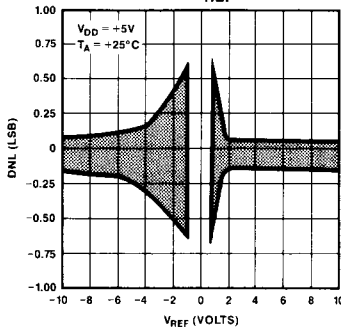
TYPICAL PERFORMANCE CHARACTERISTICS

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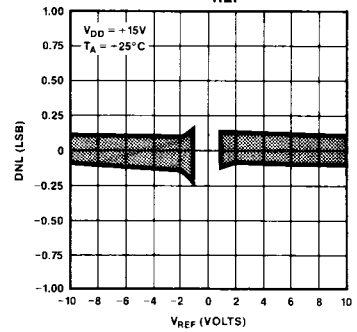
CHANNEL-TO-CHANNEL MATCHING (DAC A & B ARE SUPERIMPOSED)



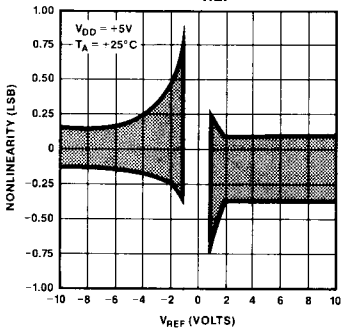
DIFFERENTIAL NONLINEARITY vs V_{REF}



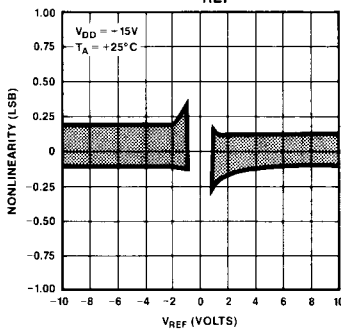
DIFFERENTIAL NONLINEARITY vs V_{REF}



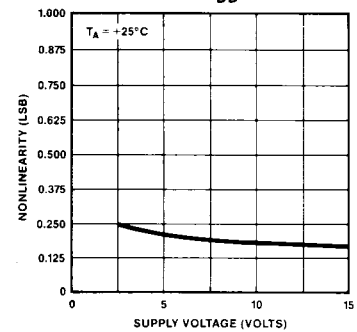
NONLINEARITY vs V_{REF}



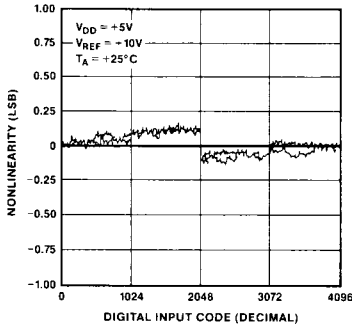
NONLINEARITY vs V_{REF}



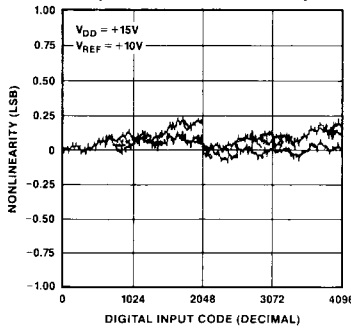
NONLINEARITY vs V_{DD}



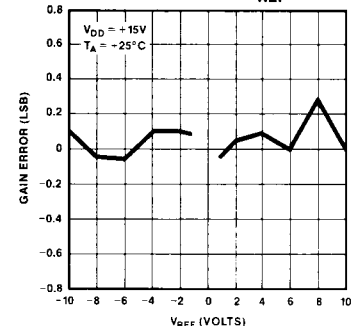
NONLINEARITY vs CODE (DAC A & B ARE SUPERIMPOSED)



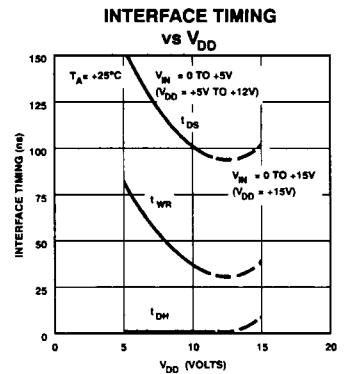
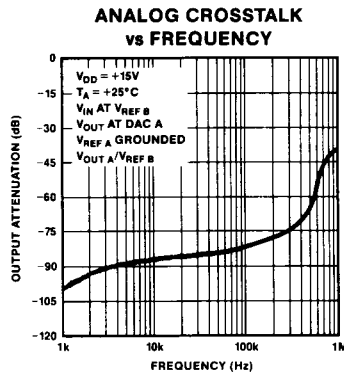
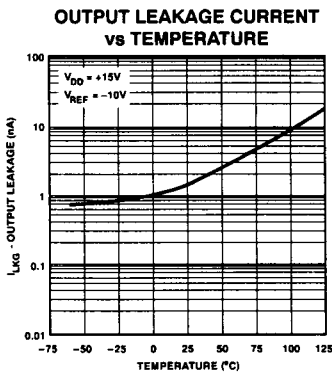
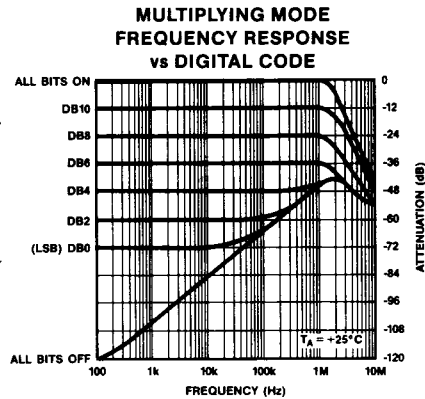
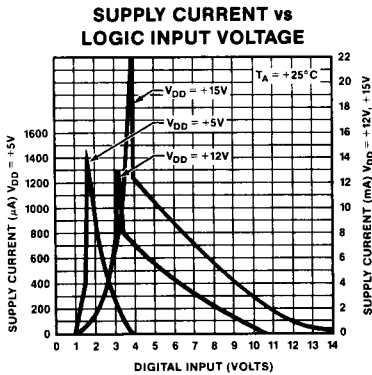
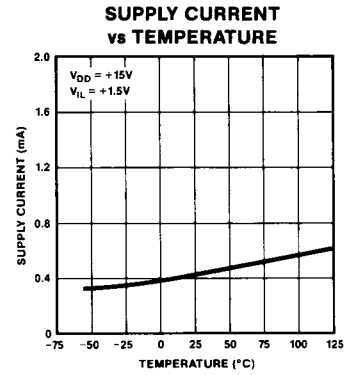
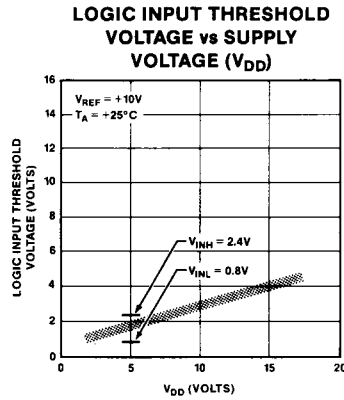
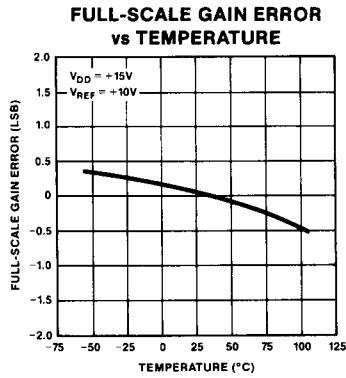
NONLINEARITY vs CODE AT $T_A = -55^\circ C, +25^\circ C, +125^\circ C$ FOR DAC A & B (ALL SUPERIMPOSED)



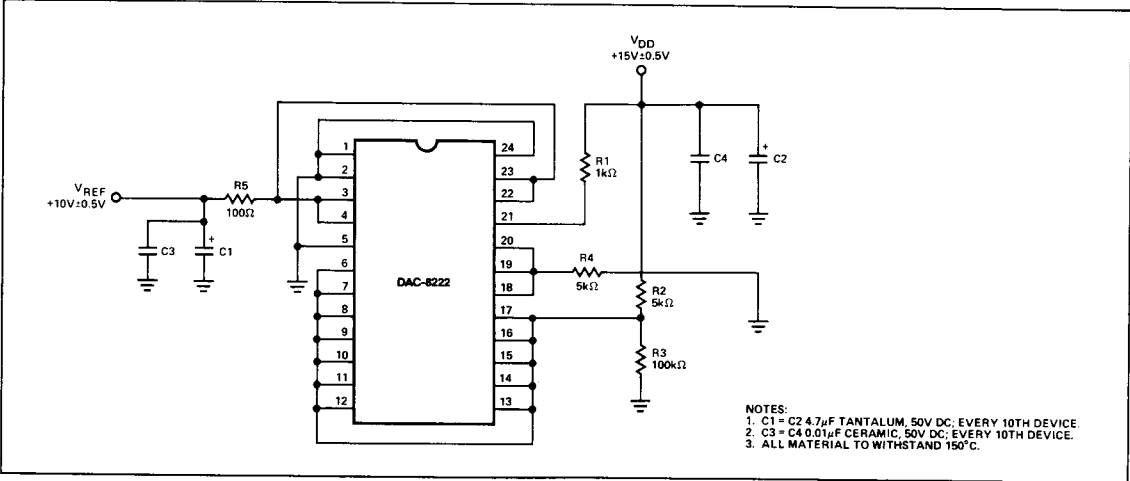
ABSOLUTE GAIN ERROR CHANGE vs V_{REF}



TYPICAL PERFORMANCE CHARACTERISTICS



BURN-IN CIRCUIT



2

PARAMETER DEFINITIONS

RESOLUTION (n)

The resolution of a DAC is the number of states (2^n) that the full-scale range (FSR) is divided (or resolved) into; where n is equal to the number of bits.

RELATIVE ACCURACY (INL)

Relative accuracy, or integral nonlinearity, is the maximum deviation of the analog output (from the ideal) from a straight line drawn between the end points. It is expressed in terms of least significant bit (LSB), or as a percent of full scale.

DIFFERENTIAL NONLINEARITY (DNL)

Differential nonlinearity is the worst case deviation of any adjacent analog output from the ideal 1 LSB step size. The deviation of the actual "step size" from the ideal step size of 1 LSB is called the differential nonlinearity error or DNL. DACs with DNL greater than ± 1 LSB may be nonmonotonic. $\pm 1/2$ LSB INL guarantees monotonicity and ± 1 LSB maximum DNL.

GAIN ERROR (G_{FSE})

Gain error is the difference between the actual and the ideal analog output range, expressed as a percent of full-scale or in terms of LSB value. It is the deviation in slope of the DAC transfer characteristic from ideal.

See Orientation in Digital-to-Analog Converters Section of the current data book, for additional parameter definitions.

GENERAL CIRCUIT DESCRIPTION

CONVERTER SECTION

The DAC-8222 contains four 12-bit registers (two input registers and two DAC registers), two highly-stable thin-film R-2R resistor ladder networks, and interface control logic circuitry. Also included are 24 single-pole, double-throw, NMOS transistor current switches.

FIGURE 1: Simplified Single DAC Circuit Configuration. (Switches Are Shown For All Digital Inputs At Zero)

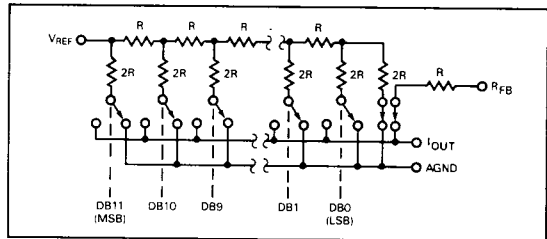


FIGURE 2: N-Channel Current Steering Switch

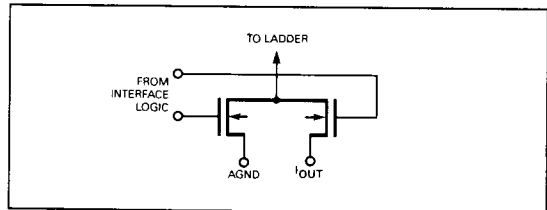


Figure 1 shows a simplified circuit for the R-2R ladder network and transistor switches for one DAC. R is typically 11kΩ. The transistor switches are binary scaled in size to maintain a constant voltage drop across each switch. Figure 2 shows a single NMOS transistor switch.

The binary-weighted currents are switched between I_{OUT} and AGND by the N-channel MOS transistor switches. The selection between I_{OUT} and AGND is determined by the digital input code. It is important to note here that the voltage difference

DAC-8222

between I_{OUT} and AGND terminals be as close to zero as practical in order to keep DAC errors to a minimum. This is normally done by connecting AGND to the noninverting input of an op amp and I_{OUT} to the inverting input. The DAC's internal resistor (R_{FB}) can be used for the feedback resistor by connecting the op amp's output directly to the DAC's R_{FB} terminal. The op amp also provides the current-to-voltage conversion for the DAC's output current. The output voltage is dependent on the DAC's digital input code and V_{REF} , and is given by:

$$V_{OUT} = -V_{REF} \times D/4096$$

where D is the digital input code integer number that is between 0 and 4095.

The DAC's input resistance, V_{REF} (Figure 1), is always equal to a constant value, R. This means that V_{REF} can be driven by a reference voltage or current, AC or DC (positive or negative). It is recommended that a low-temperature-coefficient external R_{FB} resistor be used if a current source is employed.

The DAC's output capacitance (C_{OUT}) is code dependent and varies from 90pF (all digital inputs low) to 120pF (all digital inputs high).

Figure 1 shows a transistor switch in series with the R-2R ladder terminating resistor and R_{FB} resistor. They were designed into the DAC to binarily match the ladder leg switches and improve power supply rejection and gain error temperature coefficient. The gates of these transistor switches are connected to V_{DD} , so that an "open-circuit" exists when V_{DD} is not applied. This means that an op amp's output voltage will go to either "rail" if powered up before the DAC. Also, R_{FB} resistance cannot be measured without V_{DD} being applied.

FIGURE 3: Digital Input Structure For One Bit

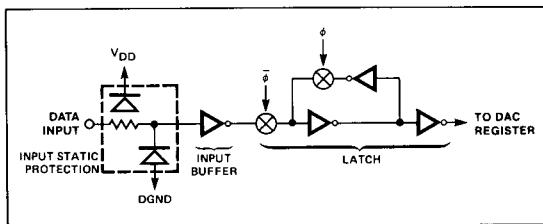
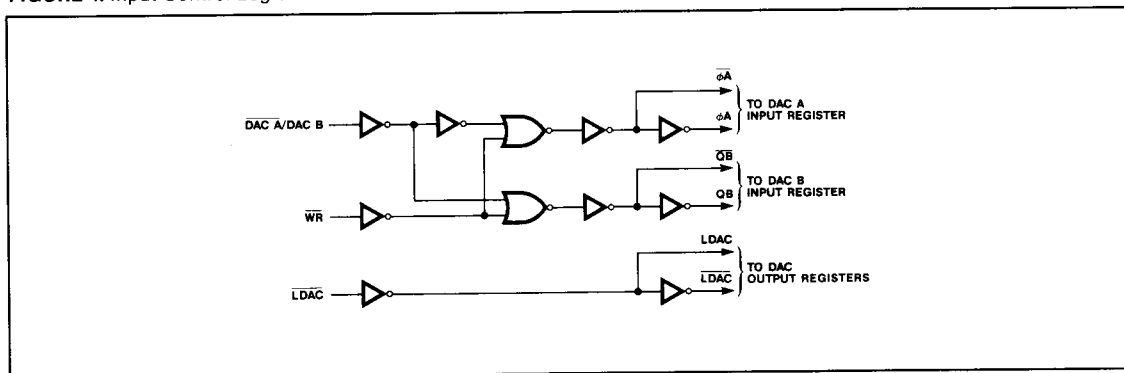


FIGURE 4: Input Control Logic



DIGITAL SECTION

The DAC-8222's digital inputs are CMOS inverters. They were designed to convert TTL and CMOS input logic levels into voltage levels to drive the internal circuitry. The digital inputs are TTL compatible at $V_{DD} = +5V$ and CMOS compatible at $V_{DD} = +15V$. The DAC-8222 can use +5V CMOS logic levels with $V_{DD} = +12V$; however, supply current will rise to approximately 5-6mA.

Figure 3 shows the DAC's digital input register structure for one bit. This circuit drives the DAC register. Digital controls ϕ and $\bar{\phi}$ shown are generated from DAC A/DAC B and WR control signals.

As shown in Figure 3, these inputs are electrostatic-discharge protected with two internal distributed diodes; they are connected between V_{DD} and DGND. Each digital input has a typical input current of less than 1nA.

When the digital inputs are in the region of +1.2V to +2.8V (peaking at +1.8V) using a +5V power supply, or in the region of +1.7V to +12V (peaking at +3.9V) with a +15V power supply, the input register transistors are operating in their linear region and draw current from the power supply. It is, therefore, recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible to keep supply currents at a minimum. The DAC-8222 may be operated with any supply voltage between the range of +5V to +15V.

INTERFACE CONTROL LOGIC

The DAC-8222's input control logic circuitry is shown in Figure 4. Note how the WR signal is used in conjunction with DAC A/DAC B to load data into either input register. LDAC loads data from the input registers to the DAC register; the DAC's analog output voltage is determined by the data contained in each DAC register.

The truth table for the DAC registers is shown in the Mode Selection Table. Note how the input register is transparent when \overline{WR} is low and \overline{LDAC} is high, and that the DAC register is transparent when WR is high and LDAC is low (LDAC updates the DAC's analog output voltage). The DAC is transparent from input to output when WR and LDAC are both low, and the DAC is latched (input and output is not being updated) when WR and LDAC are both high.

MODE SELECTION TABLE

DIGITAL INPUTS			REGISTER STATUS			
DAC A/B	WR	LDAC	DAC A		DAC B	
			INPUT REGISTER	DAC REGISTER	INPUT REGISTER	DAC REGISTER
L	L	L	WRITE	WRITE	LATCHED	WRITE
H	L	L	LATCHED	WRITE	WRITE	WRITE
L	L	H	WRITE	LATCHED	LATCHED	LATCHED
H	L	H	LATCHED	LATCHED	WRITE	LATCHED
X	H	L	LATCHED	WRITE	LATCHED	WRITE
X	H	H	LATCHED	LATCHED	LATCHED	LATCHED

L = Low H = High X = Don't Care

INTERFACE CONTROL LOGIC

DAC A/DAC B (Pin 18)–DAC Selection. Active low for DAC A and active high for DAC B.

WR (Pin 20)–WRITE. Active Low. Used to write data into either DAC A or DAC B input registers, or active high latches data into the input registers.

LDAC (Pin 19)–LOAD DAC. Active Low. Used to simultaneously transfer data from DAC A and DAC B input registers to both DAC outputs. The DAC becomes transparent (activity on the digital inputs appear at the analog output) when both WR and LDAC are low. Data is latched into the output registers on the rising edge of LDAC.

WRITE TIMING CYCLES

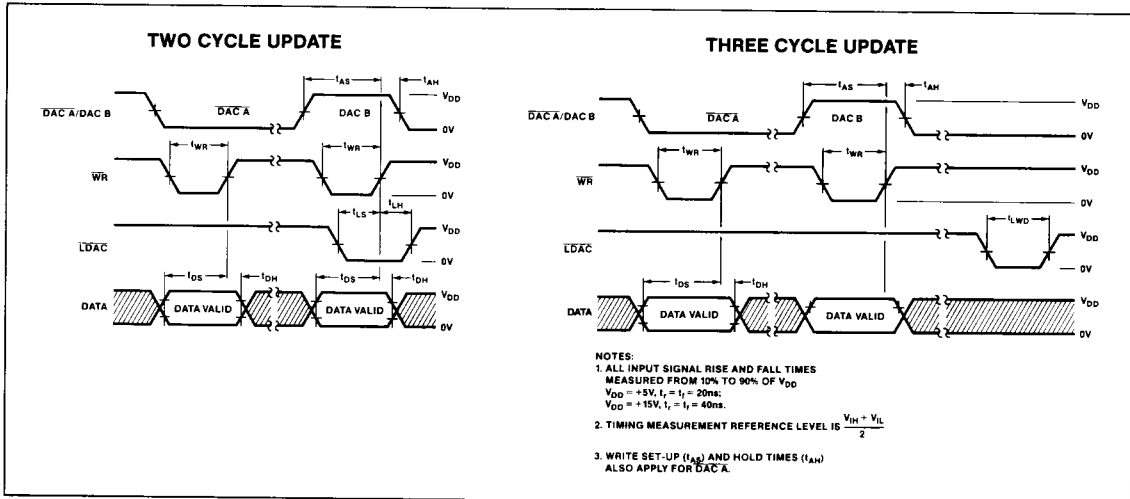
Two timing diagrams are shown and are at the user's discretion which to use.

The TWO CYCLE UPDATE, as the name implies, allows both DAC registers to be loaded and the outputs updated in two cycles. Data is first loaded into one DAC's input register on the first write cycle, and then new data loaded into the other DAC's input register while simultaneously updating both DAC outputs on the second cycle.

The THREE CYCLE UPDATE allows DAC A and DAC B registers to be loaded and analog output to be updated at a later time. The first two cycles load both DACs as above, and the third cycle updates the outputs.

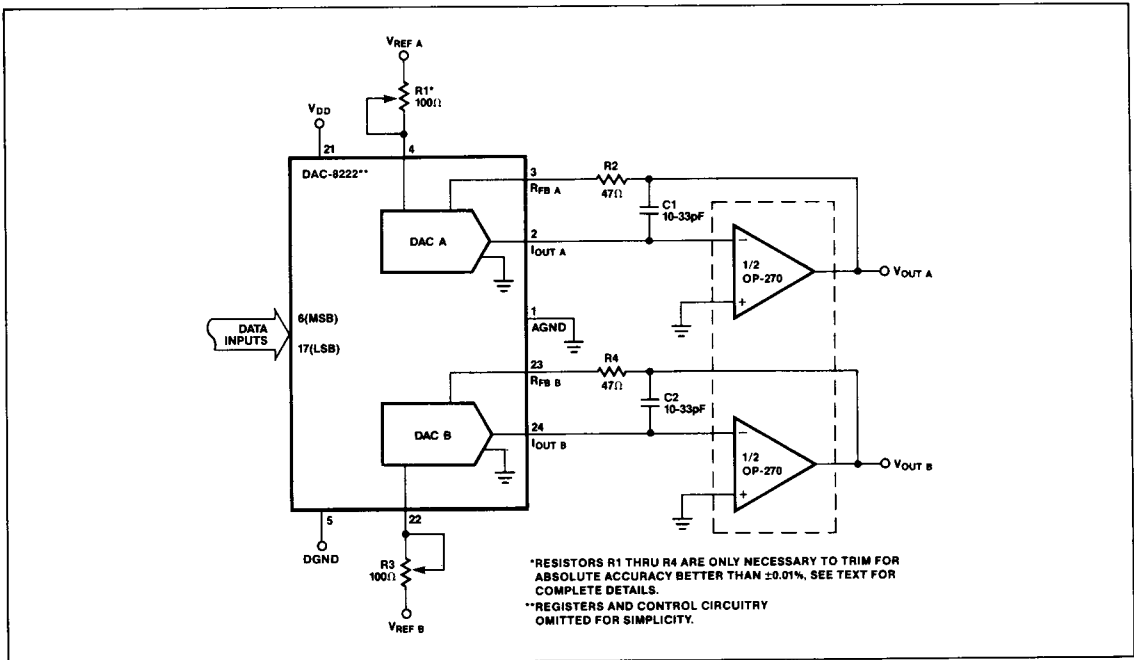
The LDAC and DAC A/DAC B control pins can be tied together and controlled with a single strobe. When using the DAC in this configuration, DAC B must be loaded first.

WRITE CYCLE TIMING DIAGRAM



DAC-8222

FIGURE 5: Unipolar Configuration (2-Quadrant Multiplication)



APPLICATIONS INFORMATION

UNIPOLAR OPERATION

Figure 5 shows a simple unipolar (2-quadrant multiplication) circuit using the DAC-8222 and OP-270 dual op amp (use two OP-42s for higher speeds), and Table 1 the corresponding code table. Resistors R1, R2, and R3, R4 are used only if full-scale gain adjustments are required. Low-temperature coefficient (approximately 50 ppm/°C) resistors or trimmers should be used. Maximum full-scale error without these resistors for the top grade device and $V_{REF} = \pm 10V$ is 0.024% and 0.097% for the low grade. C1 and C2 provide phase compensation to help reduce overshoot and ringing when high-speed op amps are used.

Full-scale adjustment is accomplished by loading the digital inputs with all 1s and adjusting R1 (or R3) so that

$$V_{OUT} = V_{REF} \times \left(\frac{4095}{4096} \right)$$

Full-scale can also be adjusted by varying V_{REF} voltage, thus eliminating R1, R2, R3 and R4. Zero adjustment is performed by setting the DAC's digital inputs to all 0s and adjusting the op amp's offset adjust so that $V_{OUT} = 0V$. To maintain monotonicity and minimize gain and linearity errors, it is recommended that the op amp offset voltage be adjusted to less than 10% of 1 LSB (244 μV) over the operating temperature range of interest.

TABLE 1: Unipolar Binary Code Table (Refer to Figure 5)

BINARY NUMBER IN DAC REGISTER		ANALOG OUTPUT, V_{OUT} (DAC A or DAC B)
MSB	LSB	
1111	1111 1111	$-V_{REF} \left(\frac{4095}{4096} \right)$
1000	0000 0000	$-V_{REF} \left(\frac{2048}{4096} \right) = -1/2V_{REF}$
0000	0000 0001	$-V_{REF} \left(\frac{1}{4096} \right)$
0000	0000 0000	0V

NOTE:

$$1 \text{ LSB} = (2^{-12}) (V_{REF}) = \frac{1}{4096} (V_{REF})$$

BIPOLAR OPERATION

The bipolar (offset binary) 4-quadrant operation configuration using the DAC-8222 is shown in Figure 6 and the corresponding code in Table 2. The circuit makes use of the OP-470, a quad op amp (use four OP-42s for higher speeds).

Resistors R1, R2, R3, and R4 may be omitted and full-scale output voltage may be adjusted by varying V_{REF} or the value of R5 and R8. If resistors R1, R2, R3, and R4 are omitted, then

FIGURE 6: Bipolar Configuration (4-Quadrant Multiplication)

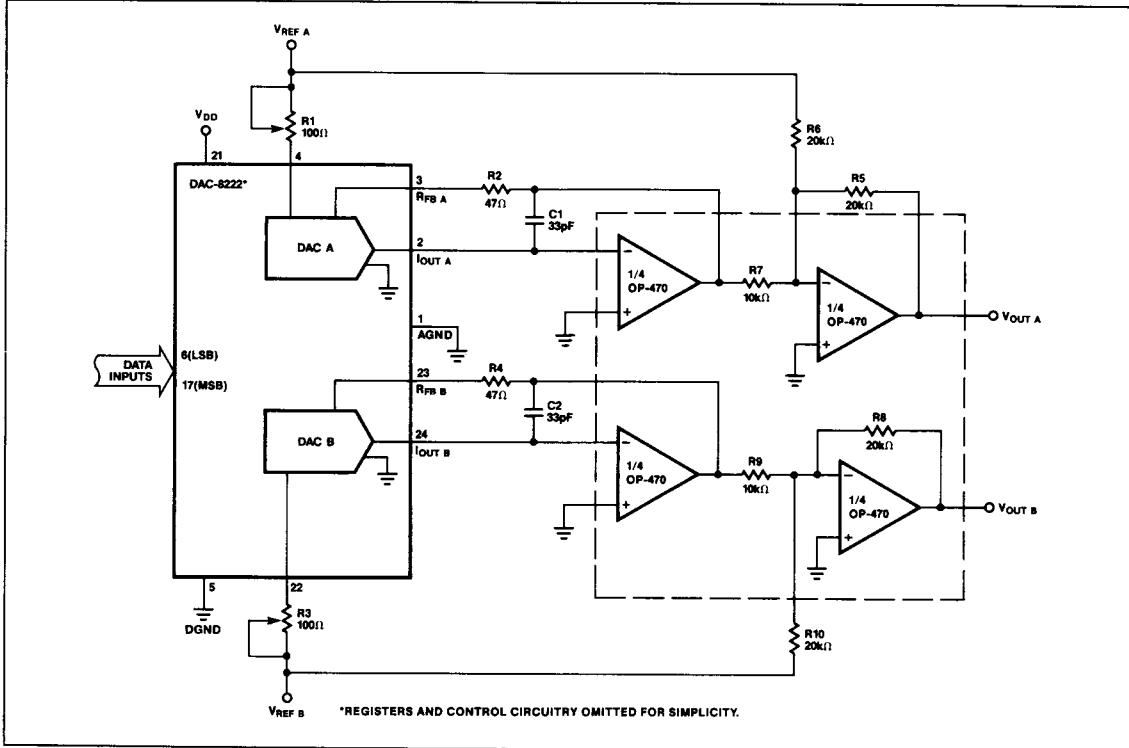


TABLE 2: Bipolar (Offset Binary) Code Table
(Refer to Figure 6)

BINARY NUMBER IN DAC REGISTER		ANALOG OUTPUT, V_{OUT} (DAC A or DAC B)
MSB	LSB	
1111	1111 1111	$+V_{REF} \left(\frac{2047}{2048} \right)$
1000	0000 0001	$+V_{REF} \left(\frac{1}{2048} \right)$
1000	0000 0000	0V
0111	1111 1111	$-V_{REF} \left(\frac{1}{2048} \right)$
0000	0000 0000	$-V_{REF} \left(\frac{2048}{2048} \right)$

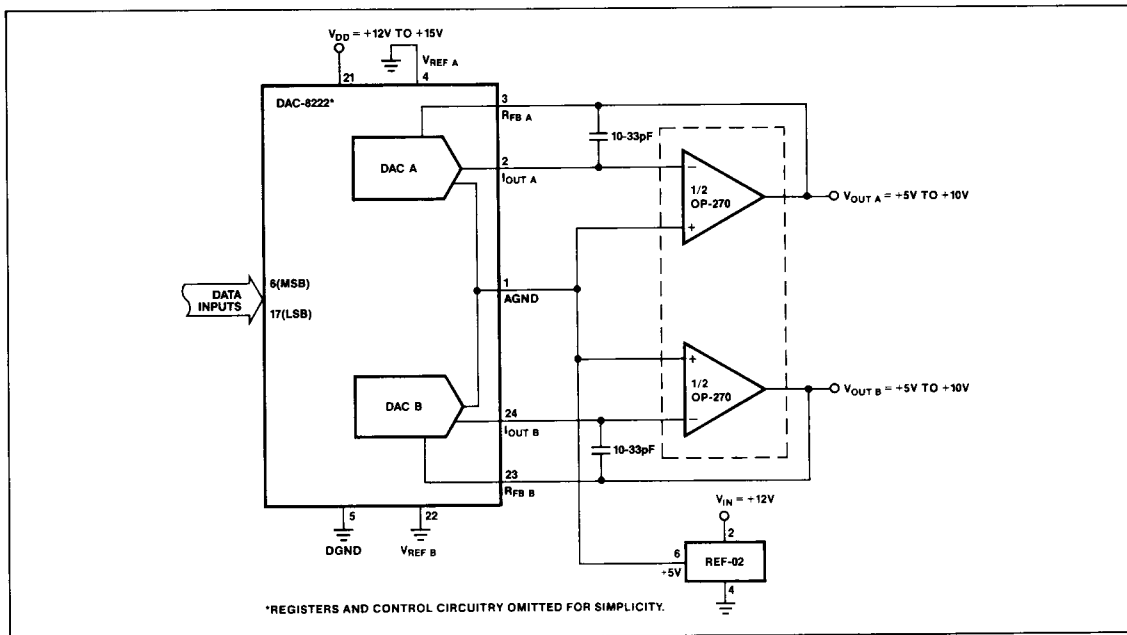
NOTE:
1 LSB = $(2^{-11}) (V_{REF}) = \frac{1}{2048} (V_{REF})$

resistors R5, R6, R7, should be ratio-matched to 0.01% so that gain error meets data sheet specifications. (Corresponding resistors, R8, R9, and R10 for DAC B should also be matched to 0.01%). The resistors should have identical temperature coefficients if operating over the full temperature range.

Zero and full-scale are adjusted one of two ways and are at the users discretion. Zero-output can be adjusted by first setting the digital inputs to 1000 0000 0000 and adjusting R1 (R3 for DAC B) so that $V_{OUT A}$ (or $V_{OUT B}$) equals 0V. If R1, R2 (R3, R4 for DAC B) are omitted, then $V_{OUT} = 0V$ can be adjusted by varying R6, R7 (R9, R10 for DAC B) ratios. Full-scale is adjusted by setting the digital inputs to 1111 1111 1111 and varying R5 (R8 for DAC B). Full-scale can also be adjusted by varying V_{REF} . Full-scale output is equal to V_{REF} minus one LSB.

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FIGURE 7: Single Supply Operation (Current Switching Mode)



SINGLE SUPPLY OPERATION

CURRENT STEERING MODE

Because the DAC-8222's R-2R resistor ladder terminating resistor is internally connected to AGND, it lends itself well to single supply operation in the current steering mode. This means that AGND can be raised above system ground as shown in Figure 7. The output voltage range will be from +5V to +10V depending on the digital input code and is given by:

$$V_{OUT} = V_{OS} + (n/4096) (V_{OS})$$

where V_{OS} = Offset Reference Voltage (+5V in Figure 7)
 n = Decimal Equivalent of the Digital Input Word

VOLTAGE SWITCHING MODE

Figure 8 shows the DAC-8222 in a single supply voltage switching mode of operation. In this configuration, the DAC's R-2R ladder acts as a voltage divider. The output voltage at the V_{REF} pin exhibits a constant impedance R (typically 11k Ω) and must be buffered by an op amp. R_{FB} pins are not used in this circuit configuration. The reference input voltage must be maintained within +1.25V of AGND and V_{DD} from +12V to +15V to preserve device accuracy.

The output voltage expression is given by:

$$V_{OUT} = V_{REF} (n/4096)$$

where n = Decimal Equivalent of the Digital Input Word

APPLICATIONS TIPS

GENERAL GROUND MANAGEMENT

Grounding techniques should be tailored to each individual system. Ground loops should be avoided, and ground current paths should be as short as possible and have a low impedance.

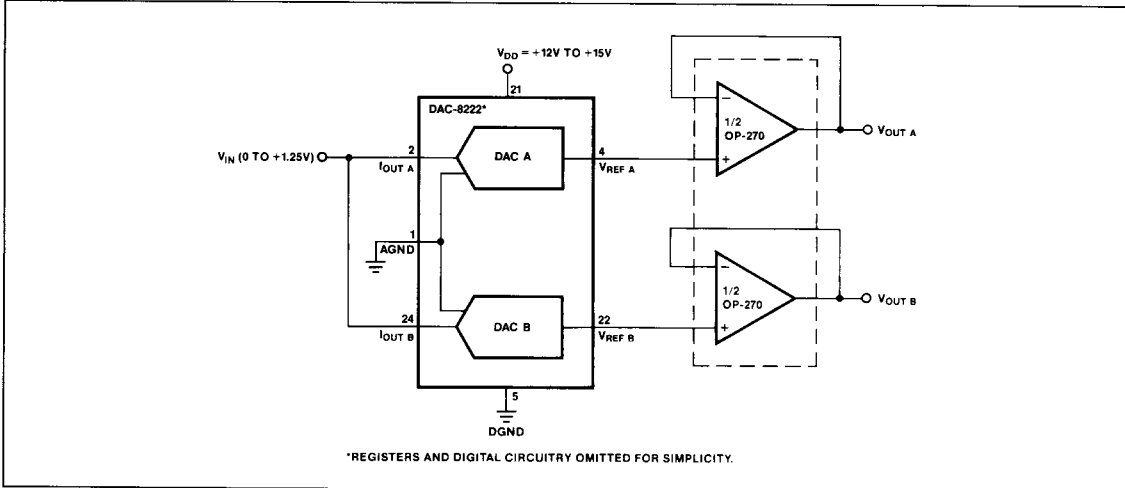
The DAC-8222's AGND and DGND pins should be tied together at the device socket to prevent digital transients from appearing at the analog output. This common point then becomes the single ground point connection. AGND and DGND should then be brought out separately and tied to their respective power supply grounds. Ground loops can be created if both grounds are tied together at more than one location, i.e., tied together at the device and at the digital and analog power supplies.

A PC board ground plane can be used for the single point ground connection should the connections not be practical at the device socket. If neither of these connections is practical or allowed, then the device should be placed as close as possible to the system's single point ground connection. Back-to-back Schottky diodes should then be connected between AGND and DGND.

POWER SUPPLY DECOUPLING

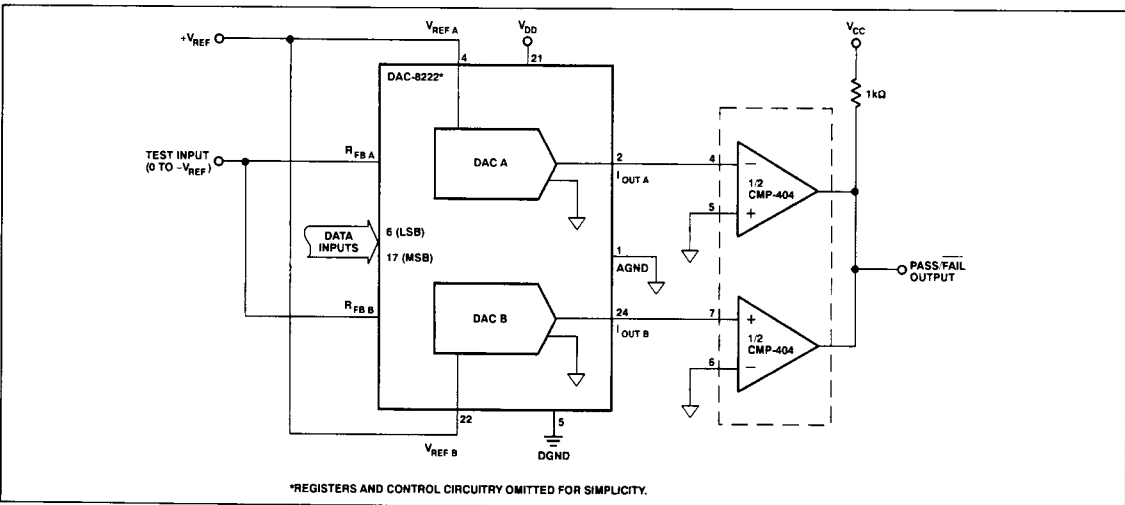
Power supplies used with the DAC-8222 should be well filtered and regulated. Local supply decoupling consisting of a 1 to 10 μ F tantalum capacitor in parallel with a 0.1 μ F ceramic is highly recommended. The capacitors should be connected between the V_{DD} and DGND pins and at the device socket.

FIGURE 8: Single Supply Operation (Voltage Switching Mode)



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FIGURE 9: Digitally-Programmable Window Detector (Upper/Lower Limit Detector)



BASIC APPLICATIONS

PROGRAMMING WINDOW DETECTOR

Figure 9 shows the DAC-8222 used in a programmable window detector configuration. The required upper and lower limits for the test are loaded into DAC A and DAC B. If a signal at the test input is not within the programmed limits, the output will indicate a logic zero.

MICROPROCESSOR INTERFACE CIRCUITS

The DAC-8222's versatile loading structure greatly simplifies interfacing to 16-bit bus systems; it also reduces the number of "glue" logic components. Data loading into its 12-bit wide data input is achieved by use of only two control signals, \overline{WR} and \overline{LDAC} . DAC selection is controlled with a single DAC A/DAC B line.

Figures 10 and 11 show how easily the DAC-8222 interfaces with the 8086 and 68000 16-bit microprocessors.

DAC-8222

FIGURE 10: DAC-8222 To 8086 Interface

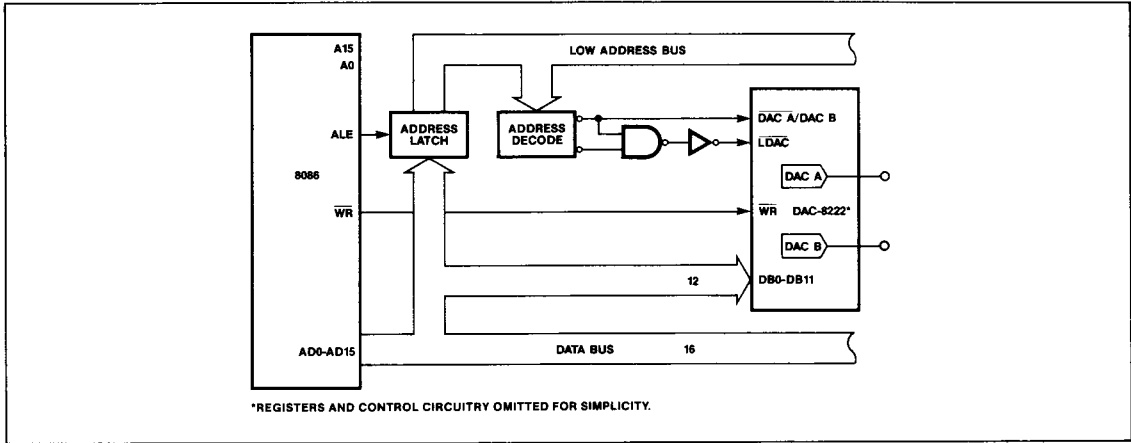


FIGURE 11: DAC-8222 To 68000 Interface

