zilog

Z89321/371

16-BIT DIGITAL SIGNAL PROCESSORS

FEATURES

Device	DSP ROM [KW]	OTP [KW]	DSP RAM [Words]	MIPS
Z89321	4		512	20
Z89371		4	512	20

Device	40-Pin DIP	44-Pin PLCC	44-Pin PQFP
Z89321	X	X	X
Z89371	X	X	X

- 0°C to 70°C Standard Temperature Range
  –40°C to +85°C Extended Temperature Range
- 4.5 to 5.5 Volt Operating Range

DSP Core

- 16-Bit Fixed Point DSP with 24-Bit ALU and Accumulator
- Single-Cycle Multiply and ALU Operations
- Six-Level Hardware Stack
- Six Data RAM Pointers and Sixteen Program Memory Pointers
- RISC Processor with 30 Instruction Types

Internal Peripherals

- 13-Bit General-Purpose Timer
- Dual Channel 8/16/64-Bit CODEC Interface with optional Hardware μ-Law Compression

External Peripheral Interface

- 16-Bit Tri-Stated External Data Bus
- 3-Bit Latched External Address Bus
- Wait-State Generator
- Three Vectored Interrupts

GENERAL DESCRIPTION

The Z893x1 products are high-performance Digital Signal Processors (DSPs) with a modified Harvard architecture featuring separate program and dual data memory banks. The design has been optimized for processing power with a minimum of silicon area.

The Z893x1 16/24-Bit architecture accommodates advanced signal processing algorithms. The operating performance and efficient architecture provide deterministic instruction execution. Compression, filtering, frequency detection, audio, voice detection/synthesis, and other vital algorithms can all be implemented.

Six data RAM pointers provide circular buffer capabilities and simultaneous dual operand fetching. Three vectored interrupts are complemented by a six-level stack. A 13-bit Timer is available for general-purpose use. A CODEC Interface allows high-speed transfer rates to accommodate digital audio and voice data. A dedicated Counter/Timer provides the necessary timing signals for the CODEC Interface.

The Z893x1 CODEC Interface is compatible with 8-bit PCM and 16/64-bit CODECs used in digital audio applications, and serial A/D and D/A converters. A Wait-State Generator is provided to accommodate slow external peripherals.

For prototypes, low volume, or special production runs, the Z89371 is a one-time programmable (OTP) device.

GENERAL DESCRIPTION (Continued)

Note: All signals with an overline are active Low. For example in RD/$\overline{WR}$, RD is active High and $\overline{WR}$ is active Low.

The power connections follow the convention described below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

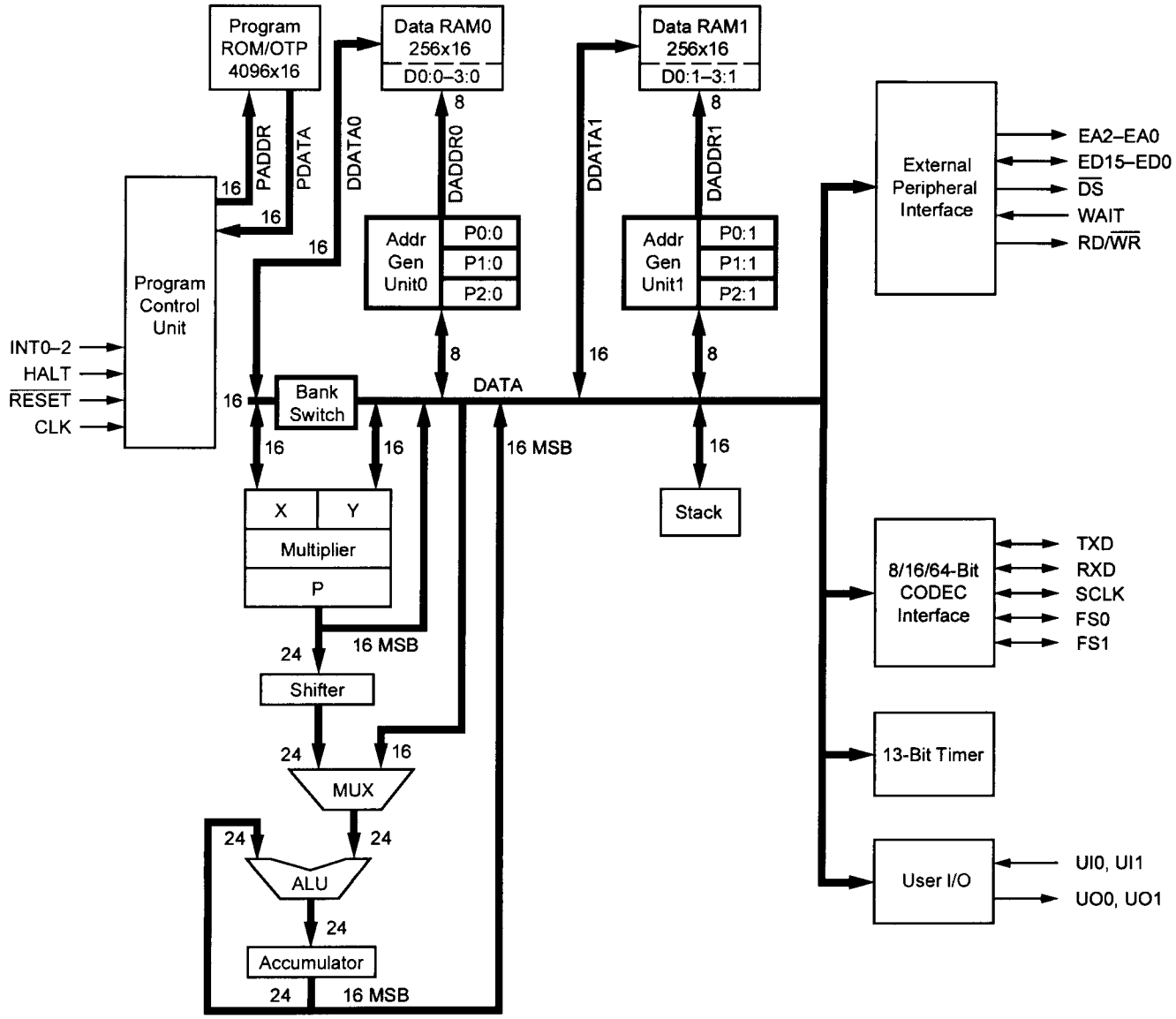


Figure 1. Z893x1 Functional Block Diagram

PIN FUNCTIONS

External Bus and External Registers. The following is made to clarify naming conventions used in this specification. The external bus and external registers are *"external"* to the DSP core, and are used to access internal and external peripherals.

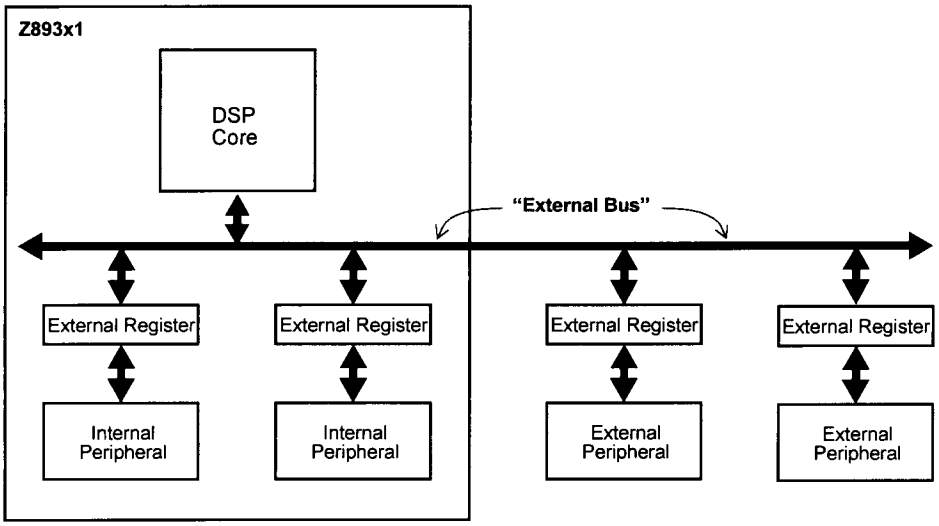


Figure 2. "External" Bus

EA2–EA0. External Address Bus (output).These pins control the user-defined register address output (latched). This bus is driven during both internal and external accesses. One of seven user-defined external registers is selected by the processor for reads or writes. External registers EXT0–EXT3 are always available to the user. External registers EXT4–EXT6 are used internally by the processor, or optionally by the user, if the pertinent internal peripherals are disabled. EXT7 is always reserved for use by the processor.

ED15–ED0. External Data Bus (input/output). These pins are the data bus for the user-defined external registers. The pins are normally tri-stated, except when these registers are specified as destination registers in a write instruction to an external peripheral. This bus uses the control signals RD/$\overline{WR}$, $\overline{DS}$, WAIT and the address pins EA2–EA0.

Note: The ED Bus was known as the EXT Bus in earlier versions of this document, and may be referred to as the EXT Bus, pins EXT15–EXT0, in other older related documents.

$\overline{DS}$. Data Strobe (output). This pin provides the data strobe signal for the ED Bus. DS is active for transfers to/from external peripherals only.

RD/$\overline{WR}$. Read/$\overline{Write}$ Select (output). This pin controls the data direction signal for the ED Bus. Data is available from the processor on ED15–ED0 when this signal and $\overline{DS}$ are both Low.

WAIT. WAIT State (input). The wait signal is sampled at the rising edge of the clock with appropriate setup and hold times. A single wait-state can be generated internally by setting the appropriate bits in the wait state register. The user must drive this line if multiple wait states are required. This pin has an internal pull-down.

HALT. Halt State (input). This pin stops program execution. The processor continuously executes NOPs and the program counter remains at the same value when this pin is held High. This pin has an internal pull-down.

INT0–INT2. Interrupts (input, positive edge triggered). These pins control interrupt requests 0–2. Interrupts are generated on the rising edge of the input signal. The DSP

PIN FUNCTIONS (Continued)

fetches the interrupt service routine starting addresses from the following program memory locations:

Device	INT0	INT1	INT2
Z89321/371	0FFFH	0FFEH	0FFDH
Z89391	FFFFH	FFFEH	FFFDH

The interrupt priority is INT0 = highest, INT2 = lowest. These pins have internal pull-downs.

Note: INT1 and INT2 pins are not available on the 40-pin DIP package.

CLK Clock (input). This pin is the clock circuit input.

$\overline{\text{RESET}}$. Reset (input, active Low). This pin resets the processor. It pushes the contents of the Program Counter (PC) onto the stack and then fetches a new PC value from program memory address 0FFCH (or FFFCH for the Z89391) after the RESET signal is released. The Status register is set to all zeros. At power-up, RAM and other registers are undefined; however, they are left unchanged with subsequent resets. RESET can be asserted asynchronously. If the rising edge of RESET meets prescribed setup conditions relative to the falling edge of the clock, the processor commences execution with a fixed number of clock cycles later. See the Timing Diagrams definitions for details.

UI0, UI1. User Input (input). These general-purpose input pins are directly tested by the conditional branch instructions. The pins can also be read as bits in the status register. These are asynchronous input signals that have no special clock synchronization requirements.

UO0, UO1. User Output (output). These general-purpose output pins reflect the value of two bits in the status register. These bits may be used to output data by writing to the status register.

Note: The value at the output pin is inverted from the value in the register.

The pins **SCLK, FS0, FS1, RXD** and **TXD** are described in the CODEC Interface section.

PIN DESCRIPTION

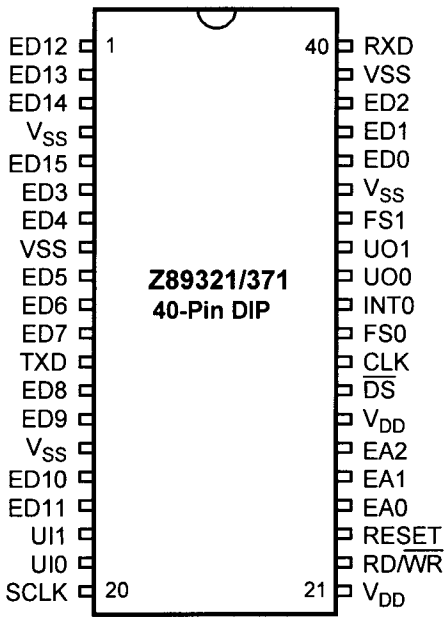


Figure 3. Z89321/371 40-Pin DIP Pin Assignments

Table 1. Z89321/371 40-Pin DIP Pin Identification

No.	Symbol	Function	Direction	No.	Symbol	Function	Direction
1	ED12	External Data Bus	In/Out	21	V_{DD}	Power Supply	Input
2	ED13	External Data Bus	In/Out	22	RD/$\overline{WR}$	Read/$\overline{Write}$ select for ED bus	Output
3	ED14	External Data Bus	In/Out	23	RESET	Reset	Input
4	V_{SS}	Ground		24	EA0	External Address Bus	Output
5	ED15	External Data Bus	In/Out	25	EA1	External Address Bus	Output
6	ED3	External Data Bus	In/Out	26	EA2	External Address Bus	Output
7	ED4	External Data Bus	In/Out	27	V_{DD}	Power Supply	Input
8	V_{SS}	Ground		28	$\overline{DS}$	Data Strobe for ED Bus	Output
9	ED5	External Data Bus	In/Out	29	CLK	Clock	Input
10	ED6	External Data Bus	In/Out	30	FS0	Frame Sync–CODEC Ch. 0	Output
11	ED7	External Data Bus	In/Out	31	INT0	Interrupt	Input
12	TXD	Serial Output Data	Output	32	UO0	User Output	Output
13	ED8	External Data Bus	In/Out	33	UO1	User Output	Output
14	ED9	External Data Bus	In/Out	34	FS1	Frame Sync–CODEC Ch. 1	Output
15	V_{SS}	Ground		35	V_{SS}	Ground	
16	ED10	External Data Bus	In/Out	36	ED0	External Data Bus	In/Out
17	ED11	External Data Bus	In/Out	37	ED1	External Data Bus	In/Out
18	UI1	User Input	Input	38	ED2	External Data Bus	In/Out
19	UI0	User Input	Input	39	V_{SS}	Ground	
20	SCLK	CODEC Serial Clock	Output	40	RXD	Serial Input Data	Input

Note: HALT, WAIT, INT1 and INT2 are not available in the 40-pin DIP package.

PIN DESCRIPTION (Continued)

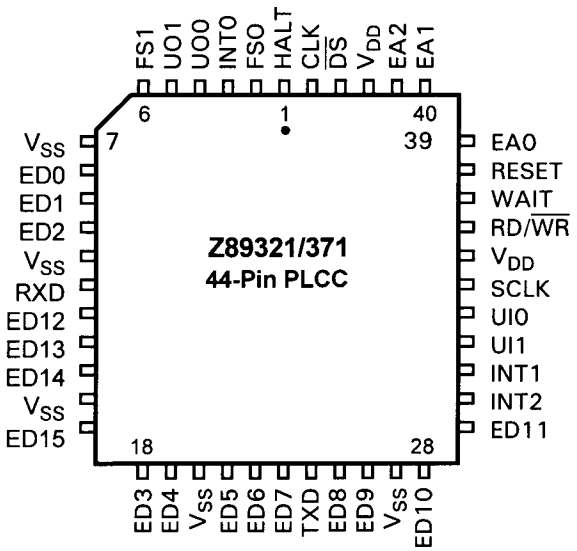


Figure 4. Z89321/371 44-Pin PLCC Pin Assignments

Table 2. Z89321/371 44-Pin PLCC Pin Identification

No.	Symbol	Function	Direction
1	HALT	Stop execution	Input
2	FS0	Frame Sync–CODEC Ch. 0	Output
3	INT0	Interrupt	Input
4	UO0	User Output	Output
5	UO1	User Output	Output
6	FS1	Frame Sync–CODEC Ch. 1	Output
7	V_{SS}	Ground	
8	ED0	External Data Bus	In/Out
9	ED1	External Data Bus	In/Out
10	ED2	External Data Bus	In/Out
11	V_{SS}	Ground	
12	RXD	Serial Input Data	Input
13	ED12	External Data Bus	In/Out
14	ED13	External Data Bus	In/Out
15	ED14	External Data Bus	In/Out
16	V_{SS}	Ground	
17	ED15	External Data Bus	In/Out
18	ED3	External Data Bus	In/Out
19	ED4	External Data Bus	In/Out
20	V_{SS}	Ground	
21	ED5	External Data Bus	In/Out
22	ED6	External Data Bus	In/Out

Table 2. Z89321/371 44-Pin PLCC Pin Identification

No.	Symbol	Function	Direction
23	ED7	External Data Bus	In/Out
24	TXD	Serial Output Data	Output
25	ED8	External Data Bus	In/Out
26	ED9	External Data Bus	In/Out
27	V_{SS}	Ground	
28	ED10	External Data Bus	In/Out
29	ED11	External Data Bus	In/Out
30	INT2	Interrupt	Input
31	INT1	Interrupt	Input
32	UI1	User Input	Input
33	UI0	User Input	Input
34	SCLK	CODEC Serial Clock	Output
35	V_{DD}	Power Supply	Input
36	RD/$\overline{WR}$	Read/$\overline{Write}$ select for ED bus	Output
37	WAIT	Wait state	Input
38	RESET	Reset	Input
39	EA0	External Address bus	Output
40	EA1	External Address bus	Output
41	EA2	External Address bus	Output
42	V_{DD}	Power Supply	Input
43	$\overline{DS}$	Data Strobe for ED Bus	Output
44	CLK	Clock	Input

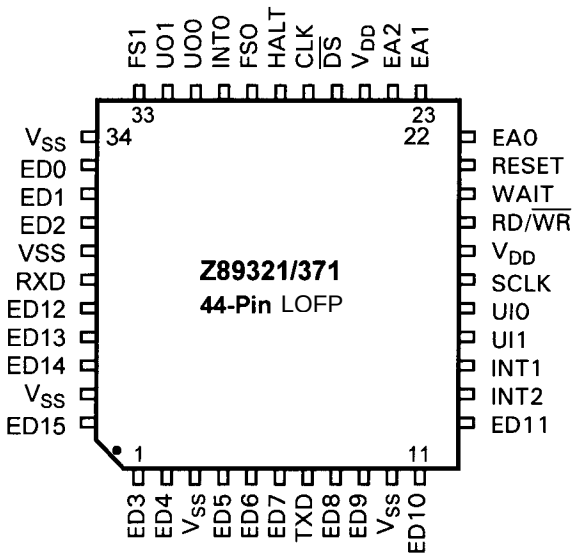


Figure 5. Z89321/371 44-Pin LOFP Pin Assignments

Table 3. Z89321/371 44-Pin LOFP Pin Identification

No.	Symbol	Function	Direction
1	ED3	External Data Bus	In/Out
2	ED4	External Data Bus	In/Out
3	V_{SS}	Ground	
4	ED5	External Data Bus	In/Out
5	ED6	External Data Bus	In/Out
6	ED7	External Data Bus	In/Out
7	TXD	Serial Output Data	Output
8	ED8	External Data Bus	In/Out
9	ED9	External Data Bus	In/Out
10	V_{SS}	Ground	
11	ED10	External Data Bus	In/Out
12	ED11	External Data Bus	In/Out
13	INT2	Interrupt	Input
14	INT1	Interrupt	Input
15	UI1	User Input	Input
16	UI0	User Input	Input
17	SCLK	CODEC Serial Clock	Output
18	V_{DD}	Power Supply	Input
19	RD/$\overline{WR}$	Read/$\overline{Write}$ select for ED bus	Output
20	WAIT	Wait state	Input
21	RESET	Reset	Input
22	EA0	External Address bus	Output

Table 3. Z89321/371 44-Pin LOFP Pin Identification

No.	Symbol	Function	Direction
23	EA1	External Address bus	Output
24	EA2	External Address bus	Output
25	V_{DD}	Power Supply	Input
26	$\overline{DS}$	Data Strobe for ED Bus	Output
27	CLK	Clock	Input
28	HALT	Stop execution	Input
29	FS0	Frame Sync–CODEC Ch. 0	Output
30	INT0	Interrupt	Input
31	UO0	User Output	Output
32	UO1	User Output	Output
33	FS1	Frame Sync–CODEC Ch. 1	Output
34	V_{SS}	Ground	
35	ED0	External Data Bus	In/Out
36	ED1	External Data Bus	In/Out
37	ED2	External Data Bus	In/Out
38	V_{SS}	Ground	
39	RXD	Serial Input Data	Input
40	ED12	External Data Bus	In/Out
41	ED13	External Data Bus	In/Out
42	ED14	External Data Bus	In/Out
43	V_{SS}	Ground	
44	ED15	External Data Bus	In/Out

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{DD}	Supply voltage with respect to V_{SS}	–0.3	7.0	V
T_{STG}	Storage Temperature	–65	150	°C
T_A	Ambient Operating Temperature			
	"S" device	0	70	°C
	"E" device	–40	85	°C

Stresses greater than those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only. Operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground.

Positive current $I_{(+)}$ flows into the referenced pin.

Negative current $I_{(-)}$ flows out of the referenced pin.

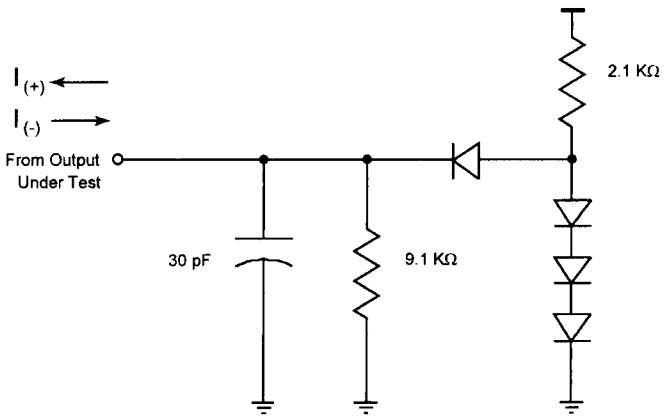


Figure 6. Test Load Diagram

DC ELECTRICAL CHARACTERISTICS

Table 4. V_{DD} = 5V ±10%, TA = 0°C to +70°C for "S" Temperature Range (T_A = –40°C to +85°C for "E" temperature range, unless otherwise noted)

Sym	Parameter	Condition	Min	Typ	Max	Units
I_{DD}	Supply Current	V_{DD} = 5.5V		70.0	TBD	mA
I_{DC}	DC Power Consumption	V_{DD} = 5.0V and CLK stopped High		5.0	TBD	mA
V_{IH}	Input High Level		2.7			V
V_{IL}	Input Low Level				0.8	V
I_L	Input Leakage				10	µA
V_{OH}	Output High Voltage	I_{OH} = –100 µA	V_{DD}–0.2			V
		I_{OH} = –160 µA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA			0.4	V
		I_{OL} = 2.0 mA			0.5	V
I_{FL}	Output Floating Leakage Current				10	µA

AC ELECTRICAL CHARACTERISTICS

Table 5. V_{DD} = 5V ±10%, T_A = 0°C to +70°C for "S" Temperature Range (T_A = –40°C to +85°C for "E" temperature range, unless otherwise noted)

Symbol	Parameter	Min [ns]	Max [ns]
Clock			
TCY	CLK Cycle Time	50	31250
CPWH	CLK Pulse Width High	21	
CPWL	CLK Pulse Width Low	21	
Tr	CLK Rise Time		2
Tf	CLK Fall Time		2
External Peripheral Bus			
DSVALID	$\overline{DS}$ Valid Time from CLK Fall	0	15
DSHOLD	$\overline{DS}$ Hold Time from CLK Rise	0	15
EASET	EA Setup Time to $\overline{DS}$ Fall	10	
EAHOLD	EA Hold Time from $\overline{DS}$ Rise	4	
RWSET	Read/Write Setup Time to $\overline{DS}$ Fall	10	
RWHOLD	Read/Write Hold Time from $\overline{DS}$ Rise	0	
RDSET	Data Read Setup Time to $\overline{DS}$ Rise	15	
RDHOLD	Data Read Hold Time from $\overline{DS}$ Rise	0	
WRVALID	Data Write Valid Time from $\overline{DS}$ Fall		5
WRHOLD	Data Write Hold Time from $\overline{DS}$ Rise	2	
Reset			
RSET	Reset Setup Time to CLK Fall for synchronous operation	15	
RWIDTH	Reset Low Pulse Width	2 TCY	
RRISE	Reset Rise Time		50
Interrupt			
INTSET	Interrupt Setup Time to CLK Fall	7	
INTWIDTH	Interrupt Low Pulse Width	1 TCY	
Halt			
HSET	Halt Setup Time to CLK Rise	4	
HHOLD	Halt Hold Time from CLK Rise	12	
Wait State			
WSET	Wait Setup Time to CLK Rise	20	
WHOLD	Wait Hold Time from CLK Rise	10	
CODEC Interface			
SSET	SCLK Setup Time from CLK Rise		15
FSSET	FSYNC Setup Time from SCLK Rise		7
TXSET	TXD Setup Time from SCLK Rise		7
RXSET	RXD Setup Time to SCLK Fall	7	
RXHOLD	RXD Hold Time from SCLK Fall	0	

TIMING DIAGRAMS

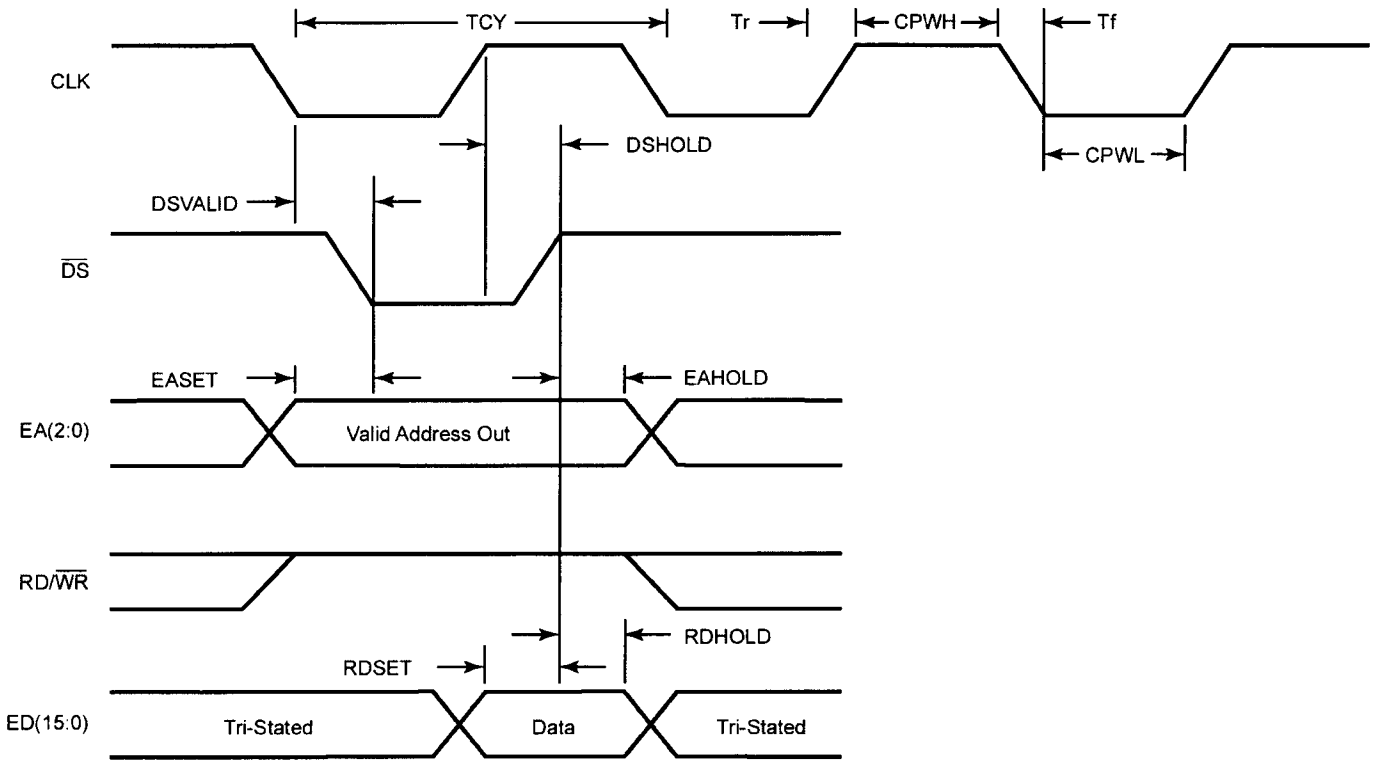


Figure 7. Read Timing

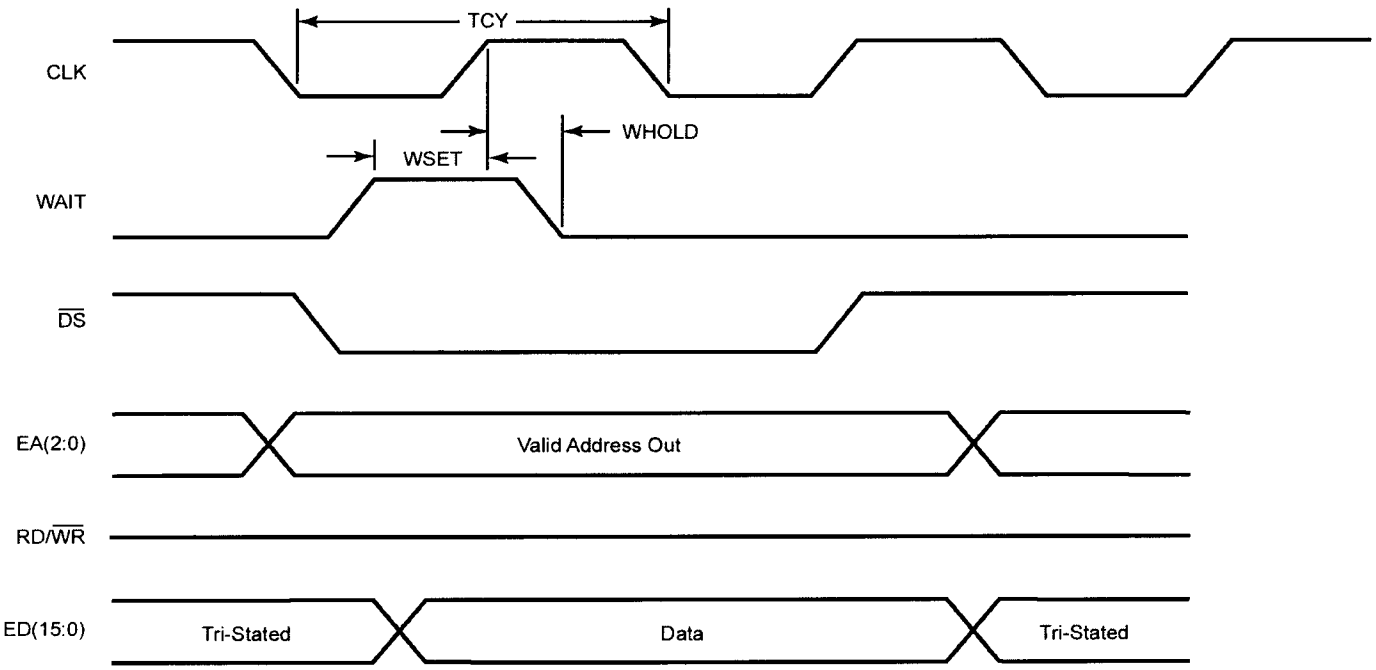


Figure 8. External Data (ED) Bus Read Timing Using WAIT Pin

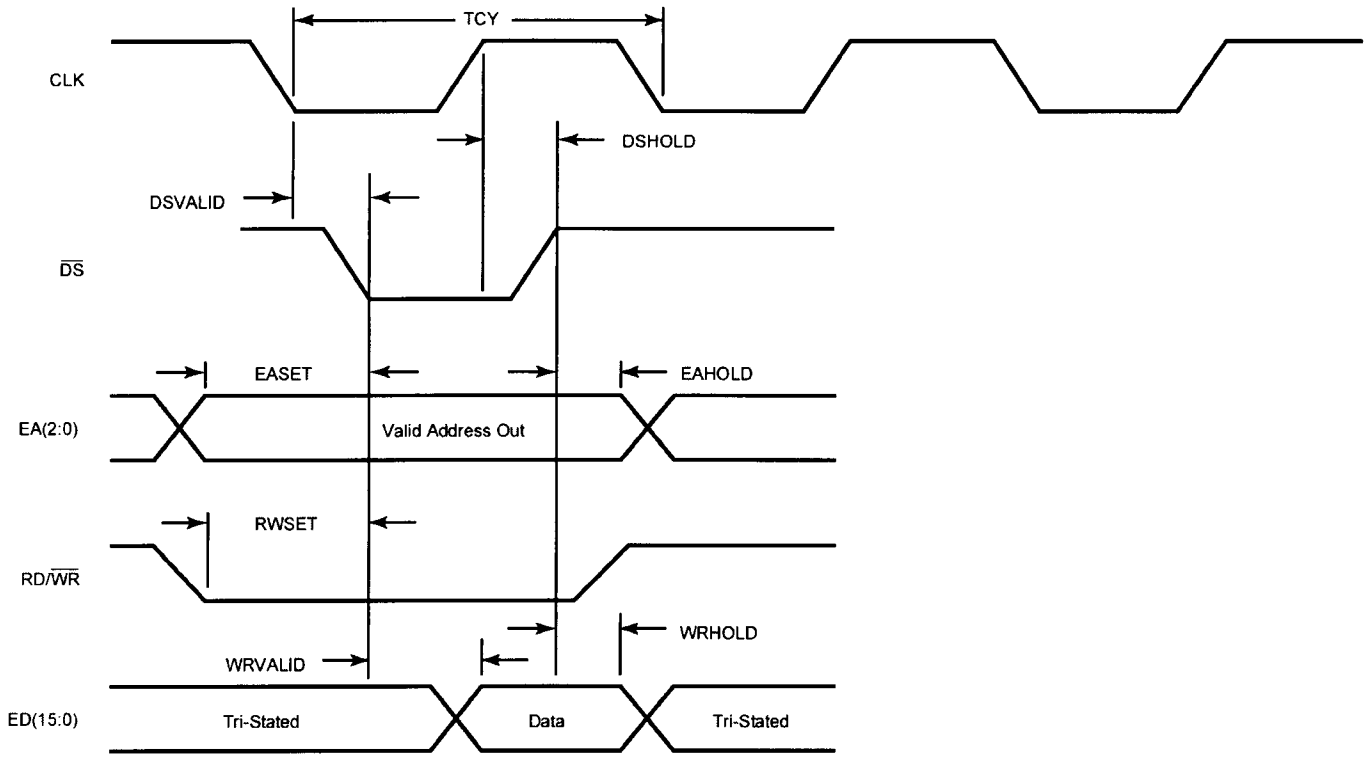


Figure 9. Write Timing

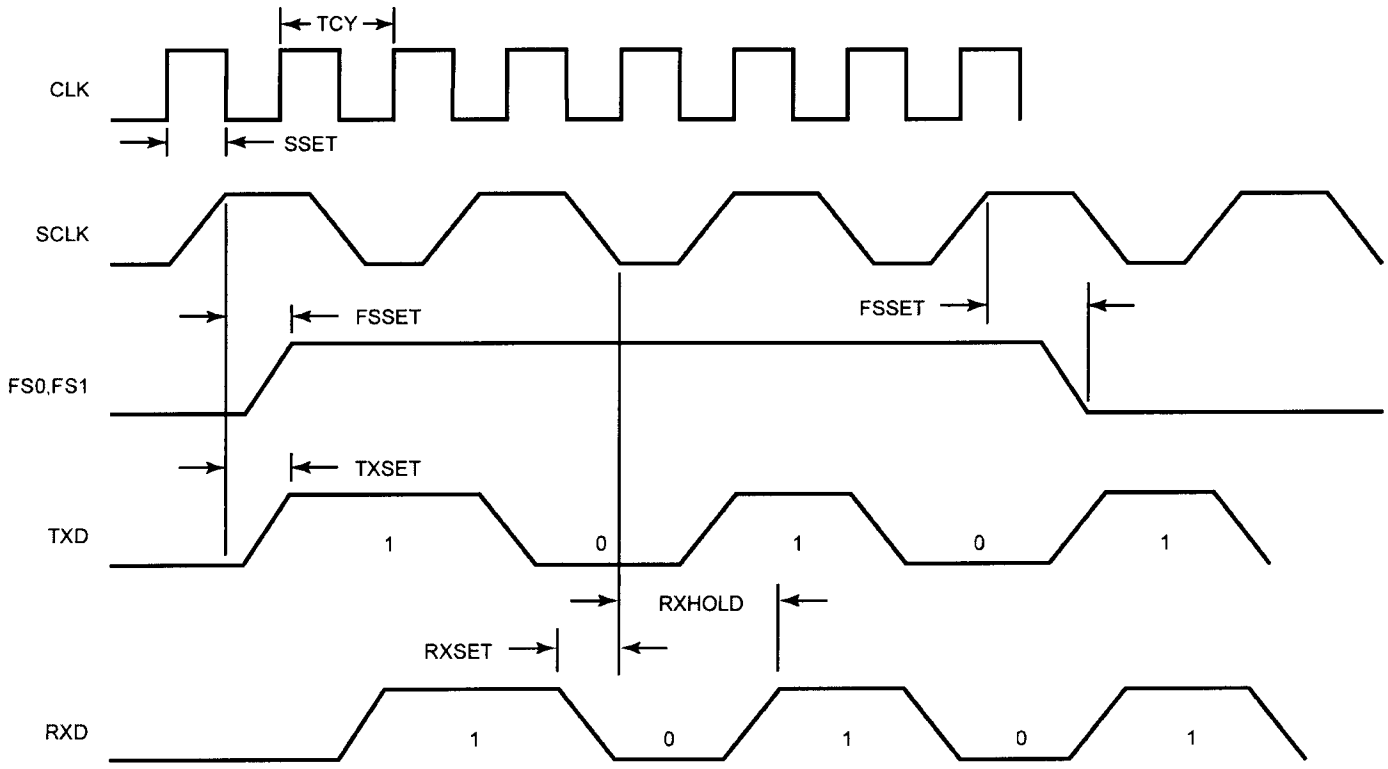


Figure 10. CODEC Interface Timing

TIMING DIAGRAMS (Continued)

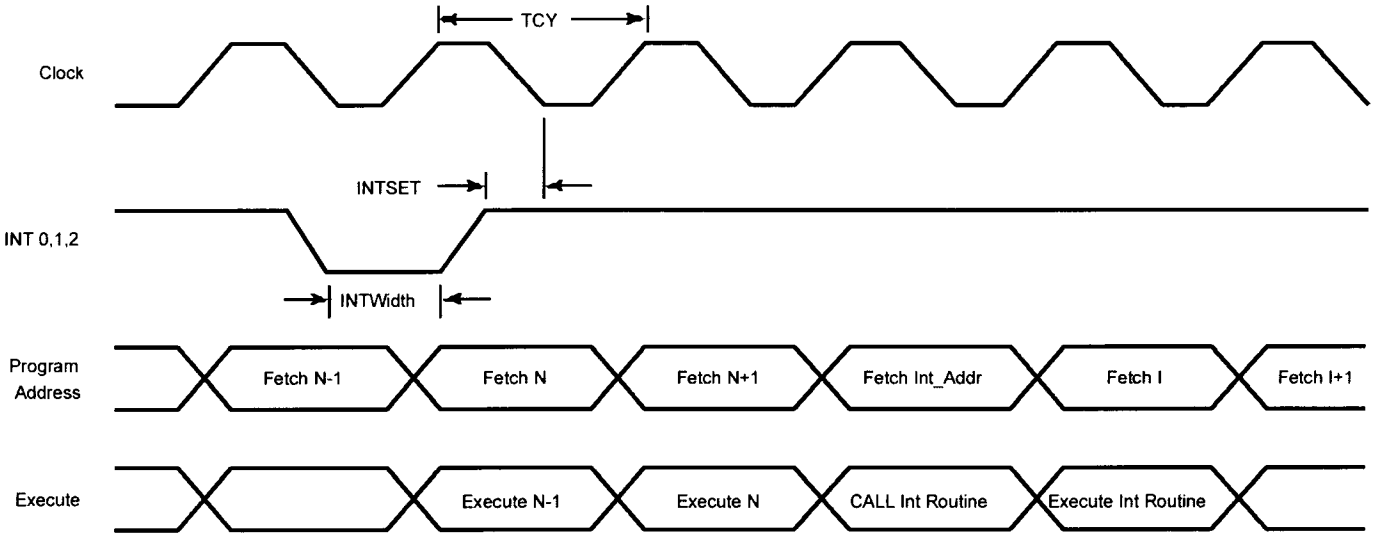


Figure 11. Interrupt Timing

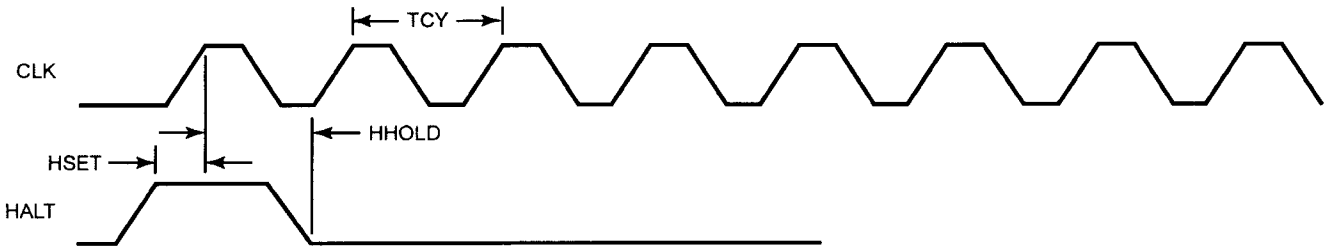


Figure 12. HALT Timing

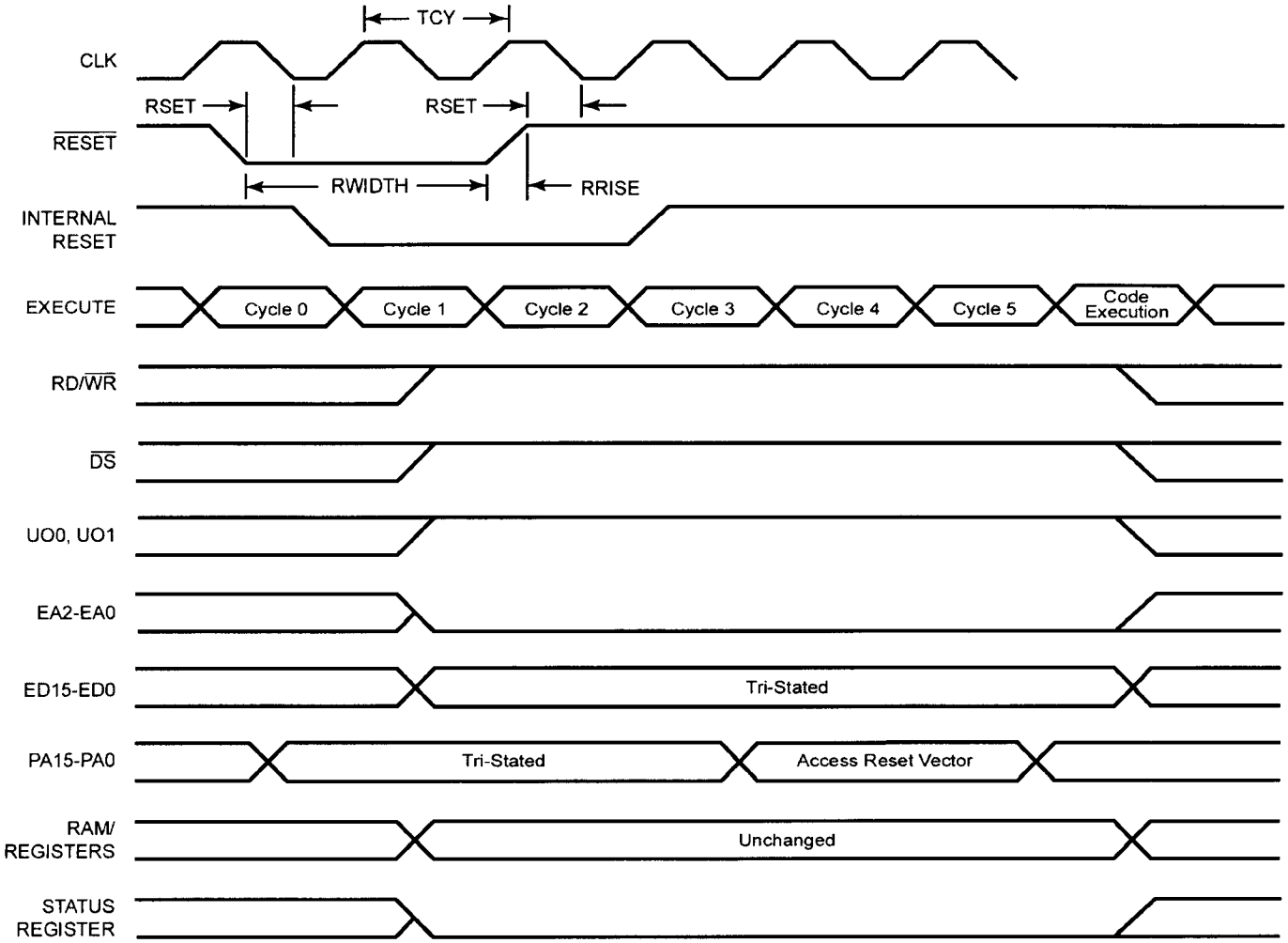


Figure 13. Synchronous Reset Timing

FUNCTIONAL DESCRIPTION

Instruction Timing. Most instructions are executed in one machine cycle. A multiplication or multiply/accumulate instruction requires a single cycle. Long immediate instructions (and Jump or Call instructions) are executed in two machine cycles. Specific instruction cycle times are described in the Instruction Description section.

Multiply/Accumulate. The multiplier can perform a 16-bit x 16-bit multiply (or multiply/accumulate) in one machine cycle using the Accumulator and/or both the X and Y inputs. The multiplier produces a 32-bit result; however, only the 24 most significant bits are saved for the next instruction or accumulation. For operations on very small numbers, where the least-significant bits are important, the data should first be scaled to avoid truncation errors.

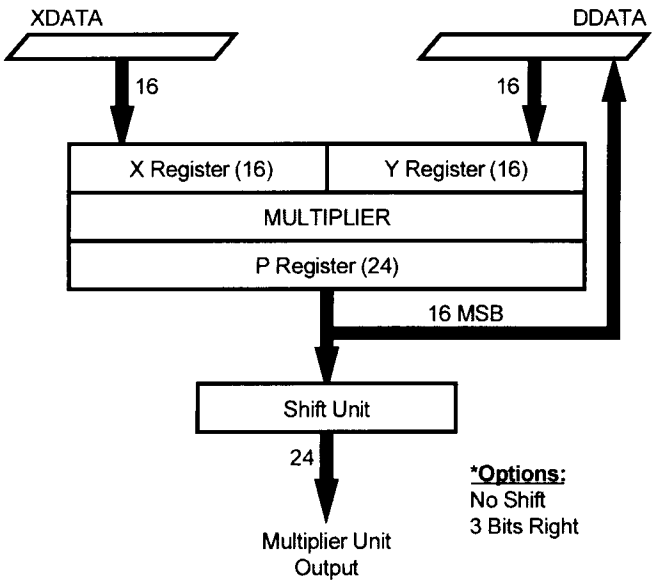


Figure 14. Multiplier Block Diagram

All inputs to the multiplier should be fractional two's-complement, 16-bit binary numbers, putting them in the range [–1 to 0.9999695]. The result is in 24 bits, so the range is [–1 to 0.9999999].

If 8000H is loaded into both the X and Y registers, the multiplication will produce an incorrect result. A positive one (+1) cannot be represented in fractional notation. The multiplier will actually yield the result 8000H x 8000H = 8000H (–1 x –1 = –1). The user should avoid this case to prevent erroneous results.

A shifter between the P Register and the Multiplier Unit Output can shift the data by three bits right or no shift.

Data Bus Bank Switch. There is a switch that connects the X Bus to the DDATA Bus that allows both the X and Y registers to be loaded with the same operand for a one cycle squaring operation. The switch is also used to read the X register.

ALU. The ALU has two input ports. One is connected to the output of the 24-bit Accumulator. The other input selects either the Multiplier Unit Output or the 16-bit DDATA bus (left-justified with zeros in the eight LSBs). The ALU performs arithmetic, logic, and shift operations.

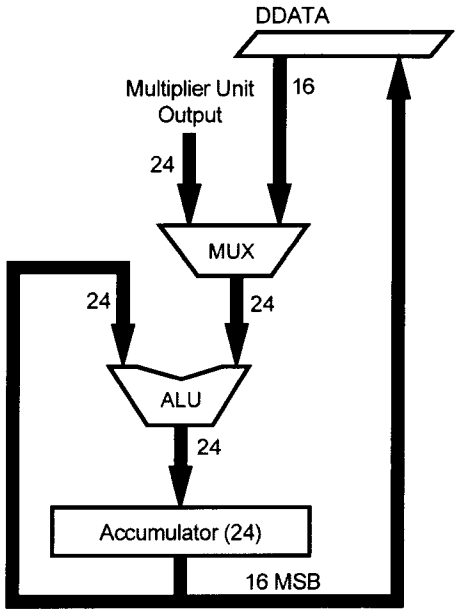


Figure 15. ALU Block Diagram

Hardware Stack. A six-level hardware stack is connected to the DDATA bus to hold subroutine return addresses or data. The Call instruction pushes PC+2 onto the stack, and the RET instruction pops the contents of the stack to the PC.

User Inputs and Outputs. The Z893x1 has two user inputs, UI0 and UI1, and two user outputs, UO0 and UO1. The input pins are connected directly to status register bits S10 and S11. These bits can be read, or they can be used as a condition code in any conditional instruction. The output pins are connected directly to status register bits S5 and S6, and can be written to.

Note: The value at the output pin is inverted from the value in the register.

Interrupts. The Z893x1 has three positive edge-triggered interrupt inputs. An interrupt is serviced at the end of an instruction execution. Two machine cycles are required to enter an interrupt instruction sequence. The PC is pushed onto the stack. At the end of the interrupt service routine, a RET instruction is used to pop the stack into the PC. The priority of the interrupts is INT0 = highest, INT2 = lowest. When those peripherals are enabled, INT1 is dedicated to the CODEC Interface and INT2 is dedicated to the 13-bit timer.

The Set-Interrupt-Enable-Flag (SIEF) instruction enables the interrupts. Interrupts are automatically disabled when entering an interrupt service routine. Before exiting an interrupt service routine, the SIEF instruction can be used to re-enable interrupts.

Registers. The Z893x1 has 19 internal registers and up to seven user-defined 16-bit external registers (EXT0–EXT6). The external register address space for EXT4–EXT6 is used by the Z893x1 internal peripherals. Disabling a peripheral allows access to these addresses for general-purpose use.

External Register Usage. The external registers EXT0–EXT6 are accessed using the External Address Bus EA2–EA0, the External Data Bus (ED Bus) ED15–ED0, and control signals $\overline{DS}$, WAIT, and RD/$\overline{WR}$. These registers provide a convenient data transfer capability with external peripherals. Data transfers can be performed in a single-cycle. An internal Wait-State generator is provided to accommodate slower external peripherals. A single wait state can be implemented through control register EXT7–2. For additional wait states, the WAIT pin can be used. The WAIT pin is monitored only during execution of a read or write instruction to external peripherals on the ED bus.

Wait-State Generator. An internal Wait-State generator is provided to accommodate slow external peripherals. A single Wait-State can be implemented through a control register. For additional states, a dedicated pin (WAIT) can be held Low. The WAIT pin is monitored only during execution of a read or write instruction to external peripherals (ED bus).

CODEC Interface. The CODEC Interface provides the necessary control signals for transmission of CODEC information to/from the processor. The CODEC Interface accommodates external 8-bit PCM or 16/64-bit linear CODECs. The CODEC Interface can also be used with external A/D and D/A converters. The interface can also be used as a high-speed serial port.

µ-Law Compression. The CODEC Interface provides optional hardware µ-Law compression from 13-bit format to 8-bit format. Decompression is performed in software using a 128-word lookup table.

Timers. Two programmable timers, a general purpose 13-bit Timer, and a dedicated 12-bit Counter/Timer are provided to support the CODEC Interface. The 13-bit Timer can be operated in either continuous or one-shot mode. If the CODEC Interface is not enabled, its 12-bit Counter/Timer is also available for general-purpose use.

MEMORY MAP

Program Memory. Programs of up to 4K words can be masked into internal ROM (Z89321) or programmed into an OTP (Z89371). Four locations are dedicated to the vector addresses for the three interrupts (0FFDH–0FFFH) and the starting address following a $\overline{\text{RESET}}$ (0FFCH). Internal ROM is mapped from 0000H to 0FFFH, and the highest location for program instructions is 0FFBH.

Internal Data RAM. All Z893x1 family members have internal 512 x 16-bit data RAM organized as two banks of 256 x 16-bit words each (RAM0 and RAM1). The three addressing modes available to access the data RAM are direct addressing, short form direct, and register indirect.

The contents of both data RAM banks can be read simultaneously and loaded into the X and Y inputs of the multiplier during a multiply instruction.

The addresses for each data RAM bank are:

0–255 (0000H–00FFH) for RAM0
256–511 (0100H–01FFH) for RAM1

Data RAM Pointers. In register indirect, each data RAM bank is addressed by one of three data RAM address pointers:

Pn:b, where
n = pointer number = 0, 1, or 2
b = bank = 0 or 1,

thus,

P0:0, P1:0, P2:0 for RAM0
P0:1, P1:1, P2:1 for RAM1

In auto-increment, loop-increment, and loop-decrement indirect addressing, the pointer is automatically modified.

The data RAM pointers, which may be read or written directly, are 8-bit registers connected to the lower byte of the internal 16-bit DDATA Bus.

Program Memory Pointers. The first 16 locations of each data RAM bank can be used as pointers to locations in Program Memory. These locations can be an efficient way to address coefficients. The programmer selects a pointer location using two bits in the status register and two bits in the operand. At any one time, there are eight usable pointers, four per bank, and the four pointers are in consecutive locations.

Dn:b, where
n = pointer number = 0, 1, 2, or 3
b = bank = 0 or 1,

thus,

D0:0, D1:0, D2:0, D3:0 for RAM0
D0:1, D1:1, D2:1, D3:1 for RAM1

For example, if S3/S4 = 01 in the status register, then D0:0/D1:0/D2:0/D3:0 refer to register locations 4/5/6/7 in data RAM Bank 0.

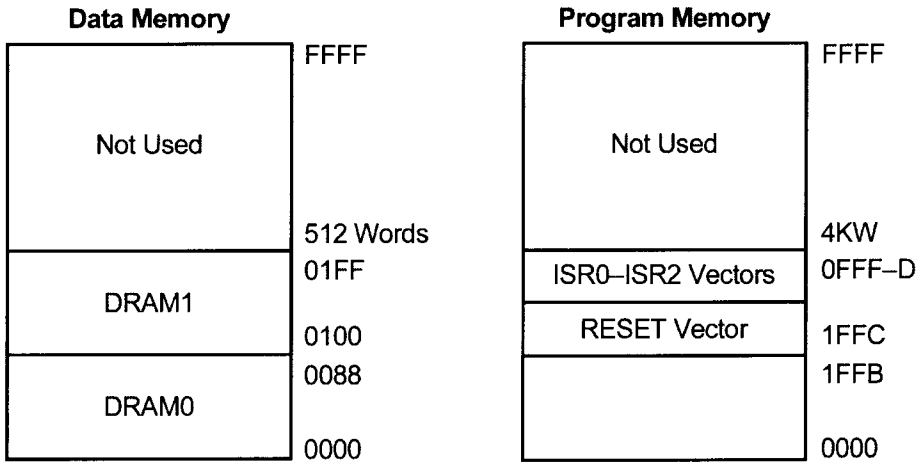


Figure 16. Memory Map

REGISTERS

The internal registers are defined in Table 6 below:

Table 6. Register Definitions

Register	Definition
X	Multiplier X Input, 16-bits
Y	Multiplier Y Input, 16-bits
P	Multiplier Output, 24-bits
A	Accumulator, 24-bits
Pn:b	Six Data RAM Pointers, 8-bits each
PC	Program Counter, 16-bits
SR	Status Register, 16-bits
EXT4	13-bit Timer Configuration Register
EXT5–1	CODEC Interface Channel 0 Data
EXT5–2	CODEC Interface Channel 0 Data
EXT6–1	CODEC Interface Channel 1 Data
EXT6–2	CODEC Interface Channel 1 Data
EXT7–1	CODEC Interface Configuration Register
EXT7–2	Wait-State Generator and CODEC Interface Configuration Register

Note: The loading and reading of the three pairs of CODEC Interface registers (EXT5–1,2 EXT6–1,2 and EXT7–1,2) are described in the CODEC Interface section.

X and **Y** are two 16-bit input registers for the multiplier. These registers can be utilized as temporary registers when the multiplier is not being used.

P holds the result of multiplications and is read-only.

A is a 24-bit Accumulator. The output of the ALU is sent to this register. When 16-bit data is transferred into this register, it is placed into the 16 MSBs, and the least significant eight bits are set to zero. Only the upper 16 bits are transferred to the destination register when the Accumulator is selected as a source register in transfer instructions.

Pn:b are the pointer registers for accessing data RAM where n = 0, 1, or 2, and b = 0 or 1. These registers can perform either a direct read or write function, and each can point to locations in data RAM.

PC is the Program Counter. Any instruction which may modify this register requires two clock cycles.

SR is the status register. It contains the ALU status and processor control bits (Table 7).

Table 7. Status Register Bit Functions

SR Bit	Function	Read/Write
S15 (N)	ALU Negative	RO
S14 (OV)	ALU Overflow	RO
S13 (Z)	ALU Zero	RO
S12 (L)	Carry	RO
S11 (UI1)	User Input 1	RO
S10 (UI0)	User Input 0	RO
S9 (SH3)	MPY Output Arithmetically Shifted Right by Three Bits	R/W
S8 (OP)	Overflow Protection	R/W
S7 (IE)	Interrupt Enable	R/W
S6 (UO1)	User Output 1	R/W
S5 (UO0)	User Output 0	R/W
S4–S3	"Short Form Direct" bits	R/W
S2–S0 (RPL)	RAM Pointer Loop Size	R/W

Note: RO = read only, RW = read/write. The status register can always be read in its entirety.

S15–S12 are set/reset by the ALU after an operation.

S11–S10 are set/reset by the user inputs.

If S9 is set, and a multiply/shift option is used, the shifter shifts the result three bits right. This feature allows the data to be scaled and prevents overflows.

If S8 is set, the hardware clamps at maximum positive or negative values instead of overflowing.

S7 enables interrupts.

S6–S0 are control bits.

REGISTERS (Continued)

Table 8. RPL Description

S2	S1	S0	Loop Size
0	0	0	256
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

The following are not actually registers; however, they have a read/write function that acts primarily the same way as the hardware registers do on the chip:

Register	Register Definition
BUS	DDATA Bus
Dn:b	Program Memory Pointers
EXTn	External Registers

BUS is a read-only register which, when accessed, returns the contents of the D-Bus. BUS is used for emulation only.

Dn:b refers to locations in RAM that can be used as a pointer to locations in program memory. These locations make the Z89321/371 capable for coefficient addressing. The programmer decides which location to choose from based on two bits in the status register and two bits in the operand; only the lower 16 possible locations in RAM can be specified. At any one time, there are eight usable pointers, four per bank, and the four pointer are in consecutive locations in RAM. For example, if S3/S4=1 in the status register, then D0:0/D1:0/D2:0/D3:0 refer to register locations 4/5/6/7 in RAM Bank 0.

Note: When the data pointers are being written to, a number is actually being loaded to Data RAM. In effect, these data pointers can be used as a limited method for writing to RAM.

EXT0–EXT3 are used to map external peripherals into the address space of the processor.

Note: The actual register RAM does not exist on the chip, but would exist as part of the external device (such as an A/D result latch). The External Address Bus, EA2–EA0, the External Data Bus, ED15–ED0 and the control signals $\overline{DS}$, WAIT and RD/$\overline{WR}$, are used to access external peripherals.

EXT4 is used by the 13-bit Timer. If the Timer is disabled, then this address can be used to access an external peripheral on the External Data Bus.

EXT5 and **EXT6** are used by the CODEC Interface channels 0 and 1 respectively. If a CODEC channel is disabled, the corresponding address can be used to access an external peripheral.

EXT7 is used to program wait states for EXT0–EXT6, and is not available for accessing an external peripheral.

If both the Timer and CODEC Interface are disabled, there are 7 addresses available to access external peripherals.

If both the Timer and CODEC Interface are enabled, there are 4 addresses available to access external peripherals.

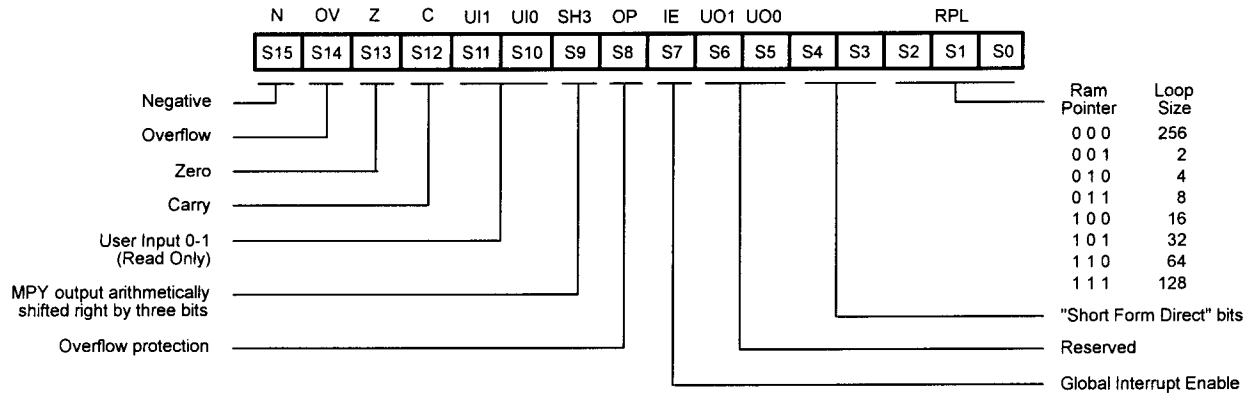


Figure 17. Status Register

PERIPHERAL OPERATION

Overview

The peripherals for the Z893x1 family consist of a general purpose 13-bit Timer and a dual channel CODEC Interface.

The CODEC Interface contains its own 12-bit Counter/Timer. When the CODEC Interface is disabled, the Counter/Timer is available for general purpose use.

The output of the 12-bit Counter/Timer can also be linked with the input of the 13-bit Timer for extended timing. See the EXT4 and EXT7 register definitions for more information and examples.

Enabling and Disabling Peripherals

At power on, and after a $\overline{\text{RESET}}$, the 13-bit general purpose Timer is enabled, but count operation is disabled. See the EXT4 register definition for more information concerning the operation of the Timer. While the Timer is enabled, it uses INT2 to signal a time out. When the Timer is disabled, EXT4 and INT2 are available for use by an external peripheral.

At power on, and after a $\overline{\text{RESET}}$, the CODEC Interface is disabled. See EXT5, EXT6, and EXT7 register definitions for more information concerning the operation of the CODEC Interface. While the CODEC Interface is enabled, it uses INT1 to signal the end of a frame. When a CODEC Interface channel is disabled, its corresponding EXT address is available. When both channels are disabled, EXT5, EXT6, and INT1 are available for use by an external peripheral. EXT7 is always reserved for internal use.

If an internal peripheral is enabled, the External Bus data and data strobe signals for the corresponding register address are not available on the External Bus (internal peripheral data transfers are processed internally).

Interrupts

The Z893x1 interrupts are:

INT0	General-Purpose Use
INT1	CODEC Interface (when enabled), or else User
INT2	Timer (when enabled), or else User

13-BIT GENERAL PURPOSE TIMER

The General-Purpose Timer can be enabled or disabled. At power-on or $\overline{\text{RESET}}$, the counter is enabled. When the Timer is disabled, it can only be re-enabled by another $\overline{\text{RESET}}$. The Timer operates in a continuous or one-shot mode, and can be stopped. The Timer utilizes a 13-bit down-counter.

Continuous Mode With a load instruction, the user sets the Timer to run the mode, selects the clock source, and loads a non-zero count value:

1. When the down-counter reaches zero, an interrupt is generated on INT2,
2. The non-zero count value is automatically reloaded into the down-counter,
3. The process continues at step #1.

One-Shot Mode With a load instruction, the user sets the Timer to run the mode, selects the clock source, and loads a non-zero count value:

4. When the down-counter reaches zero, an interrupt is generated on INT2,
5. The user interrupt service routine must load a zero value into the Count Operation bit (D14 of EXT4),
6. The process stops.

Timing Intervals If the Timer clock source is CLK/2:

Time Interval = (count value) x (2/CLK)

Timer Frequency = (CLK/2) / (count value)

where CLK denotes the system clock frequency.

Extended Timing Intervals The Timer interval can be extended beyond 13-bits by using the Timer in conjunction with the CODEC Interface Counter/Timer. The count is thus extended to a maximum of 25 bits:

- 12-bits from the CODEC counter/timer
- 13-bits from the Timer

If the Timer clock source is the CODEC counter output:

Time Interval =(Timer count value) x (CODEC counter/timer period)

Timer Freq. = (CODEC counter/timer freq.) ÷ (Timer count value)

Timer Interrupt Behavior The following clarifies the behavior of the Timer interrupt:

- While the Timer is enabled, it utilizes theINT2 service routine address.
- The Timer is enabled after $\overline{\text{RESET}}$; however, the Timer is in stop mode.
- The INT2 pin has an internal pull-down.
- When the Timer is in run mode, it generates an interrupt each time it counts down to zero.
- When the Timer is disabled, INT2 can be controlled by an external peripheral.

Note: If the Timer is to be disabled, and an external peripheral is driving INT2, it should hold INT2 High while the Timer is being disabled.

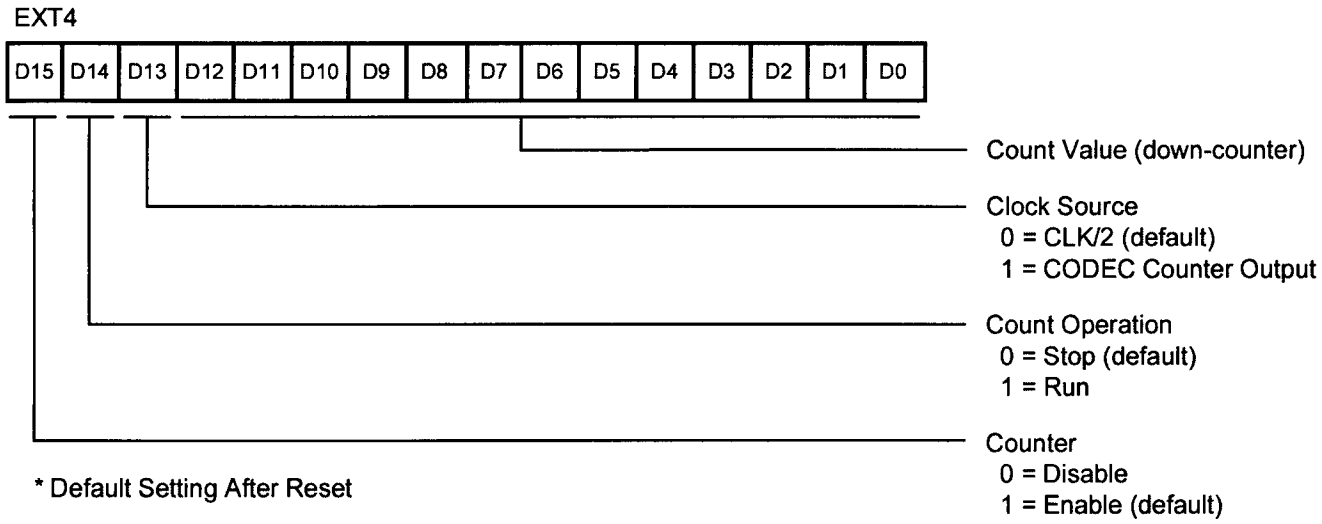


Figure 18. Timer Register EXT4

CODEC INTERFACE

Overview

The CODEC Interface not only supports a variety of external 8-bit, 16-bit linear, 64-bit sigma-delta stereo CODECs, and external A/D and D/A Converters, but the interface can also be used as a general purpose high-speed serial port. The CODEC Interface includes optional hardware μ-Law compression. The CODEC Interface is designed to support both Half-Duplex and Full-Duplex operation. The CODEC Interface is designed to operate in master mode only. The CODEC Interface generates a serial clock and two Frame Sync signals, which allows for two channels of data.

Hardware

The CODEC Interface hardware uses six 16-bit registers, μ-Law compression logic, and general-purpose control logic to control transfers to/from the appropriate registers.

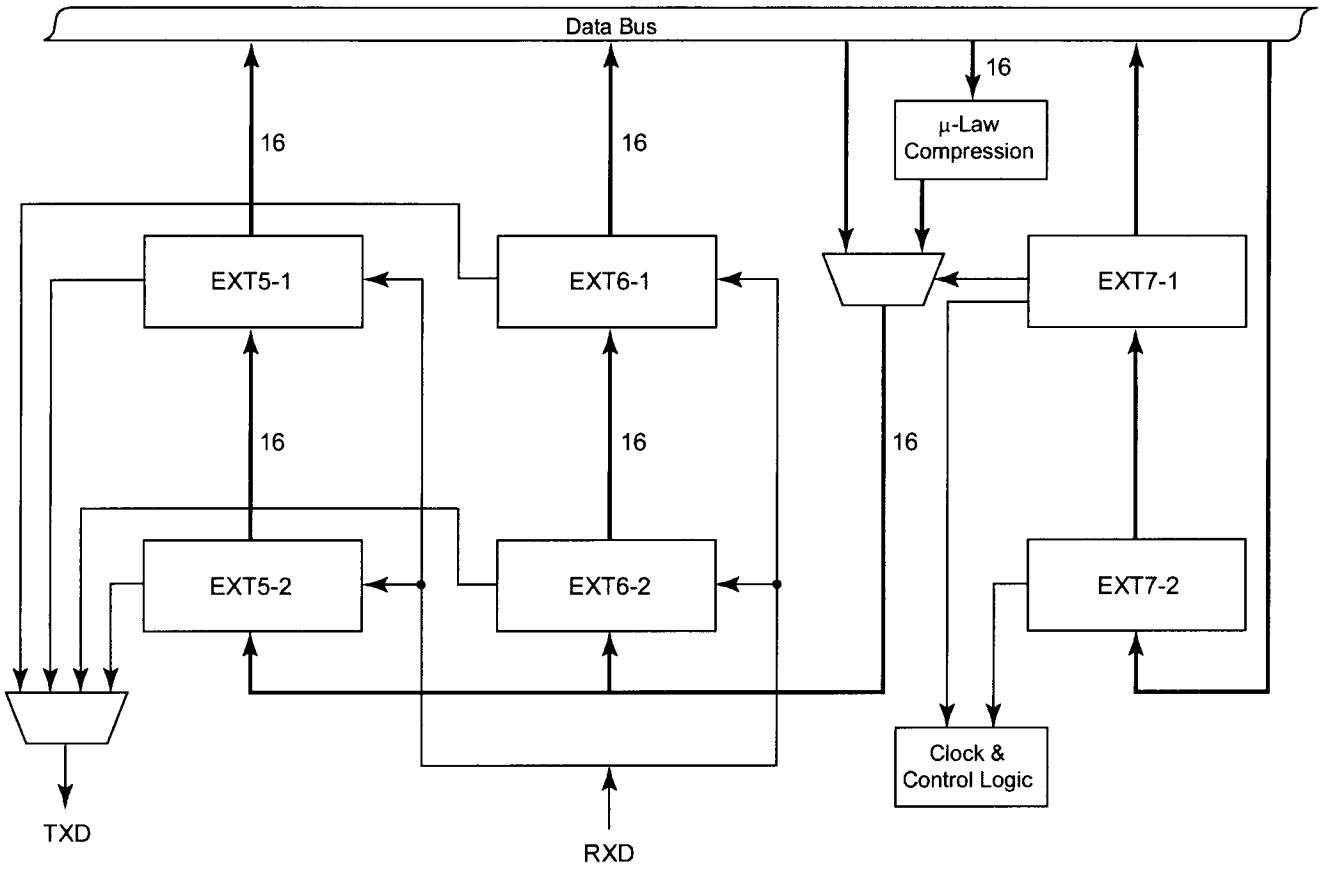


Figure 19. CODEC Interface Block Diagram

CODEC Interface Control Signals

SCLK. Serial Clock (output). This pin provides the clock signal for operating the external CODEC. A 4-bit prescaler is used to divide down the system clock (CLK) to produce the desired output frequency of SCLK. An internal divide-by-two is performed on CLK before passing it to the SCLK prescaler:

$$SCLK = (CLK/2) \div PS$$

where PS = 2's complement of the 4-bit Pre-Scaler value (PS is an up-counter).

TXD. Serial Output Data (output). This pin provides 8, 16, and 64-bit data transfers. Each bit is clocked out of the processor by the rising edge of SCLK, with the MSB transmitted first.

RXD. Serial Input Data (input). This pin provides 8, 16, and 64-bit data transfers. Each bit is clocked into the processor by the falling edge of SCLK, with the MSB received first.

FS0, FS1. Frame Sync 0 and Frame Sync 1 (output). These pins are used to mark data transfer/receive frames. The rising and falling edge of the Frame Sync signals indicate the beginning and the end of each serial data transmission.

CODEC Interface Interrupt Behavior

When the transmission of serial data is completed, the CODEC Interface generates an internal interrupt which vectors to the INT1 service routine address. This interrupt is coincident with the falling edge of FS1. The following clarifies the behavior of the CODEC Interface interrupt:

- While the CODEC Interface is enabled, it utilizes the INT1 service routine address.
- The CODEC Interface will be disabled after $\overline{\text{RESET}}$.
- The INT1 pin has an internal pull-down.
- If INT1 is tied High, the CODEC Interface generates an interrupt at the end of each frame transfer.
- If INT1 is not connected, or tied Low, the CODEC Interface not only generates an interrupt when first enabled, but generates an interrupt at the end of each frame transfer.
- When the CODEC Interface is disabled, INT1 can be controlled by an external peripheral.

Note: In single channel applications, use Channel 1 because INT1 coincides with FS1, not FS0.

Registers

The CODEC Interface registers (EXT5, EXT6 and EXT7) each act as a 2-deep FIFO. See the CODEC Interface Block Diagram for more information, Figure 19. Two operations may be required for some data transfers.

EXT5 and **EXT6.** The CODEC Interface constantly transfers and receives data during normal operation. The reading of receive data, and the writing of transmit data, are interleaved.

An example of Channel 1 operation in 8 or 16-bit mode, where one can wait for the input data, is as follows:

```
LD<dest>, EXT6          ; Read previous input data from
                          EXT6–1
LD EXT6, <xmit data>    ; Push current data from EXT6–2
                          to EXT6–1
                        ; Load EXT6–2 with data to be
                          transmitted
```

To obtain the input data as soon as it arrives, and extra instruction is required:

```
LD EXT6,<anything>      ; Push current input data from
                          EXT6–2 to EXT6–1
LD<test>, EXT6          ; Read current input data from
                          EXT6–1
LD EXT6, <xmit data>    ; Load EXT6–2 with data to be
                          transmitted
```

For 64-bit mode, one can use the following code sequence:

```
LD <Ch. 0 MSW input dest>, ; Get MSW of Ch. 0 input
EXT5
LD <Ch. 1 MSW input dest>, ; Get MSW of Ch 1 input
EXT6
LD EXT5,                ; Move LSB of Ch. 0 input
<Ch. 0 MSW output data>   and Load MSW of output
LD EXT6,                ; Move LSB of Ch. 1 input
<Ch. 1 MSW output data>   and Load MSW of output
LD<Ch. 0 LSW input test>, ; Get LSW of Ch. 0 input
EXT5
LD<Ch. 1 LSW input test>, ; Get LSW of Ch. 1 input
EXT6
LD EXT5,                ; Load LSW of Ch. 0 output
<Ch. 0 LSW output data>
LD EXT6,                ; Load LSW of Ch. 1 output
<Ch. 1 LSW output data>
```

Note: EXT# denotes EXT5 or EXT6.

In the 8 and 16-bit modes, EXT5–2 and EXT6–2 are the shift registers for Channel 0 and Channel 1, respectively. In 8-bit mode, the 8-bits reside in the least significant byte for both transmit and receive. In 64-bit mode, the output/input order is EXT 5–1 first, followed by EXT5–2, EXT6–1, and finally by EXT6–2. In all modes, the MSB is shifted out/in first.

Channel 0 uses FS0, EXT5–1, and EXT5–2. Channel 1 uses FS1, EXT6–1, and EXT6–2.

EXT7. This register contains the configuration information for the CODEC Interface and the Wait-State Generator. In normal operation, the user writes configuration data for EXT7–1 followed by configuration data for EXT7–2.

```
Write EXT7 LD EXT7, <config data1>  ; Move data to 7–2
           LD EXT7, <config data2>  ; Move data to 7–1
```

CODEC INTERFACE (Continued)

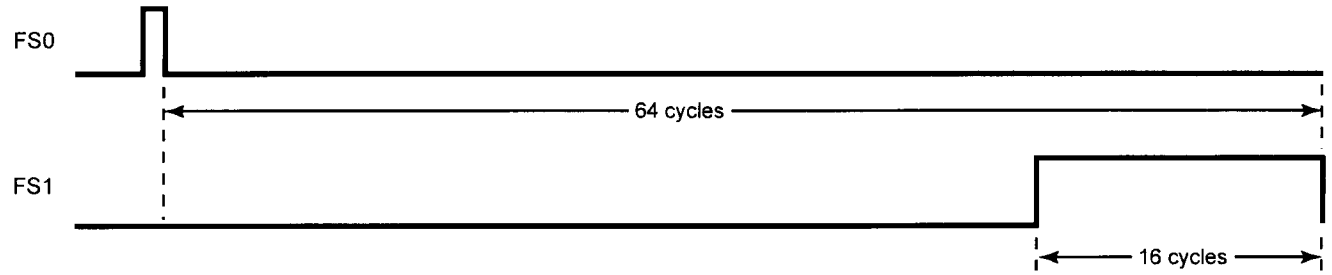


Figure 20. 64-Bit CODEC Frame Synchronization

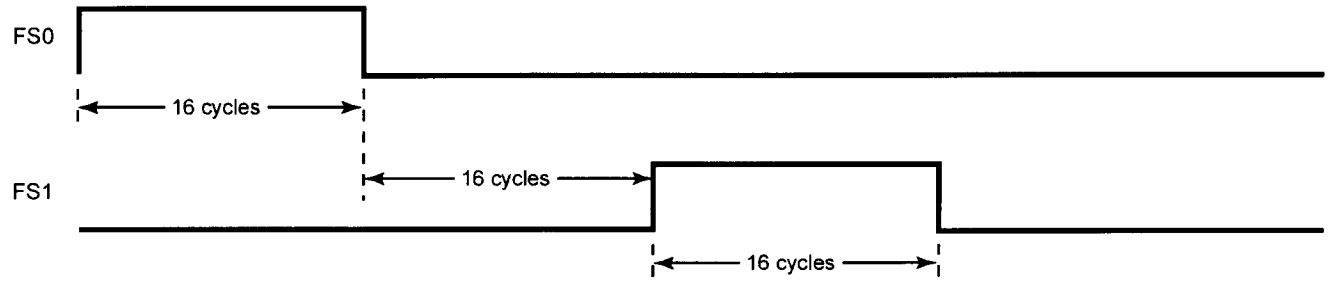


Figure 21. 16-Bit CODEC Frame Synchronization

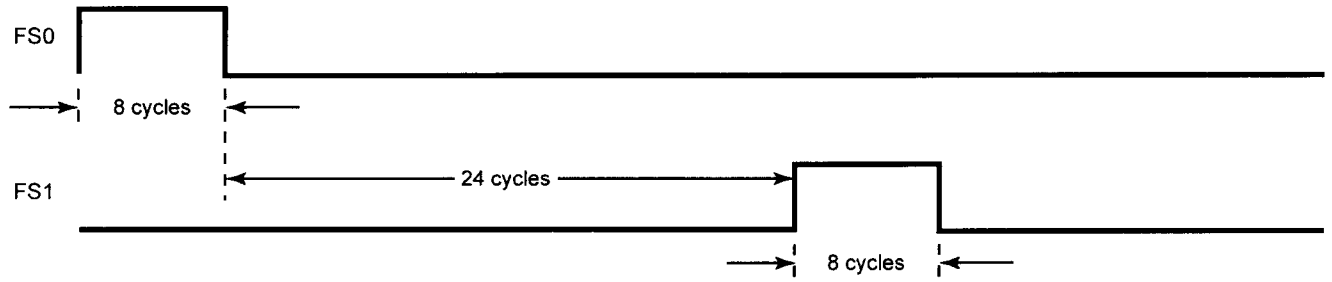


Figure 22. 8-Bit CODEC Frame Synchronization

CODEC INTERFACE (Continued)

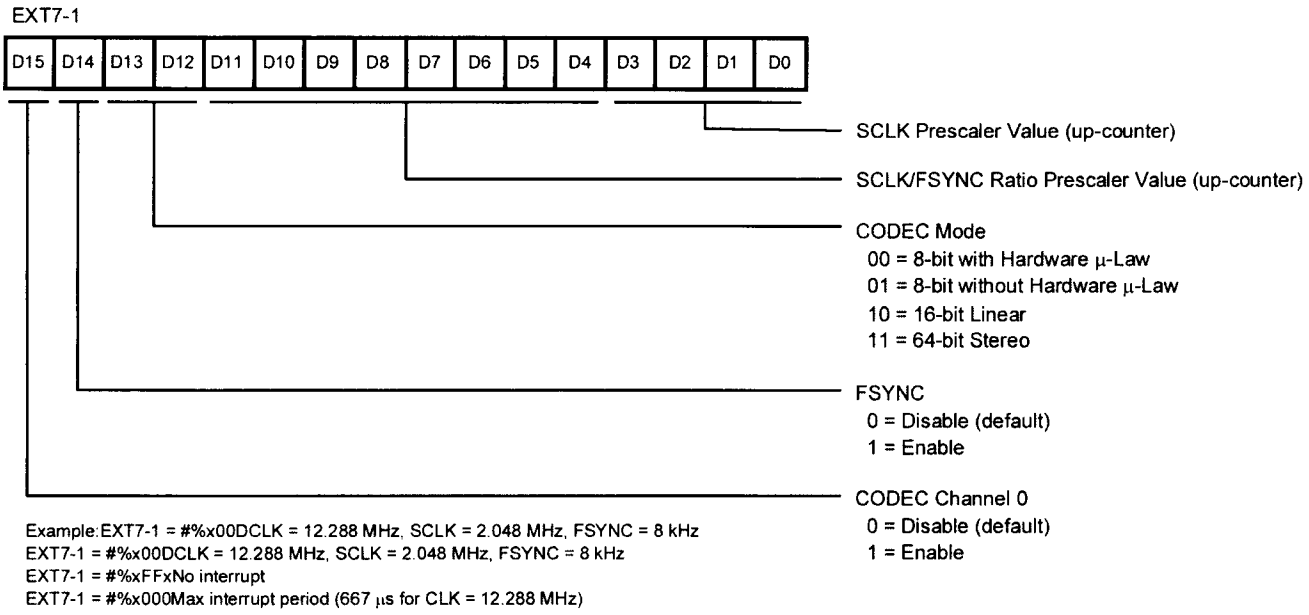


Figure 23. CODEC Interface Control Register

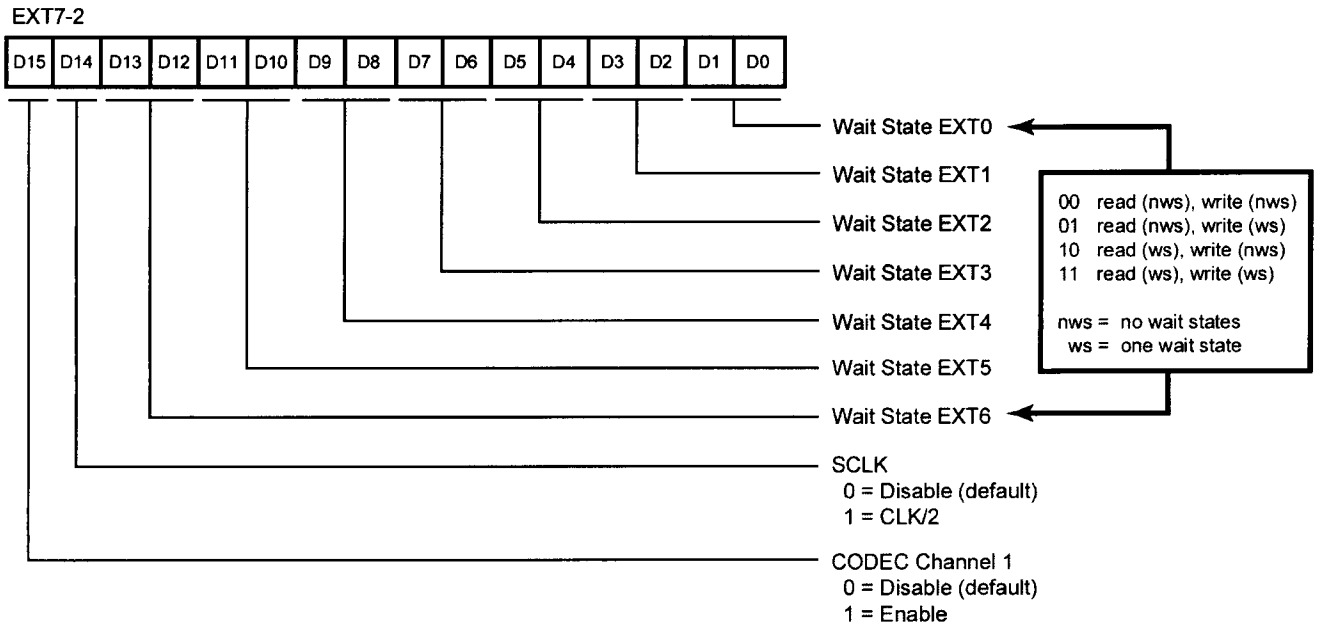


Figure 24. Wait-State Generator and CODEC Interface Control Register

INSTRUCTION SET

The addressing modes are:

<pregs>, <hwregs> These modes are used for loads to and from registers within the chip, such as loading to the accumulator, or loading from a pointer register. The names of the registers are specified in the operand field (destination first, then source).

<dregs> This mode is used for access to the lower 16 addresses in each bank of RAM. The 4-bit address comes from 2 bits of the status register and 2 bits of the operand field of the data pointer. Data registers can be used to access data in RAM, but typically these registers are used as pointers to access data from the program memory.

<accind> Similar to the previous mode, the address for the program memory read is stored in the Accumulator. Hence, @A in the second operand field loads the number in memory specified by the address in A.

<direct> The direct mode allows read or write to data RAM from the Accumulator by specifying the absolute address of the RAM in the operand of the instruction. A number between 0 and 255 indicates a location in RAM bank 0, and a number between 256 and 511 indicates a location in RAM bank 1.

<limm> This address mode indicates a long immediate operand. A 16-bit word can be loaded directly from the operand into the specified register or memory location.

<simm> This address mode indicates a short immediate operand. It is used to load 8-bit data into the specified RAM pointer.

<regind> This mode is used for indirect access to the data RAM. The address of the RAM location is stored in the pointer. The "@" symbol indicates "indirect" and precedes the pointer. For example, @P1:1 refers to the location in RAM bank 1 specified by the value in the pointer.

<memind> This mode is used for indirect access to the program memory. The address of the memory is located in a RAM location, which is specified by the value in a pointer. Therefore, @@P1:1 instructs the processor to read from a location in memory. This instruction specifies a value in RAM, and the location of the RAM is, in turn, specified by the value in the pointer.

Note: The data pointer can also be used for a memory access in this manner, but only one "@" precedes the pointer. In both cases, each time the addressing mode is used, the memory address stored in RAM is incremented by one to allow easy transfer of sequential data from program memory.

Table 9. Instruction Set Addressing Modes

Symbolic Name	Syntax	Description
<pregs>	Pn:b	Pointer Registers
<dregs> (points to RAM)	Dn:b	Data Registers
<hwregs>	X, Y, PC, SR, P, EDn, A, BUS	Hardware Registers
<accind> (points to Program Memory)	@A	Accumulator Memory Indirect
<direct>	<expression>	Direct Address Expression
<limm>	#<const exp>	Long (16-bit) Immediate Value
<simm>	#<const exp>	Short (8-bit) Immediate Value
<regind> (points to RAM)	@Pn:b	Pointer Register Indirect
	@Pn:b+	Pointer Register Indirect with Increment
	@Pn:b–LOOP	Pointer Register Indirect with Loop Decrement
	@Pn:b+LOOP	Pointer register Indirect with Loop Increment
<memind> (points to Program Memory)	@@Pn:b	Pointer Register Memory Indirect
	@Dn:b	Data Register Memory Indirect
	@@Pn:b–LOOP	Pointer Register Memory Indirect with Loop Decrement
	@@Pn:b+LOOP	Pointer Register Memory Indirect with Loop Increment
	@@Pn:b+	Pointer Register Memory Indirect with Increment

CONDITION CODES

The following Instruction Description defines the condition codes supported by the DSP assembler. If the instruction description refers to the < cc > (condition code) symbol in one of its addressing modes, the instruction will only execute if the condition is true.

Code	Description
C	Carry
EQ	Equal (same as Z)
F	False
IE	Interrupts Enabled
MI	Minus
NC	No Carry
NE	Not Equal (same as NZ)
NIE	No Interrupts Enabled
NOV	No Overflow
NU0	Not User Zero
NU1	Not User One
NZ	Not zero
OV	Overflow
PL	Plus (Positive)
U0	User Zero
U1	User One
UGE	Unsigned Greater Than or Equal (Same as NC)
ULT	Unsigned Less Than (Same as C)
Z	Zero

INSTRUCTION DESCRIPTIONS

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
ABS	Absolute Value	ABS[<cc>,]<src>	<cc>,A	1	1	ABS NC, A
			A	1	1	ABS A
ADD	Addition	ADD<dest>,<src>	A,<pregs>	1	1	ADD A,P0:0
			A,<dregs>	1	1	ADD A,D0:0
			A,<limm>	2	2	ADD A,#%1234
			A,<memind>	1	3	ADD A,@@P0:0
			A,<direct>	1	1	ADD A,%F2
			A,<regind>	1	1	ADD A,@P1:1
			A,<hwregs>	1	1	ADD A,X
			A,<simm>	1	1	ADD A, #%12
AND	Bitwise AND	AND<dest>,<src>	A,<pregs>	1	1	AND A,P2:0
			A,<dregs>	1	1	AND A,D0:1
			A,<limm>	2	2	AND A,#%1234
			A,<memind>	1	3	AND A,@@P1:0
			A,<direct>	1	1	AND A,%2C
			A,<regind>	1	1	AND A,@P1:2+LOOP
			A,<hwregs>	1	1	AND A,EXT3
			A,<simm>	1	1	AND A, #%12
CALL	Subroutine call	CALL [<cc>,]<address>	<cc>,<direct>	2	2	CALL Z,sub2
			<direct>	2	2	CALL sub1
CCF	Clear C flag	CCF	None	1	1	CCF
CIEF	Clear IE Flag	CIEF	None	1	1	CIEF
COPF	Clear OP flag	COPF	None	1	1	COPF
CP	Comparison	CP<src1>,<src2>	A,<pregs>	1	1	CP A,P0:0
			A,<dregs>	1	1	CP A,D3:1
			A,<memind>	1	3	CP A,@@P0:1
			A,<direct>	1	1	CP A,%FF
			A,<regind>	1	1	CP A,@P2:1+
			A,<hwregs>	1	1	CP A,STACK
			A,<limm>	2	2	CP A,#%FFCF
			A,<simm>	1	1	CP A, #%12
DEC	Decrement	DEC [<cc>,]<dest>	<cc>,A	1	1	DEC NZ,A
			A	1	1	DEC A
INC	Increment	INC [<cc>,] <dest>	<cc>,A	1	1	INC PL,A
			A	1	1	INC A
JP	Jump	JP [<cc>,]<address>	<cc>,<direct>	2	2	JP C,Label
			<direct>	2	2	JP Label
LD	Load destination with source	LD<dest>,<src>	A,<hwregs>	1	1	LD A,X
			A,<dregs>	1	1	LD A,D0:0
			A,<pregs>	1	1	LD A,P0:1
			A,<regind>	1	1	LD A,@P1:1
			A,<memind>	1	3	LD A,@D0:0
			A,<direct>	1	1	LD A,124
			<direct>,A	1	1	LD 124,A
			<dregs>,<hwregs>	1	1	LD D0:0,EXT7
			<pregs>,<simm>	1	1	LD P1:1,#%FA
			<pregs>,<hwregs>	1	1	LD P1:1,EXT1
			<regind>,<limm>	1	1	LD@P1:1,#1234
			<regind>,<hwregs>	1	1	LD @P1:1+,X
			<hwregs>,<pregs>	1	1	LD Y,P0:0
			<hwregs>,<dregs>	1	1	LD SR,D0:0
			<hwregs>,<limm>	2	2	LD PC,#%1234
			<hwregs>,<accind>	1	3	LD X,@A
			<hwregs>,<memind>	1	3	LD Y,@D0:0
			<hwregs>,<regind>	1	1	LD A,@P0:0–LOOP
			<hwregs>,<hwregs>	1	1	LD X,EXT6

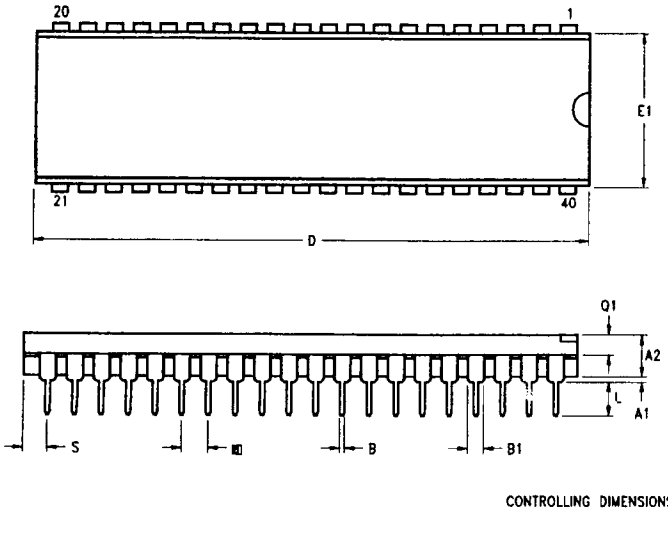
Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
Notes: 1. When <dest> is <hwregs>, <dest> cannot be P. 2. When <dest> is <hwregs> and <src> is <hwregs>, <dest> cannot be EXTn if <src> is EXTn, <dest> cannot be X if <src> is X, <dest> cannot be SR if <src> is SR. 3. When <src> is <accind> <dest> cannot be A.						
MLD	Multiply	MLD <src1>,<src2> [,<bank switch>]	<hwregs>,<regind> <hwregs>,<regind>, bank switch> <regind>,<regind> <regind>,<regind>, <bank switch>	1 1 1 1	1 1 1 1	MLD A,@P0:0+LOOP MLD A,@P1:0,OFF MLD @P1:1,@P2:0 MLD @P0:1,@P1:0,ON
Notes: 1. If src1 is <regind> it must be a bank 1 register. Src2's <regind must be a bank 0 register. 2. <hwregs> for src1 cannot be X. 3. For the operands <hwregs>, <regind> the <bank switch> defaults to OFF. For the operands <regind>, the <bank switch> defaults to ON.						
MPYA	Multiply and add	MPYA <src1>,<src2> [,<bank switch>]	<hwregs>,<regind> <hwregs>,<regind>, bank switch> <regind>,<regind> <regind>,<regind>, <bank switch>	1 1 1 1	1 1 1 1	MPYA A,@P0:0 MPYA A,@P1:0,OFF MPYA @P1:1,@P2:0 MPYA@P0:1,@P1:0,ON
Notes: 1. If src1 is <regind> it must be a bank 1 register. Src2's <regind> must be a bank 0 register. 2. <hwregs> for src1 cannot be X. 3. For the operands <hwregs>, <regind> the <bank switch> defaults to OFF. For the operands <regind>, the <bank switch> defaults to ON.						
MPYS	Multiply and subtract	MPYS <src1>,<src2> [,<bank switch>]	<hwregs>,<regind> <hwregs>,<regind>, bank switch> <regind>,<regind> <regind>,<regind>, <bank switch>	1 1 1 1	1 1 1 1	MPYS A,@P0:0 MPYS A,@P1:0,OFF MPYS @P1:1,@P2:0 MPYS @P0:1,@P1:0,ON
Notes: 1. If src1 is <regind> it must be a bank 1 register. Src2's <regind> must be a bank 0 register. 2. <hwregs> for src1 cannot be X. 3. For the operands <hwregs>, <regind> the <bank switch> defaults to OFF. For the operands <regind>, <regind> the <bank switch> defaults to ON.						
NEG	Negate	NEG <cc>,A	<cc>, A A	1 1	1 1	NEG MI,A NEG A
NOP	No operation	NOP	None	1	1	NOP
OR	Bitwise OR	OR <dest>,<src>	A,<pregs> A,<dregs> A,<limm> A,<memind> A,<direct> A,<regind> A,<hwregs> A,<simm>	1 1 2 1 1 1 1 1	1 1 2 3 1 1 1 1	OR A,P0:1 OR A, D0:1 OR A,#%2C21 OR A,@@P2:1+ OR A, %2C OR A,@P1:0–LOOP OR A,EXT6 OR A,#%12
POP	Pop value from stack	POP <dest>	<pregs> <dregs> <regind> <hwregs>	1 1 1 1	1 1 1 1	POP P0:0 POP D0:1 POP @P0:0 POP A

INSTRUCTION DESCRIPTIONS (Continued)

Inst.	Description	Synopsis	Operands	Words	Cycles	Examples
PUSH	Push value onto stack	PUSH <src>	<pregs>	1	1	PUSH P0:0
			<dregs>	1	1	PUSH D0:1
			<regind>	1	1	PUSH @P0:0
			<hwregs>	1	1	PUSH BUS
			<limm>	2	2	PUSH #12345
			<accind>	1	3	PUSH @A
			<memind>	1	3	PUSH @@P0:0
RET	Return from subroutine	RET	None	1	2	RET
RL	Rotate Left	RL <cc>,A	<cc>,A	1	1	RL NZ,A
			A	1	1	RL A
RR	Rotate Right	RR <cc>,A	<cc>,A	1	1	RR C,A
			A	1	1	RR A
SCF	Set C flag	SCF	None	1	1	SCF
SIEF	Set IE flag	SIEF	None	1	1	SIEF
SLL	Shift left logical	SLL	[<cc>,]A	1	1	SLL NZ,A
			A	1	1	SLL A
SOPF	Set OP flag	SOPF	None	1	1	SOPF
SRA	Shift right arithmetic	SRA<cc>,A	<cc>,A	1	1	SRA NZ,A
			A	1	1	SRA A
SUB	Subtract	SUB<dest>,<src>	A,<pregs>	1	1	SUB A,P1:1
			A,<dregs>	1	1	SUB A,D0:1
			A,<limm>	2	2	SUB A,#%2C2C
			A,<memind>	1	3	SUB A,@D0:1
			A,<direct>	1	1	SUB A,%15
			A,<regind>	1	1	SUB A,@P2:0–LOOP
			A,<hwregs>	1	1	SUB A,STACK
			A,<simm>	1	1	SUB A, #%12
XOR	Bitwise exclusive OR	XOR <dest>,<src>	A,<pregs>	1	1	XOR A,P2:0
			A,<dregs>	1	1	XOR A,D0:1
			A,<limm>	2	2	XOR A,#13933
			A,<memind>	1	3	XOR A,@@P2:1+
			A,<direct>	1	1	XOR A,%2F
			A,<regind>	1	1	XOR A,@P2:0
			A,<hwregs>	1	1	XOR A,BUS
			A,<simm>	1	1	XOR A, #%12

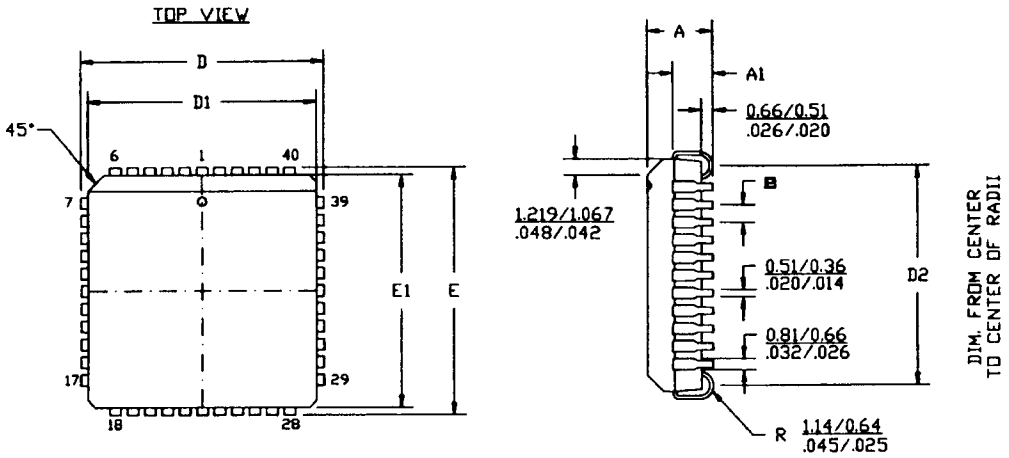
Bank Switch Operand. The third (optional) operand of the MLD, MPYA and MPYS instructions represents whether the bank switch is set ON or OFF. To more clearly represent this capacity, the keywords ON and OFF are used to state the status of the switch. These keywords are referenced in the instruction descriptions through the <bank switch> symbol. The most notable capability this item provides is that a source operand can be multiplied by itself (squared).

PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

Figure 25. 40-Pin Package Diagram

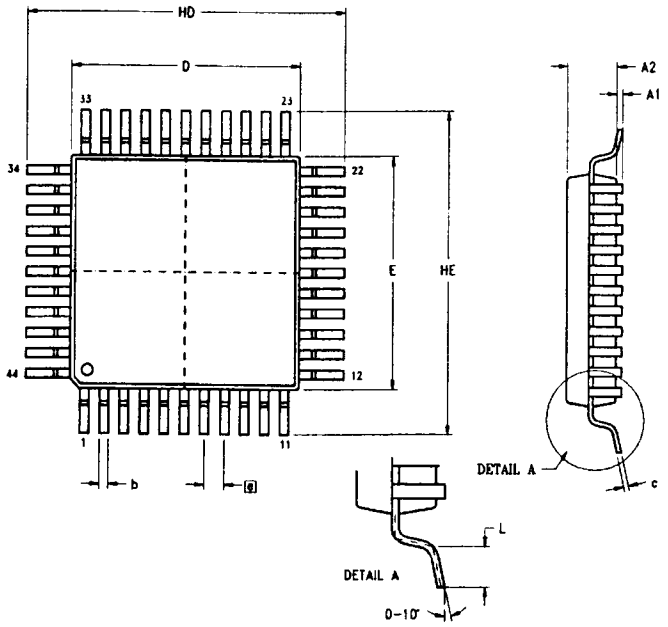


NOTES:
1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN.
3. DIMENSION : MM / INCH

SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	.168	.180
A1	2.41	2.92	.095	.115
D/E	17.40	17.65	.685	.695
D1/E1	16.51	16.66	.650	.656
D2	15.24	16.00	.600	.630
e	1.27 TYP		.050 TYP	

Figure 26. 44-Pin PLCC Package Diagram

PACKAGE INFORMATION (Continued)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.05	0.25	.002	.010
A2	2.00	2.25	.078	.089
b	0.25	0.45	.010	.018
c	0.13	0.20	.005	.008
HD	13.70	14.15	.539	.557
D	9.90	10.10	.390	.398
HE	13.70	14.15	.539	.557
E	9.90	10.10	.390	.398
e	0.80 TYP		.0315 TYP	
L	0.60	1.20	.024	.047

NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. LEAD COPLANARITY : MAX .10 (.004")

Figure 27. 44-Pin LQFP Package Diagram

ORDERING INFORMATION

Z89321
Z8932120PSC
Z8932120VSC
Z8932120VEC
Z8932120FSC
Z8932120FEC
Z89371
Z8937120PSC
Z8937120VSC
Z8937120FSC

For fast results, contact your local ZiLOG sales office for assistance in ordering the part desired.

Codes

Package	P = Plastic DIP
	V = Plastic PLCC
	F = Plastic LOFP
Temperature	S = 0°C to +70°C
	E = –40°C to 85°C
Speed	20 = 20 MHz
Environmental	C = Plastic Standard

Example:

Z 89321 20 V S C is a Z89321, 20 MHz, PLCC, 0° to +70°C, Plastic Standard Flow

- C — Environmental Flow
- S — Temperature
- V — Package
- 20 — Speed
- 89321 — Product Number
- Z — ZiLOG Prefix

Pre-Characterization Product:

The product represented by this document is newly introduced and ZiLOG has not completed the full characterization of the product. The document states what ZiLOG knows about this product at this time, but additional features or non-conformance with some aspects of the document may be found, either by ZiLOG or its customers in the course of further application and characterization work. In addition, ZiLOG cautions that delivery may be uncertain at times, due to start-up yield issues.

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For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at http://www.zilog.com/kb.

For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at http://support.zilog.com.