DSP56L307

24-Bit Digital Signal Processor

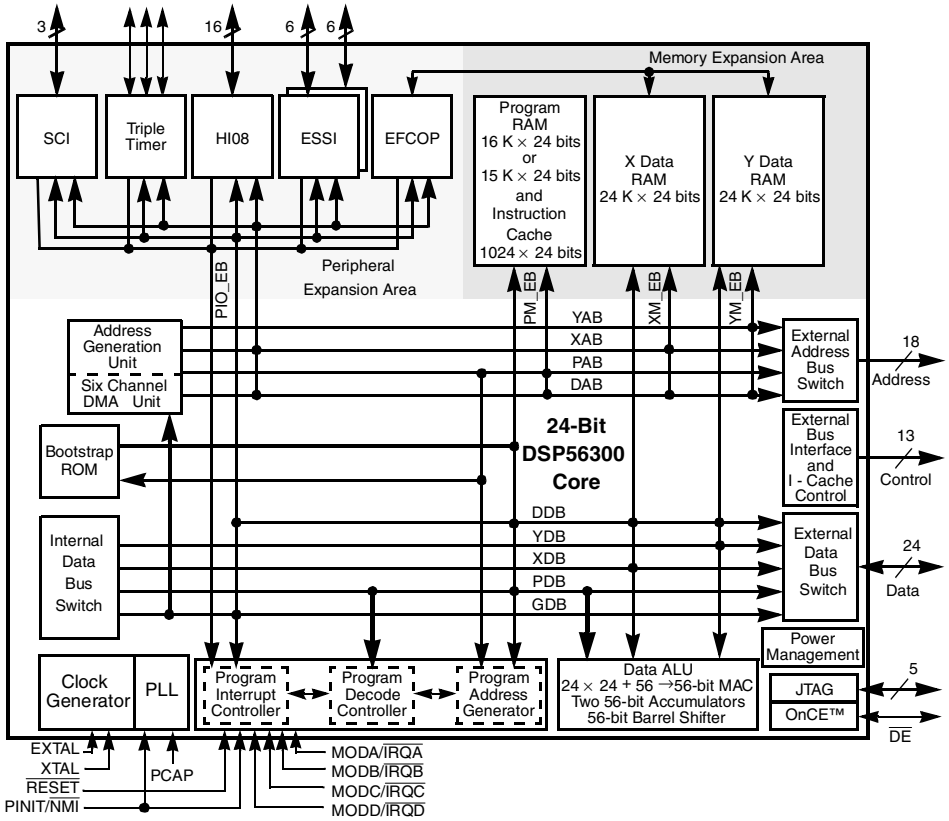

Figure 1. DSP56L307 Block Diagram

The DSP56L307 is intended for applications requiring a large amount of internal memory, such as networking and wireless infrastructure applications. The EFCOP can accelerate general filtering applications, such as echo-cancellation applications, correlation, and general-purpose convolution-based algorithms.

The Freescale DSP56L307, a member of the DSP56300 DSP family, supports network applications with general filtering operations. The Enhanced Filter Coprocessor (EFCOP) executes filter algorithms in parallel with core operations, enhancing signal quality with no impact on channel throughput or total channels supported. The result is increased overall performance. Like the other DSP56300 family members, the DSP56L307 uses a high-performance, single-clock-cycle-per- instruction engine (DSP56000 code-compatible), a barrel shifter, 24-bit addressing, an instruction cache, and a direct memory access (DMA) controller (see **Figure 1**). The DSP56L307 performs at 160 million multiply-accumulates per second (MMACS), attaining 320 MMACS when the EFCOP is in use. It operates with an internal 160 MHz clock with a 1.8 volt core and independent 3.3 volt input/output (I/O) power.

Note: This document contains information on a new product. Specifications and information herein are subject to change without notice.

Features

Table 1 lists the features of the DSP56L307 device.

Table 1. DSP56L307 Features

<table>
<tr><th>Feature</th><th>Description</th></tr>
<tr><td>High-Performance DSP56300 Core</td><td>
• 160 million multiply-accumulates per second (MMACS) (321 MMACS using the EFCOP in filtering applications) with a 160 MHz clock at 1.8 V core and 3.3 V I/O
• Object code compatible with the DSP56000 core with highly parallel instruction set
• Data arithmetic logic unit (Data ALU) with fully pipelined 24 × 24-bit parallel multiplier-accumulator (MAC), 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing), conditional ALU instructions, and 24-bit or 16-bit arithmetic support under software control
• Program control unit (PCU) with position-independent code (PIC) support, addressing modes optimized for DSP applications (including immediate offsets), internal instruction cache controller, internal memory-expandable hardware stack, nested hardware DO loops, and fast auto-return interrupts
• Direct memory access (DMA) with six DMA channels supporting internal and external accesses; one-, two- and three-dimensional transfers (including circular buffering); end-of-block-transfer interrupts; and triggering from interrupt lines and all peripherals
• Phase-lock loop (PLL) allows change of low-power divide factor (DF) without loss of lock and output clock with skew elimination
• Hardware debugging support including on-chip emulation (OnCE) module, Joint Test Action Group (JTAG) test access port (TAP)
</td></tr>
<tr><td>Enhanced Filter Coprocessor (EFCOP)</td><td>
• Internal 24 × 24-bit filtering and echo-cancellation coprocessor that runs in parallel to the DSP core
• Operation at the same frequency as the core (up to 160 MHz)
• Support for a variety of filter modes, some of which are optimized for cellular base station applications:
  • Real finite impulse response (FIR) with real taps
  • Complex FIR with complex taps
  • Complex FIR generating pure real or pure imaginary outputs alternately
  • A 4-bit decimation factor in FIR filters, thus providing a decimation ratio up to 16
  • Direct form 1 (DFI) Infinite Impulse Response (IIR) filter
  • Direct form 2 (DFII) IIR filter
  • Four scaling factors (1, 4, 8, 16) for IIR output
  • Adaptive FIR filter with true least mean square (LMS) coefficient updates
  • Adaptive FIR filter with delayed LMS coefficient updates
</td></tr>
<tr><td>Internal Peripherals</td><td>
• Enhanced 8-bit parallel host interface (HI08) supports a variety of buses (for example, ISA) and provides glueless connection to a number of industry-standard microcomputers, microprocessors, and DSPs
• Two enhanced synchronous serial interfaces (ESSI), each with one receiver and three transmitters (allows six-channel home theater)
• Serial communications interface (SCI) with baud rate generator
• Triple timer module
• Up to 34 programmable general-purpose input/output (GPIO) pins, depending on which peripherals are enabled
</td></tr>
<tr><td>Internal Memories</td><td>
• 192 × 24-bit bootstrap ROM
• 192 K × 24-bit RAM total
• Program RAM, instruction cache, X data RAM, and Y data RAM sizes are programmable:
<table>
<tr><th>Program RAM Size</th><th>Instruction Cache Size</th><th>X Data RAM Size*</th><th>Y Data RAM Size*</th><th>Instruction Cache</th><th>Switch Mode</th><th>MSW1</th><th>MSW0</th></tr>
<tr><td>16 K × 24-bit</td><td>0</td><td>24 K × 24-bit</td><td>24 K × 24-bit</td><td>disabled</td><td>disabled</td><td>0/1</td><td>0/1</td></tr>
<tr><td>15 K × 24-bit</td><td>1024 × 24-bit</td><td>24 K × 24-bit</td><td>24 K × 24-bit</td><td>enabled</td><td>disabled</td><td>0/1</td><td>0/1</td></tr>
<tr><td>48 K × 24-bit</td><td>0</td><td>8 K × 24-bit</td><td>8 K × 24-bit</td><td>disabled</td><td>enabled</td><td>0</td><td>0</td></tr>
<tr><td>47 K × 24-bit</td><td>1024 × 24-bit</td><td>8 K × 24-bit</td><td>8 K × 24-bit</td><td>enabled</td><td>enabled</td><td>0</td><td>0</td></tr>
<tr><td>40 K × 24-bit</td><td>0</td><td>12 K × 24-bit</td><td>12 K × 24-bit</td><td>disabled</td><td>enabled</td><td>0</td><td>1</td></tr>
<tr><td>39 K × 24-bit</td><td>1024 × 24-bit</td><td>12 K × 24-bit</td><td>12 K × 24-bit</td><td>enabled</td><td>enabled</td><td>0</td><td>1</td></tr>
<tr><td>32 K × 24-bit</td><td>0</td><td>16 K × 24-bit</td><td>16 K × 24-bit</td><td>disabled</td><td>enabled</td><td>1</td><td>0</td></tr>
<tr><td>31 K × 24-bit</td><td>1024 × 24-bit</td><td>16 K × 24-bit</td><td>16 K × 24-bit</td><td>enabled</td><td>enabled</td><td>1</td><td>0</td></tr>
<tr><td>24 K × 24-bit</td><td>0</td><td>20 K × 24-bit</td><td>20 K × 24-bit</td><td>disabled</td><td>enabled</td><td>1</td><td>1</td></tr>
<tr><td>23 K × 24-bit</td><td>1024 × 24-bit</td><td>20 K × 24-bit</td><td>20 K × 24-bit</td><td>enabled</td><td>enabled</td><td>1</td><td>1</td></tr>
<tr><td colspan="8">*Includes 4 K × 24-bit shared memory (that is, memory shared by the core and the EFCOP)</td></tr>
</table>
</td></tr>
</table>

Table 1. DSP56L307 Features (Continued)

Feature	Description
External Memory Expansion	• Data memory expansion to two 256 K × 24-bit word memory spaces using the standard external address lines • Program memory expansion to one 256 K × 24-bit words memory space using the standard external address lines • External memory expansion port • Chip select logic for glueless interface to static random access memory (SRAMs) • Internal DRAM Controller for glueless interface to dynamic random access memory (DRAMs) up to 100 MHz operating frequency
Power Dissipation	• Very low-power CMOS design • Wait and Stop low-power standby modes • Fully static design specified to operate down to 0 Hz (dc) • Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)
Packaging	• Molded array plastic-ball grid array (MAP-BGA) package in lead-free or lead-bearing versions.

Target Applications

- Wireless and wireline infrastructure applications
- Multi-channel wireless local loop systems
- DSP resource boards
- High-speed modem banks
- Packet telephony

Product Documentation

The documents listed in **Table 2** are required for a complete description of the DSP56L307 device and are necessary to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, or a Freescale Semiconductor Literature Distribution Center. For documentation updates, visit the Freescale DSP website. See the contact information on the back cover of this document.

Table 2. DSP56L307 Documentation

Name	Description	Order Number
DSP56L307 Technical Data	Description, features list, and specifications of the DSP56L307	DSP56L307
DSP56L307 User's Manual	Detailed functional description of the DSP56L307 memory configuration, operation, and register programming	DSP56L307UM
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM
Application Notes	Documents describing specific applications or optimized device operation including code examples	See the DSP56L307 product website

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