FEATURES

- **TI AM572x/AM574x Sitara Processor**
  - **1.5 GHz Dual ARM Cortex-A15**
    - ARM Neon and HW floating point
    - 32 KB L1 Program/Data Cache
    - 2 MB L2 cache
  - **Up to 2 C66x floating-point DSPs**
    - 750 MHz operation
    - 32 KB L1 Program/Data Cache
    - 288 KB Internal SRAM
  - **Hardware Acceleration**
    - Power VR SGX544 3D GPU
    - H.264 Video Encode/Decode
    - Up to 4 Embedded Vision Engines
    - 2x ARM Cortex-M4 co-processors
    - 2x dual-core PRUs
    - Crypto Hardware accelerators
- **On-Board Xilinx Artix-7 FPGA**
  - Up to XC7A50T
    - Up To 2,700 KBits Block RAM
    - Up To 52,160 Logic Cells
  - PCIe Interface to AM57x
  - 2 Transceivers available for external IO
- Up To 4 GB DDR3 RAM on dual banks
- Up To 32 MB QSPI based NOR FLASH
- Integrated Power Management
- Dual Edge and Board to Board Connectors
  - **96 FPGA I/O Pins**
  - **Up To 199 AM57xx Multiplexed IO's**
    - 2x 10/100/1000 EMAC / MDIO
    - 2x 10/100 EMAC supporting EtherCAT
    - McASP (audio) interface
    - Camera/Video Input
    - 2x MMC/SD
    - 3x I2C, 3x UART
  - 1x USB 2.0 dual-role
  - 1x USB 3.0 dual-role
  - SATA-2 (6 Gbps)
  - HDMI 1.4a Output

APPLICATIONS

- Embedded Instrumentation
- Factory Automation
- Industrial Communication
- Grid Infrastructure
- Industrial Drives
- Medical Instrumentation
- Embedded Control Processing
- Network Enabled Data Acquisition
- Test and Measurement
- Software Defined Radio
- Power Protection Systems
- Embedded Cameras
- Smart Vision Systems

BENEFITS

- Rapid Development / Deployment
- Multiple Connectivity and Interface Options
- Rich User Interfaces
- High System Integration
- Fixed & Floating Point Operations
- High-Level OS Support
  - Linux
  - Android
- Embedded Digital Signal Processing

DESCRIPTION

The MitySOM-AM57F is a highly configurable, very small form-factor processor card that features a Texas Instruments AM57xx series 1.5 GHz Sitara Processor tightly integrated with the Xilinx Artix-7 Field Programmable Gate Array (FPGA), NOR FLASH and DDR3 RAM memory subsystems. The design of the MitySOM-AM57F allows end-users the capability to develop programs/logic images for all of the compute elements on the AM57xx as well as for the FGPA. The MitySOM-AM57F provides a complete and flexible digital processing infrastructure necessary for the most demanding embedded applications development.

The onboard processor provides a dual CPU core topology. The Sitara AM57xx processor family includes a dual ARM Cortex-A15 microprocessor unit (MPU) subsystem capable of running the rich software applications programmer interfaces (APIs) expected by modern system designers. The ARM architecture supports several operating systems, including Linux and Android. In addition to the MPU, the AM57xx also includes up to two DSP C66x floating-point digital signal processing (DSP) core. The DSP core supports the freely provided TI SYSBIOS real-time kernel. Users can leverage the DSP to execute real-time compute algorithms (codecs, image/data processing, compression techniques, filtering, etc.).

For additional acceleration, the AM5xx provides 2 Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS) processing modules, and options are available for up to 4 Embedded Vision Engines (EVE), programmable image and vision processing engines.

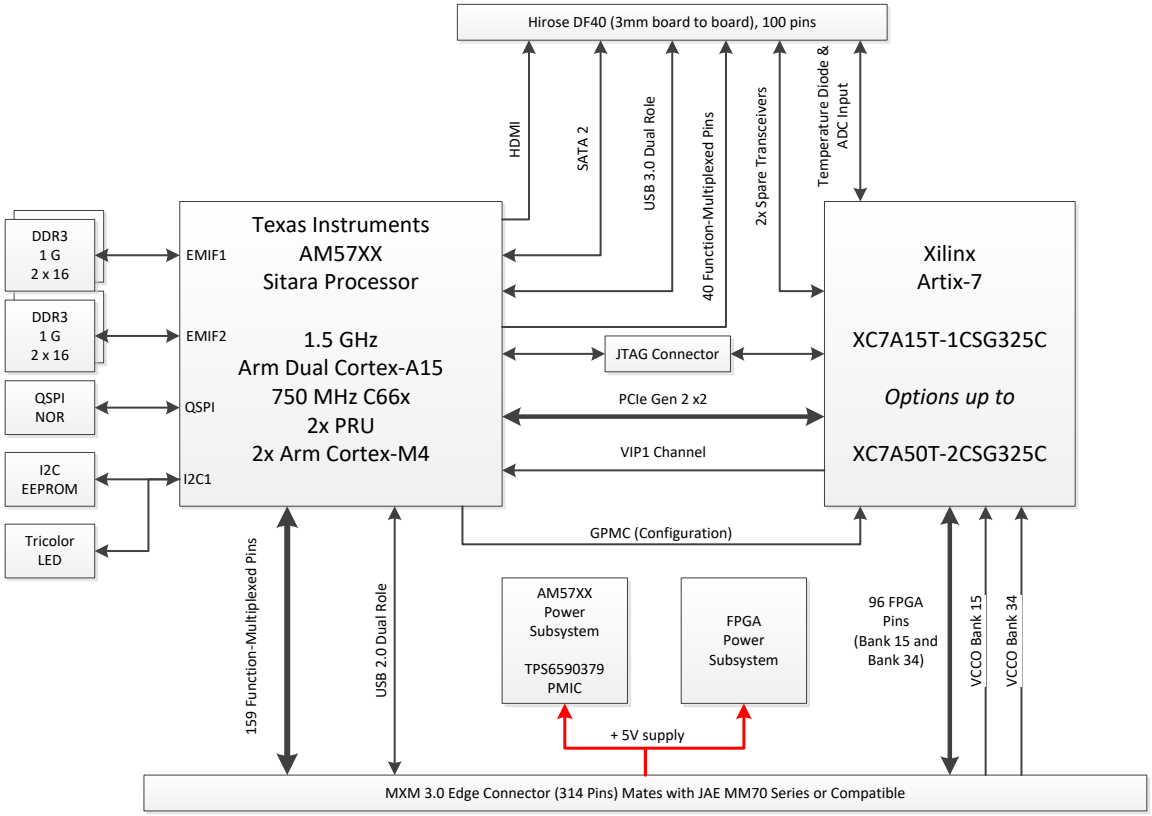

Figure 1 MitySOM-AM57F Block Diagram

Figure 1 provides a top-level block diagram of the MitySOM-AM57F processor card. As shown in the figure, there are two main interfaces to the module: a 314 pin Mobile PCI Express Module (MXM) style card-edge connector (J1), with 310 positions utilized, and a 100 pin Hirose DF40 series board-to-board connector (J3). The MXM card-edge connector interface provides power, 155 function multiplex pins from the Sitara processor (supporting 2x RGMII Ethernet MACs, 2x MII Ethercat master or slave interfaces, multiple I2C, UART, digital audio and SPI peripherals as well as standard GPIO), and up to 96 pins of configurable FPGA I/O for application-defined interfacing. The Hirose connector provides a high-speed interface for the AM57xx HDMI, SATA, and USB 3.0 interfaces as well as 2 spare FPGA transceiver lanes.

FPGA Bank I/O

The MitySOM-AM57F provides 96 lines of FPGA I/O directly to the MXM card-edge interface. The 96 lines of FPGA I/O are distributed evenly across 2 banks of the FPGA, Bank 15 and Bank 34. These I/O lines and their associated logic are completely configurable within the FPGA at the end user's discretion.

With the Xilinx Artix-7 series FPGA, up to the XC7A50T, each of the user-controlled banks may be configured to operate on a different electrical interface standard based on input voltage provided at the card-edge connector. The banks support 3.3V, 2.5V, and 1.8V standard CMOS switching level technology depending on the voltage supplied to VCCO_34_EXT (for bank 34) and VCCO_15_EXT (for bank 15) pins on J1. These pins must be powered externally based on the application requirements. For 3.3V or 1.8V levels, the VDD_1V8F or PS_3V3 output supplies on J1 may be used to power VCCO_34_EXT and VCCO_15_EXT. If 2.5V is required (e.g., to support LVDS or 2.5V voltage standards) then an external 2.5V supply must be connected to these pins.

In addition, the I/O lines from the FPGA have been routed as differential pairs and support higher speed LVDS standards as well as SSTL 2.5 switching standards. Various forms of termination (pull-up/pull-down, digitally controlled impedance matching) are available within the FPGA switch fabric. Refer to the Xilinx Artix-7 user's guide for more information.

The FPGA pins are configured to present a weak pull-up resistance (minimum 8.2K ohm) to VCCO prior to bitstream configuration loading. Designers should consider any power on requirements for FPGA controlled pins and use pull-down resistors as required.

FPGA Transceiver Support

Two spare transceiver lanes and a reference clock input of the Artix-7 have been routed to J3 on the MitySOM-AM57F interface. These lanes may be used for high-speed interfacing at the user's discretion. These lanes are not decoupled.

AM57xx DDR3 Memory Interface

The AM57xx processor includes two dedicated 32-bit DDR3 1066 SDRAM external memory interfaces (EMIF) shared between the onboard ARM, DSP, and hardware acceleration modules. Each bank is configured with up to 2 GB of DDR3, resulting in 4 GB available memory for the processor subsystem. Each bank is capable of burst bandwidths up to 4,264 MB/sec.

AM57xx QSPI NOR FLASH Interface

The MitySOM-AM57F includes up to 32 MB of Quad-SPI NOR FLASH. This FLASH memory is intended to store a factory provided bootloader, and typically a compressed image of a Linux kernel for the ARM core processor if alternate boot media such as Micro-SD card or eMMC is not available.

AM57xx Video Interfaces

The AM57xx includes a dedicated HDMI 1.4a output interface and up to 3 Display Parallel Interface (DPI) Video Output Ports as indicated in the Multifunction IO pins in the interfaces section. The AM57xx provides 2 Video Input Ports. One is available directly on the Multifunction IO pins and a second video input port (VIP1) has been routed directly to the on-board FPGA to support interfacing to custom sensors with the FPGA and feeding the data directly to the AM57xx for processing.

AM57xx USB Interfaces

The AM57xx processor includes provisions for one USB 3.0 SuperSpeed (SS) dual-role and a second USB 2.0 dual-role device. Both of these interfaces have been routed to the external interface connectors (USB 3.0 on J3, USB 2.0 on J1) for connection to a carrier card. The USB 3.0 SS TX data lanes have been AC coupled on the SOM with 0.1uF ceramic decoupling capacitors.

The USB_VBUS (pin 240 J1) signal is connected to a comparator on the SOM's TPS6590379 VBUS pin. When USB_VBUS is greater than 2.9V, its VBUSDET signal will go high which is connected to

GPIO4_22 on the SOM. This is used by the USB driver to detect USB insertion and enable/disable USBx_DRVVBUS. If not used, this pin should be pulled to ground.

AM57xx SATA Interface

The AM57xx processor includes a physical interface and driver for a SATA-II data channel interface. The signals for this interface have been routed to the J3 connector. These signals have been AC coupled using a 0.01uF ceramic capacitor.

AM57xx Multifunction Input/Output (MFIO) Interfaces

The MitySOM-AM57F routes more than 200 multifunction IO pins from the AM57x to the external J1 or J3 connectors on the module for customer use. All of the pins operate on a 1.8V voltage domain excluding the mmc1 pins (vddshv8/LDO1) which default to 3.3V. The specific connection and available functions are included in the connector descriptions in the following sections. Functions supported include:

- Up to 10 UARTS
- Up to 3 SPI busses
- Up to 1 McASP port with up to 7 data lanes
- Up to 2 DCAN busses
- Up to 2 RGMII busses
- Up to 2 additional MII busses supporting Ethercat master and slave
- Up to 4 I2C busses
- Up to 3 MMC/SD IO interfaces

The MitySOM-AM57F does use some AM57xx multi-function pins as dedicated functions on the SOM, including:

- UART3 (balls D27, C28) as a dedicated console port
- I2C1 (balls C20, C21) used to communicate to the following peripherals:
  - Factory configuration EEPROM (24AA32AFT, Address 7b1010xxx)
  - RGB LED controller (TCA6507RUER, Address 7b1000101)
  - Power Management IC (TPS6590379ZWST, Address 7b10010xx)
- GPIO1[0] (ball AD17) used for PMIC interrupts
- GPIO2[21] (ball P1) used for FPGA init status
- GPIO2[28] (ball N2) used for FPGA programming status
- GPIO3[23] (ball AE1) used to control the PCIe reset signal to the FPGA
- GPIO4[22] (ball C11) used for VBUS_DET signal from PMIC
- GPIO7[11] (ball A22) used to control DDR VTT termination
- VIN4a interface (24-bit wide) connected to FPGA, pins de0, fld0, hsync0, and vsync0 are not used and should be available
- CPU_NMIn (ball D21) connected to FPGA pin for FPGA driven NMI
- SYS_NIRQ1/SYS_NIRQ2 (balls AB16, AC16) connected to FPGA pins for system interrupts
- GPMC interface (16 bit wide) connected to the FPGA for slave select configuration and register manipulation
- QSPI (balls P2, R2, P3, R3, U1, U2, and T2) to support up to 32MB of bootable QSPI NOR

AM57xx Boot Media Mode

The MitySOM-AM57F can be configured to boot using 2 different boot sequences according to the AM57_BOOT_MODE pin (J3 - Pin 74). The pin is pulled up to +1.8V on the SOM and results in the default boot mode being the “high” mode shown below. If the “low” mode is desired this signal should be pulled to GND on the carrier board.

- The boot sequence when AM57_BOOT_MODE **high** is:
  - SD card (MMC1 - Table 1)
  - eMMC (MMC2 - Table 2)
  - HS USB 2.0 (USB1 - Table 3)
- The boot sequence when AM57_BOOT_MODE **low** is:
  - On SOM Quad SPI NOR (QSPI1 - Table 4)
  - SD card (MMC1 - Table 1)
  - HS USB 2.0 (USB1 - Table 3)

Table 1: SD Card (MMC1) Boot Mode Signals

Interface Signal	AM57xx Ball	MitySOM-AM57F Pin
mmc1_clk	W6	J1 – Pin 165
mmc1_cmd	Y6	J1 – Pin 167
mmc1_dat0	AA6	J1 – Pin 175
mmc1_dat1	Y4	J1 – Pin 173
mmc1_dat2	AA5	J1 – Pin 171
mmc1_dat3	Y3	J1 – Pin 169

Table 2: eMMC (MMC2) Boot Mode Signals

Interface Signal	AM57xx Ball	MitySOM-AM57F Pin
mmc2_clk	J7	J1 – Pin 135
mmc2_cmd	H6	J1 – Pin 137
mmc2_dat0	J4	J1 – Pin 139
mmc2_dat1	J6	J1 – Pin 141
mmc2_dat2	H4	J1 – Pin 143
mmc2_dat3	H5	J1 – Pin 145
mmc2_dat4	K7	J1 – Pin 147
mmc2_dat5	M7	J1 – Pin 149
mmc2_dat6	J5	J1 – Pin 151
mmc2_dat7	K6	J1 – Pin 153

Table 3: HS USB 2.0 (USB1) Boot Mode Signals

Interface Signal	AM57xx Ball	MitySOM-AM57F Pin
usb1_dp	AC12	J3 – Pin 45
usb1_dm	AD12	J3 – Pin 43

Table 4: On-SOM QSPI NOR (QSPI1) Boot Mode Signals

Interface Signal	AM57xx Ball	MitySOM-AM57F Pin
qspi1_rtclk	R3	N/A
qspi1_sclk	R2	N/A
qspi1_cs0	P2	N/A
qspi1_d0	U1	N/A
qspi1_d1	P3	N/A
qspi1_d2	U2	N/A
qspi1_d3	T2	N/A

AM57xx Secure Boot Features

Secure boot features are available with MitySOM-AM57F modules that feature the AM5748 and AM5749 processors. Please contact your Critical Link sales representative for additional details if you require this feature.

Power Interface

The MitySOM-AM57F is powered via a +5.0V external supply on the VDD_5V0 pins and via the VCCO_34_EXT and VCCO_15_EXT pins.

The MitySOM-AM57F leverages a TPS659037 power management IC for managing the power sequencing/monitoring of the AM57xx. The PMIC will automatically power on when power is applied and the U-boot initialization code will set DEV_CTRL.DEV_ON to 1 to keep the PMIC powered on. This allows the software to power off the SOM at the end of power down by setting this bit to 0. The PMIC_POWERHOLD signal (PMIC ball G9), which is available external to the module at J1 Pin E3-7 should be left floating in this scenario.

Alternatively, control of the module's power state, on/off, from the baseboard can be accomplished with the PMIC_POWERHOLD signal, PMIC ball G9, which is available external to the module at J1 Pin E3-7. Driving this signal high allows the module to stay on and pulling this signal low will cause the PMIC to

begin its sequential power down process. Note this does not allow the OS to power down safely, it needs to be told to shut down separately and shutdown needs to complete before this signal goes low.
Additional supply management is performed on board to support the proper powering of the on-board DDR3 and FPGA core voltages. The FPGA bank voltages for the bank 15 and bank 34 pins must be provided externally and can be either 3.3V, 2.5V or 1.8V.

Debug LEDs

There are 3 debug LEDs on the MitySOM-AM57F module. Two are an on/off status LED tied to a specific condition and the other is controlled by software through the LED controller, TCA6507RUER, on the I2C1 interface.

Power Debug LED

D2 (POK) indicates that the module power sequence has completed successfully by lighting this yellow LED. The LED is enabled from the "PMIC_POWERGOOD" output which is also exposed at the card-edge connector pin E3-6 of the module.

Configuration Debug LED

D8 (DONE) indicates that the FPGA configuration is loaded by lighting a yellow LED. The FPGA can be loaded by the ARM in U-boot.

I2C Controllable LED

D1 is an RGB LED that is software controllable by the TCA6507RUER connected to the I2C1 interface of the AM57xx processor.

Green – U-boot turns on this LED when its loaded then off when it finishes.
Blue – The Kernel uses this LED to indicate SD card (mmc0) activity.

Software and Application Development Support

Users of the MitySOM-AM57F are encouraged to develop applications and FPGA firmware using the hardware and software development kit provided by Critical Link. The development kit includes a board support package providing a Linux based distribution and compatible GCC compiler toolchain with debugger based on the TI Linux Software Development Kit. In addition, the development kit includes support libraries necessary to program the DSP core using the TI Code Composer Studio DSP compiler toolchain.

To support rapid FPGA and application development, several example projects are provided that demonstrate using both the 16-bit general-purpose memory controller (GPMC) and the PCIe interface between the FPGA and the AM57xx processor.

Growth Options

The MitySOM-AM57F has been designed to support several options to provide customers with the ability to cost-optimize solutions for production volumes based on their project technical needs. These options include various processor options, memory configurations, FPGA densities, and operating temperature specifications including commercial and industrial temperature ranges. The available options are listed in the section below, containing ordering information. For additional ordering information and details regarding these options, or to inquire about a particular configuration not listed below, please contact Critical Link at info@criticallink.com.

ABSOLUTE MAXIMUM RATINGS

Maximum Supply Voltage, Vcc	5.5 V
Storage Temperature Range	-65ºC to 80ºC
Shock, Z-Axis	±10 g
Shock, X/Y-Axis	±10 g

OPERATING CONDITIONS

Ambient Temperature Range Commercial	0ºC to 70ºC
Ambient Temperature Range Industrial	-40ºC to 85ºC
Humidity	0 to 95% Non-condensing
MIL-STD-810F	Contact Critical Link for Details

The following are the minimum temperature ratings for the components that are installed on a MitySOM-AM57F. For specifications not contained in this table please contact a Critical Link sales representative. Please see the Thermal Management section below for additional information.

Table 5: Module Component Temperature Rating (minimum)

Temperature Range Description	Component Ratings (minimum)
Commercial (-RC model number)	0°C to 70°C
Industrial (-RI model number)	-40°C to 85°C

Thermal Management

The MitySOM-AM57F module requires consideration of thermal management depending on processor selection, loading, and other considerations. Thermal management is a system-level issue that must be addressed in conjunction with the overall system design. Every end product is different and it is advisable to perform thorough testing to ensure that the product will meet desired performance and longevity specifications.

Critical Link has developed a sample heat-spreader that is compatible with the MitySOM-AM57F. Please contact your Critical Link representative for further details and ordering information.

Card-Edge Interface Description (J1)

The first interface connector for the MitySOM-AM57F is the MXM style 314 pin card-edge interface with 310 positions utilized. The Keys are shown in the numbering but no actual pins exist. The connector interface uses 310-pins counted as follows: 281 total “pins”, minus 7 for the “keys”, plus 36 for the E1, E2, E3, and E4 pin-groups as four of these are no connects “NC”. This allows the module to be compatible with either 314 or 310 loaded position MXM connectors.

The interface contains 6 types of signals:

- Power input and ground/return (PWR / GND)
- Pins mapped to the Xilinx Artix-7 Device (FPGA)
- Multi-function signals mapped to the AM57XX device (MFIO)
- Module fixed-function pins (FF)
- Dedicated signals mapped to the Power Management IC (PMIO)
- Power output pins that may be used for driving the FPGA bank voltages (OUT)

Table 6 contains a summary of the MitySOM-AM57F MXM card-edge interface pin mapping which includes:

- Connector pin assignment
- Voltage domains (where B15 and B34 indicate Artix 7 Bank 15 and 34 Voltages)

- FPGA or AM57XX ball for direct connect pins
- Signal Options / name for each pin
    - For FPGA connections, the signal option name is of the form IO_<BANK>_<LVDSPAIR>_<N/P>

Card-Edge Mating Connector

The MitySOM-AM57F module mates with two connectors, J1 & J3, which contain the power and I/O connections for the module. The primary connector is J1 which is the card-edge interface based on the MXM connector standard.

Due to the secondary connector, J3, being a 3.0mm board to board height connector the primary connector must result in a similar board height. Critical Link recommends that a 3.0mm board height MXM connector be used, such as the JAE MM70-314 series, specifically the "-R300" option, however other connectors may be used as long as the board to board height is +/- 10%; 2.7mm to 3.3mm.

Please see our Wiki pages on our Redmine site at support.criticallink.com for up to date compatible connector options.

Table 6 J1 Pin-Out

Pin	Type	Volt	fpga ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
1	FPGA	B15	B17	-	IO_15_L16_N												
2	FPGA	B15	C18	-	IO_15_L18_N												
3	FPGA	B15	C16	-	IO_15_L16_P												
4	FPGA	B15	D18	-	IO_15_L17_N												
5	FPGA	B15	D16	-	IO_15_L14_N		SRCC_N										
6	FPGA	B15	E17	-	IO_15_L17_P												
7	FPGA	B15	E16	-	IO_15_L14_P		SRCC_P										
8	GND	-	-	-	GND												
9	FPGA	B15	F15	-	IO_15_L21_N												
10	FPGA	B15	E18	-	IO_15_L24_N												
11	FPGA	B15	G15	-	IO_15_L21_P												
12	FPGA	B15	F17	-	IO_15_L24_P												
13	GND	-	-	-	GND												
14	FPGA	B15	F18	-	IO_15_L19_N												
15	FPGA	B15	G16	-	IO_15_L20_N												
16	FPGA	B15	G17	-	IO_15_L19_P												
17	FPGA	B15	H16	-	IO_15_L20_P												
18	FPGA	B15	H18	-	IO_15_L23_N												
19	FPGA	B15	C11	-	IO_15_L4_P												
20	FPGA	B15	H17	-	IO_15_L23_P												
21	FPGA	B15	B11	-	IO_15_L4_N												
22	FPGA	B15	C8	-	IO_15_L1_N	AD0N											
23	FPGA	B15	A13	-	IO_15_L8_P	AD10P											
24	FPGA	B15	D8	-	IO_15_L1_P	AD0P											
25	FPGA	B15	A14	-	IO_15_L8_N	AD10N											

Pin	Type	Volt	fpga ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
26	GND	-	-	-	GND												
27	FPGA	B15	A15	-	IO_15_L10_N	AD11N											
28	FPGA	B15	A12	-	IO_15_L7_N	AD2N											
29	FPGA	B15	B14	-	IO_15_L10_P	AD11P											
30	FPGA	B15	B12	-	IO_15_L7_P	AD2P											
31	GND	-	-	-	GND												
32	FPGA	B15	B15	-	IO_15_L9_N	AD3N											
33	FPGA	B15	C13	-	IO_15_L11_N		SRCC_N										
34	FPGA	B15	C14	-	IO_15_L9_P	AD3P											
35	FPGA	B15	D13	-	IO_15_L11_P		SRCC_P										
36	FPGA	B15	D14	-	IO_15_L12_N		MRCC_N										
37	FPGA	B15	C12	-	IO_15_L6_N												
38	FPGA	B15	E13	-	IO_15_L12_P		MRCC_P										
39	FPGA	B15	D11	-	IO_15_L6_P												
40	FPGA	B15	F14	-	IO_15_L22_N												
41	FPGA	B15	C9	-	IO_15_L2_N	AD8N											
42	FPGA	B15	G14	-	IO_15_L22_P												
43	FPGA	B15	D9	-	IO_15_L2_P	AD8P											
44	GND	-	-	-	GND												
45	FPGA	B15	D15	-	IO_15_L13_N		MRCC_N										
46	FPGA	B34	V8	-	IO_34_L24_P												
47	FPGA	B15	E15	-	IO_15_L13_P		MRCC_P										
48	FPGA	B34	V7	-	IO_34_L24_N												
49	GND	-	-	-	GND												
50	FPGA	B34	U7	-	IO_34_L23_P												
51	FPGA	B34	R3	-	IO_34_L14_P		SRCC_P										

Pin	Type	Volt	fpga ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
52	FPGA	B34	V6	-	IO_34_L23_N												
53	FPGA	B34	T2	-	IO_34_L14_N		SRCC_N										
54	FPGA	B34	M6	-	IO_34_L8_P												
55	FPGA	B34	R2	-	IO_34_L13_P		MRCC_P										
56	FPGA	B34	N6	-	IO_34_L8_N												
57	FPGA	B34	R1	-	IO_34_L13_N		MRCC_N										
58	FPGA	B34	P6	-	IO_34_L19_P												
59	FPGA	B34	J5	-	IO_34_L2_P												
60	FPGA	B34	P5	-	IO_34_L19_N												
61	FPGA	B34	J4	-	IO_34_L2_N												
62	GND	-	-	-	GND												
63	FPGA	B34	P1	-	IO_34_L9_N												
64	FPGA	B34	T7	-	IO_34_L22_N												
65	FPGA	B34	N1	-	IO_34_L9_P												
66	FPGA	B34	R7	-	IO_34_L22_P												
67	GND	-	-	-	GND												
68	FPGA	B34	T5	-	IO_34_L21_N												
69	FPGA	B34	K6	-	IO_34_L1_N												
70	FPGA	B34	R5	-	IO_34_L21_P												
71	FPGA	B34	K5	-	IO_34_L1_P												
72	FPGA	B34	U6	-	IO_34_L20_P												
73	FPGA	B34	L5	-	IO_34_L6_P												
74	FPGA	B34	U5	-	IO_34_L20_N												
75	FPGA	B34	M5	-	IO_34_L6_N												
76	FPGA	B34	V4	-	IO_34_L18_N												
77	FPGA	B34	M4	-	IO_34_L10_P												

Pin	Type	Volt	fpga ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
78	FPGA	B34	U4	-	IO_34_L18_P												
79	FPGA	B34	N4	-	IO_34_L10_N												
80	GND	-	-	-	GND												
81	FPGA	B34	L4	-	IO_34_L5_P												
82	FPGA	B34	T4	-	IO_34_L17_P												
83	FPGA	B34	L3	-	IO_34_L5_N												
84	FPGA	B34	T3	-	IO_34_L17_N												
85	GND	-	-	-	GND												
86	FPGA	B34	N3	-	IO_34_L11_P		SRCC_P										
87	FPGA	B34	M2	-	IO_34_L7_P												
88	FPGA	B34	N2	-	IO_34_L11_N		SRCC_N										
89	FPGA	B34	M1	-	IO_34_L7_N												
90	FPGA	B34	V3	-	IO_34_L16_P												
91	FPGA	B34	P4	-	IO_34_L12_P		MRCC_P										
92	FPGA	B34	V2	-	IO_34_L16_N												
93	FPGA	B34	P3	-	IO_34_L12_N		MRCC_N										
94	FPGA	B34	U2	-	IO_34_L15_P												
95	FPGA	B34	K2	-	IO_34_L3_P												
96	FPGA	B34	U1	-	IO_34_L15_N												
97	FPGA	B34	K1	-	IO_34_L3_N												
98	GND	-	-	-	GND												
99	FPGA	B34	K3	-	IO_34_L4_P												
100	MFIO	1.8	-	U6	RGMII0_TXD0	RMII0_RXD0	MII0_RXD0	VIN2A_D10	SPI4_CS0	UART4_RTSN	PR1_MII0_RXD0	PR2_PRU1_GPI10	PR2_PRU1_GPO10	GPIO5_25			
101	FPGA	B34	L2	-	IO_34_L4_N												
102	MFIO	1.8	-	V6	RGMII0_TXD1	RMII0_RXD1	MII0_RXD1	VIN2A_VSYNC0	VIN4B_VSYNC1	SPI4_D0	UART4_CTSN	PR1_MII0_RXD1	PR2_PRU1_GPI9	PR2_PRU1_GPO9	GPIO5_24		
103	GND		-	-	GND												

Pin	Type	Volt	fpga ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
104	MFIO	1.8	-	U7	RGMII0_TXD2	RMII0_RXER	MII0_RXER	VIN2A_HSYNC0	VIN4B_HSYNC1	SPI4_D1	UART4_TXD	PR1_MII0_RXER	PR2_PRU1_GPI8	PR2_PRU1_GPO8	GPIO5_23		
105	MFIO	1.8	-	Y1	SPI3_D1	UART3_TXD	RMII1_RXER	MII0_RXCLK	VIN2A_D2	VIN4B_D2	SPI4_CS1	PR1_MII_MR0_CLK	PR2_PRU1_GPI4	PR2_PRU1_GPO4	GPIO5_19		
106	MFIO	1.8	-	V7	RGMII0_TXD3	RMII0_CRS	MII0_CRS	VIN2A_DE0	VIN4B_DE1	SPI4_SCLK	UART4_RXD	PR1_MII0_CRS	PR2_PRU1_GPI7	PR2_PRU1_GPO7	GPIO5_22		
107	MFIO	1.8	-	V2	SPI3_SCLK	UART3_RXD	RMII1_CRS	MII0_RXDV	VIN2A_D1	VIN4B_D1	PR1_MII0_RXDV	PR2_PRU1_GPI3	PR2_PRU1_GPO3	GPIO5_18			
108	MFIO	1.8	-	W9	RGMII0_TXC	UART3_CTSN	RMII1_RXD1	MII0_RXD3	VIN2A_D3	VIN4B_D3	SPI3_D0	SPI4_CS2	PR1_MII0_RXD3	PR2_PRU1_GPI5	PR2_PRU1_GPO5	GPIO5_20	
109	MFIO	3.3	-	Y9	MMC1_SDWP	UART6_TXD	I2C4_SCL	GPIO6_28									
110	MFIO	1.8	-	V9	RGMII0_TXCTL	UART3_RTSN	RMII1_RXD0	MII0_RXD2	VIN2A_D4	VIN4B_D4	SPI3_CS0	SPI4_CS3	PR1_MII0_RXD2	PR2_PRU1_GPI6	PR2_PRU1_GPO6	GPIO5_21	
111	MFIO	1.8	-	C14	PR2_MDIO_MDCLK	MCASP1_ACLKX	VIN6A_FLD0	I2C3_SDA	PR2_PRU1_GPI7	PR2_PRU1_GPO7	GPIO7_31						
112	GND	-	-	-	GND												
113	MFIO	1.8	-	D14	PR2_MDIO_DATA	MCASP1_FSX	VIN6A_DE0	I2C3_SCL	GPIO7_30								
114	MFIO	1.8	-	V4	RGMII0_RXD3	RMII1_TXD0	MII0_TXD2	VIN2A_D7	VIN4B_D7	PR1_MII0_TXD2	PR2_PRU1_GPI13	PR2_PRU1_GPO13	GPIO5_28				
115	MFIO	1.8	-	G16	UART4_RXD	MCASP4_AXR0	SPI3_D0	UART8_CTSN	VOUT2_D18	VIN4A_D18	VIN5A_D13						
116	MFIO	1.8	-	V3	RGMII0_RXD2	RMII0_TXEN	MII0_TXEN	VIN2A_D8	PR1_MII0_TXEN	PR2_PRU1_GPI14	PR2_PRU1_GPO14	GPIO5_29					
117	MFIO	1.8	-	E12	MCASP4_AXR2	MCASP1_AXR4	VOUT2_D4	VIN4A_D4	GPIO5_6								
118	MFIO	1.8	-	Y2	RGMII0_RXD1	RMII0_TXD1	MII0_TXD1	VIN2A_D9	PR1_MII0_TXD1	PR2_PRU1_GPI15	PR2_PRU1_GPO15	GPIO5_30					
119	MFIO	1.8	-	D17	MCASP4_AXR1	SPI3_CS0	UART8_RTSN	UART4_TXD	VOUT2_D19	VIN4A_D19	VIN5A_D12	PR2_PRU1_GPI0	PR2_PRU1_GPO0				
120	MFIO	1.8	-	W2	RGMII0_RXD0	RMII0_TXD0	MII0_TXD0	VIN2A_FLD0	VIN4B_FLD1	PR1_MII0_TXD0	PR2_PRU1_GPI16	PR2_PRU1_GPO16	GPIO5_31				
121	MFIO	1.8	-	C18	MCASP4_ACLKX	MCASP4_ACLKR	SPI3_SCLK	UART8_RXD	I2C4_SDA	VOUT2_D16	VIN4A_D16	VIN5A_D15					
122	MFIO	1.8	-	V5	RGMII0_RXCTL	RMII1_TXD1	MII0_TXD3	VIN2A_D6	VIN4B_D6	PR1_MII0_TXD3	PR2_PRU1_GPI12	PR2_PRU1_GPO12	GPIO5_27				
123	MFIO	1.8	-	A21	MCASP4_FSX	MCASP4_FSR	SPI3_D1	UART8_TXD	I2C4_SCL	VOUT2_D17	VIN4A_D17	VIN5A_D14					
124	MFIO	1.8	-	U5	RGMII0_RXC	RMII1_TXEN	MII0_TXCLK	VIN2A_D5	VIN4B_D5	PR1_MII_MT0_CLK	PR2_PRU1_GPI11	PR2_PRU1_GPO11	GPIO5_26				
125	FPGA	1.8	F12	-	FPGA_DONE												
126	KEY	-	-	-													
127	KEY	-	-	-													
128	KEY	-	-	-													
129	KEY	-	-	-													

Pin	Type	Volt	fpga ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
130	KEY	-	-	-													
131	KEY	-	-	-													
132	KEY	-	-	-													
133	GND	-	-	-	GND												
134	GND	-	-	-	GND												
135	MFIO	1.8	-	J7	MMC2_CLK	GPMC_A23	GPMC_A17	VIN4A_FLD0	VIN3B_D4	GPIO2_13							
136	MFIO	1.8	-	D6	RGMII1_TXD0	VIN2A_D17	VIN2B_D6	VOUT2_D6	VIN3A_D9	MII1_TXD2	EHRPWM3A	PR1_MII1_RXD2	PR1_PRU1_GPI14	PR1_PRU1_GPO14	GPIO4_25		
137	MFIO	1.8	-	H6	MMC2_CMD	GPMC_CS1	GPMC_A22	VIN4A_DE0	VIN3B_VSYNC1	GPIO2_18							
138	MFIO	1.8	-	B2	RGMII1_TXD1	VIN2A_D16	VIN2B_D7	VOUT2_D7	VIN3A_D8	MII1_TXD1	EQEP3_STROBE	PR1_MII1_RXD3	PR1_PRU1_GPI13	PR1_PRU1_GPO13	GPIO4_24		
139	MFIO	1.8	-	J4	MMC2_DAT0	GPMC_A24	GPMC_A18	VIN3B_D5	GPIO2_14								
140	MFIO	1.8	-	C4	RGMII1_TXD2	VIN2A_D15	VOUT2_D8	MII1_TXD0	EQEP3_INDEX	PR1_MII1_RXDV	PR1_PRU1_GPI12	PR1_PRU1_GPO12	GPIO4_16				
141	MFIO	1.8	-	J6	MMC2_DAT1	GPMC_A25	GPMC_A19	VIN3B_D6	GPIO2_15								
142	MFIO	1.8	-	C3	RGMII1_TXD3	VIN2A_D14	VOUT2_D9	MII1_TXCLK	EQEP3B_IN	PR1_MII_MR1_CLK	PR1_PRU1_GPI11	PR1_PRU1_GPO11	GPIO4_15				
143	MFIO	1.8	-	H4	MMC2_DAT2	GPMC_A26	GPMC_A20	VIN3B_D7	GPIO2_16								
144	MFIO	1.8	-	D5	RGMII1_TXC	VIN2A_D12	VOUT2_D11	MII1_RXCLK	KBD_COL8	ECAP2_IN_PWM2_OUT	PR1_MII1_TXD1	PR1_PRU1_GPI9	PR1_PRU1_GPO9	GPIO4_13			
145	MFIO	1.8	-	H5	MMC2_DAT3	GPMC_A27	GPMC_A21	VIN3B_HSYNC1	GPIO2_17								
146	MFIO	1.8	-	C2	RGMII1_TXCTL	VIN2A_D13	VOUT2_D10	MII1_RXDV	KBD_ROW8	EQEP3A_IN	PR1_MII1_TXD0	PR1_PRU1_GPI10	PR1_PRU1_GPO10	GPIO4_14			
147	MFIO	1.8	-	K7	GPMC_A19	MMC2_DAT4	GPMC_A13	VIN4A_D12	VIN3B_D0	GPIO2_9							
148	GND	-	-	-	GND												
149	MFIO	1.8	-	M7	GPMC_A20	MMC2_DAT5	GPMC_A14	VIN4A_D13	VIN3B_D1	GPIO2_10							
150	MFIO	1.8	-	B3	RGMII1_RXD3	VIN2A_D20	VIN2B_D3	VOUT2_D3	VIN3A_DE0	VIN3A_D12	MII1_RXER	ECAP3_IN_PWM3_OUT	PR1_MII1_RXER	PR1_PRU1_GPI17	PR1_PRU1_GPO17	GPIO4_28	
151	MFIO	1.8	-	J5	GPMC_A21	MMC2_DAT6	GPMC_A15	VIN4A_D14	VIN3B_D2	GPIO2_11							
152	MFIO	1.8	-	B4	RGMII1_RXD2	VIN2A_D21	VIN2B_D2	VOUT2_D2	VIN3A_FLD0	VIN3A_D13	MII1_COL	PR1_MII1_RXLINK	PR1_PRU1_GPI18	PR1_PRU1_GPO18	GPIO4_29		
153	MFIO	1.8	-	K6	GPMC_A22	MMC2_DAT7	GPMC_A16	VIN4A_D15	VIN3B_D3	GPIO2_12							
154	MFIO	1.8	-	B5	RGMII1_RXD1	VIN2A_D22	VIN2B_D1	VOUT2_D1	VIN3A_HSYNC0	VIN3A_D14	MII1_CRS	PR1_MII1_COL	PR1_PRU1_GPI19	PR1_PRU1_GPO19	GPIO4_30		
155	GND	-	-	-	GND												

Pin	Type	Volt	fpga ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
156	MFIO	1.8	-	A4	RGMII1_RXD0	VIN2A_D23	VIN2B_D0	VOUT2_D0	VIN3A_VSYNC0	VIN3A_D15	MII1_TXEN	PR1_MII1_CRS	PR1_PRU1_GPI20	PR1_PRU1_GPO20	GPIO4_31		
157	MFIO	1.8	-	U3	GPIO5_17	RMII_MHZ_50_CLK	VIN2A_D11	PR2_PRU1_GPI2	PR2_PRU1_GPO2								
158	MFIO	1.8	-	A3	RGMII1_RXCTL	VIN2A_D19	VIN2B_D4	VOUT2_D4	VIN3A_D11	MII1_TXER	EHRPWM3_TRIPZ_IN	PR1_MII1_RXD0	PR1_PRU1_GPI16	PR1_PRU1_GPO16	GPIO4_27		
159	MFIO	1.8	-	U4	MDIO_D	UART3_CTSN	MII0_TXER	VIN2A_D0	VIN4B_D0	PR1_MII0_RXLINK	PR2_PRU1_GPI1	PR2_PRU1_GPO1	GPIO5_16				
160	MFIO	1.8	-	C5	RGMII1_RXC	VIN2A_D18	VIN2B_D5	VOUT2_D5	VIN3A_D10	MII1_TXD3	EHRPWM3B	PR1_MII1_RXD1	PR1_PRU1_GPI15	PR1_PRU1_GPO15	GPIO4_26		
161	MFIO	1.8	-	V1	MDIO_MCLK	UART3_RTSN	MII0_COL	VIN2A_CLK0	VIN4B_CLK1	PR1_MII0_COL	PR2_PRU1_GPI0	PR2_PRU1_GPO0	GPIO5_15				
162	GND	-	-	-	GND												
163	MFIO	3.3	-	W7	MMC1_SDCD	UART6_RXD	I2C4_SDA	GPIO6_27									
164	MFIO	1.8	-	AC9	PR2_MII_MR1_CLK	MMC3_DAT2	SPI3_CS0	UART5_CTSN	VIN2B_D3	VIN5A_D3	EQEP3_INDEX	PR2_PRU0_GPI6	PR2_PRU0_GPO6	GPIO7_1			
165	MFIO	3.3	-	W6	MMC1_CLK	GPIO6_21											
166	MFIO	1.8	-	AC3	PR2_MII1_RXDV	MMC3_DAT3	SPI3_CS1	UART5_RTSN	VIN2B_D2	VIN5A_D2	EQEP3_STROBE	PR2_PRU0_GPI7	PR2_PRU0_GPO7	GPIO7_2			
167	MFIO	3.3	-	Y6	MMC1_CMD	GPIO6_22											
168	MFIO	1.8	-	E17	PR2_MII1_CRS	XREF_CLK1	MCASP2_AXR9	MCASP1_AXR5	MCASP2_AHCLKX	MCASP6_AHCLKX	VIN6A_CLK0	TIMER14	PR2_PRU1_GPI6	PR2_PRU1_GPO6	GPIO6_18		
169	MFIO	3.3	-	Y3	MMC1_DAT3	GPIO6_26											
170	MFIO	1.8	-	B19	PR2_MII1_RXER	MCASP3_AXR0	MCASP2_AXR14	UART7_CTSN	UART5_RXD	VIN6A_D1	PR2_PRU0_GPI14	PR2_PRU0_GPO14					
171	MFIO	3.3	-	AA5	MMC1_DAT2	GPIO6_25											
172	MFIO	1.8	-	D18	PR2_MII1_COL	XREF_CLK0	MCASP2_AXR8	MCASP1_AXR4	MCASP1_AHCLKX	MCASP5_AHCLKX	VIN6A_D0	HDQ0	CLKOUT2	TIMER13	PR2_PRU1_GPI5	PR2_PRU1_GPO5	GPIO6_17
173	MFIO	3.3	-	Y4	MMC1_DAT1	GPIO6_24											
174	MFIO	1.8	-	AB5	PR2_MII1_RXD0	MMC3_DAT7	SPI4_CS0	UART10_RTSN	VIN2B_CLK1	VIN5A_VSYNC0	ECAP3_IN_PWM3_OUT	PR2_PRU0_GPI11	PR2_PRU0_GPO11	GPIO1_25			
175	MFIO	3.3	-	AA6	MMC1_DAT0	GPIO6_23											
176	MFIO	1.8	-	AB8	PR2_MII1_RXD1	MMC3_DAT6	SPI4_D0	UART10_CTSN	VIN2B_DE1	VIN5A_HSYNC0	EHRPWM3_TRIPZ_IN	PR2_PRU0_GPI10	PR2_PRU0_GPO10	GPIO1_24			
177	GND	-	-	-	GND												
178	MFIO	1.8	-	AD6	PR2_MII1_RXD2	MMC3_DAT5	SPI4_D1	UART10_TXD	VIN2B_D0	VIN5A_D0	EHRPWM3B	PR2_PRU0_GPI9	PR2_PRU0_GPO9	GPIO1_23			
179	MFIO	1.8	-	P4	GPMC_A12	VIN4A_CLK0	GPMC_A0	VIN4B_FLD1	TIMER8	SPI4_CS1	DMA_EVT1	GPIO2_2					
180	MFIO	1.8	-	AC8	PR2_MII1_RXD3	MMC3_DAT4	SPI4_SCLK	UART10_RXD	VIN2B_D1	VIN5A_D1	EHRPWM3A	PR2_PRU0_GPI8	PR2_PRU0_GPO8	GPIO1_22			

Pin	Type	Volt	fpga ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
181	MFIO	1.8	-	N9	GPMC_A10	VIN3A_DE0	VOUT3_DE	VIN4B_CLK1	TIMER10	SPI4_D0	GPIO2_0						
182	MFIO	1.8	-	C17	PR2_MII1_RXLINK	MCASP3_AXR1	MCASP2_AXR15	UART7_RTSN	UART5_TXD	VIN6A_D0	VIN5A_FLD0	PR2_PRU0_GPI15	PR2_PRU0_GPO15				
183	MFIO	1.8	-	P9	GPMC_A11	VIN3A_FLD0	VOUT3_FLD	VIN4A_FLD0	VIN4B_DE1	TIMER9	SPI4_CS0	GPIO2_1					
184	MFIO	1.8	-	AC5	PR2_MII_MT1_CLK	GPIO6_10	MDIO_MCLK	I2C3_SDA	VIN2B_HSYNC1	VIN5A_CLK0	EHRPWM2A	PR2_PRU0_GPI0	PR2_PRU0_GPO0	GPIO6_10			
185	MFIO	1.8	-	P6	I2C5_SCL	GPMC_A4	QSPI1_CS3	VIN3A_D20	VOUT3_D20	VIN4A_D4	VIN4B_D4	UART6_RXD	GPIO1_26				
186	MFIO	1.8	-	AB4	PR2_MII1_TXEN	GPIO6_11	MDIO_D	I2C3_SCL	VIN2B_VSYNC1	VIN5A_DE0	EHRPWM2B	PR2_PRU0_GPI1	PR2_PRU0_GPO1	GPIO6_11			
187	MFIO	1.8	-	P5	GPMC_A7	VIN3A_D23	VOUT3_D23	VIN4A_D7	VIN4B_D7	UART8_TXD	UART6_RTSN	GPIO1_29					
188	MFIO	1.8	-	AC6	PR2_MII1_TXD0	MMC3_DAT1	SPI3_D0	UART5_TXD	VIN2B_D4	VIN5A_D4	EQEP3B_IN	PR2_PRU0_GPI5	PR2_PRU0_GPO5	GPIO7_0			
189	MFIO	1.8	-	G20	DCAN1_TX	UART8_RXD	MMC2_SDCD	HDMI1_HPD	GPIO1_14								
190	MFIO	1.8	-	AC7	PR2_MII1_TXD1	MMC3_DAT0	SPI3_D1	UART5_RXD	VIN2B_D5	VIN5A_D5	EQEP3A_IN	PR2_PRU0_GPI4	PR2_PRU0_GPO4	GPIO6_31			
191	MFIO	1.8	-	G19	DCAN1_RX	UART8_TXD	MMC2_SDWP	SATA1_LED	HDMI1_CEC	GPIO1_15							
192	MFIO	1.8	-	AC4	PR2_MII1_TXD2	MMC3_CMD	SPI3_SCLK	VIN2B_D6	VIN5A_D6	ECAP2_IN_PWM2_OUT	PR2_PRU0_GPI3	PR2_PRU0_GPO3	GPIO6_30				
193	MFIO	1.8	-	F20	UART10_TXD	GPIO6_15	MCASP1_AXR9	DCAN2_RX	VOUT2_VSYNC	VIN4A_VSYNC0	I2C3_SCL	TIMER2	GPIO6_15				
194	MFIO	1.8	-	AD4	PR2_MII1_TXD3	MMC3_CLK	VIN2B_D7	VIN5A_D7	EHRPWM2_TRIPZ_IN	PR2_PRU0_GPI2	PR2_PRU0_GPO2	GPIO6_29					
195	MFIO	1.8	-	G17	SPI2_D0	UART3_CTSN	UART5_RXD	GPIO7_16									
196	GND	-	-	-	GND												
197	MFIO	1.8	-	E15	MCASP2_ACLKR	MCASP8_AXR2	VOUT2_D8	VIN4A_D8									
198	MFIO	1.8	-	A13	PR2_MII_MR0_CLK	MCASP1_AXR13	MCASP7_AXR1	VIN6A_D10	TIMER10	PR2_PRU1_GPI15	PR2_PRU1_GPO15	GPIO6_4					
199	MFIO	1.8	-	F16	SPI1_D1	GPIO7_8											
200	MFIO	1.8	-	G14	PR2_MII0_RXDV	MCASP1_AXR14	MCASP7_ACLKX	MCASP7_ACLKR	VIN6A_D9	TIMER11	PR2_PRU1_GPI16	PR2_PRU1_GPO16	GPIO6_5				
201	MFIO	1.8	-	C26	UART1_TXD	MMC4_SDWP	GPIO7_23										
202	MFIO	1.8	-	B18	PR2_MII0_CRS	MCASP3_ACLKX	MCASP3_ACLKR	MCASP2_AXR12	UART7_RXD	VIN6A_D3	PR2_PRU0_GPI12	PR2_PRU0_GPO12	GPIO5_13				
203	MFIO	1.8	-	T6	GPMC_A2	VIN3A_D18	VOUT3_D18	VIN4A_D2	VIN4B_D2	UART7_RXD	UART5_CTSN	GPIO7_5					
204	MFIO	1.8	-	G12	PR2_MII0_RXER	MCASP1_AXR0	UART6_RXD	VIN6A_VSYNC0	I2C5_SDA	PR2_PRU1_GPI8	PR2_PRU1_GPO8	GPIO5_2					
205	MFIO	1.8	-	T7	GPMC_A3	QSPI1_CS2	VIN3A_D19	VOUT3_D19	VIN4A_D3	VIN4B_D3	UART7_TXD	UART5_RTSN	GPIO7_6				
206	MFIO	1.8	-	F15	PR2_MII0_COL	MCASP3_FSX	MCASP3_FSR	MCASP2_AXR13	UART7_TXD	VIN6A_D2	PR2_PRU0_GPI13	PR2_PRU0_GPO13	GPIO5_14				

Pin	Type	Volt	fpga ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
207	MFIO	1.8	-	R9	I2C5_SDA	GPMC_A5	VIN3A_D21	VOUT3_D21	VIN4A_D5	VIN4B_D5	UART6_TXD	GPIO1_27					
208	MFIO	1.8	-	C15	PR2_MII0_RXD0	MCASP2_AXR2	MCASP3_AXR2	VIN6A_D5	PR2_PRU0_GPI16	PR2_PRU0_GPO16	GPIO6_8						
209	MFIO	1.8	-	T9	I2C4_SDA	GPMC_A1	VIN3A_D17	VOUT3_D17	VIN4A_D1	VIN4B_D1	UART5_TXD	GPIO7_4					
210	MFIO	1.8	-	A18	PR2_MII0_RXD1	MCASP2_FSX	VIN6A_D6	PR2_PRU0_GPI19	PR2_PRU0_GPO19								
211	MFIO	1.8	-	G13	MCASP1_AXR2	MCASP6_AXR2	UART6_CTSN	VOUT2_D2	VIN4A_D2	GPIO5_4							
212	MFIO	1.8	-	A19	PR2_MII0_RXD2	MCASP2_ACLKX	VIN6A_D7	PR2_PRU0_GPI18	PR2_PRU0_GPO18								
213	MFIO	1.8	-	J11	MCASP1_AXR3	MCASP6_AXR3	UART6_RTSN	VOUT2_D3	VIN4A_D3	GPIO5_5							
214	MFIO	1.8	-	F14	PR2_MII0_RXD3	MCASP1_AXR15	MCASP7_FSX	MCASP7_FSR	VIN6A_D8	TIMER12	PR2_PRU0_GPI20	PR2_PRU0_GPO20	GPIO6_6				
215	MFIO	1.8	-	N7	GPMC_A8	VIN3A_HSYNC0	VOUT3_HSYNC	VIN4B_HSYNC1	TIMER12	SPI4_SCLK	GPIO1_30						
216	MFIO	1.8	-	A16	PR2_MII0_RXLINK	MCASP2_AXR3	MCASP3_AXR3	VIN6A_D4	PR2_PRU0_GPI17	PR2_PRU0_GPO17	GPIO6_9						
217	MFIO	1.8	-	R4	GPMC_A9	VIN3A_VSYNC0	VOUT3_VSYNC	VIN4B_VSYNC1	TIMER11	SPI4_D1	GPIO1_31						
218	MFIO	1.8	-	F12	PR2_MII_MT0_CLK	MCASP1_AXR1	UART6_TXD	VIN6A_HSYNC0	I2C5_SCL	PR2_PRU1_GPI9	PR2_PRU1_GPO9	GPIO5_3					
219	MFIO	1.8	-	R5	GPMC_A6	VIN3A_D22	VOUT3_D22	VIN4A_D6	VIN4B_D6	UART8_RXD	UART6_CTSN	GPIO1_28					
220	MFIO	1.8	-	B12	PR2_MII0_TXEN	MCASP1_AXR8	MCASP6_AXR0	SPI3_SCLK	VIN6A_D15	TIMER5	PR2_PRU1_GPI10	PR2_PRU1_GPO10	GPIO5_10				
221	MFIO	1.8	-	R6	I2C4_SCL	GPMC_A0	VIN3A_D16	VOUT3_D16	VIN4A_D0	VIN4B_D0	UART5_RXD	GPIO7_3					
222	MFIO	1.8	-	E14	PR2_MII0_TXD0	MCASP1_AXR12	MCASP7_AXR0	SPI3_CS1	VIN6A_D11	TIMER9	PR2_PRU1_GPI14	PR2_PRU1_GPO14	GPIO4_18				
223	MFIO	1.8	-	F21	GPIO6_16	MCASP1_AXR10	VOUT2_FLD	VIN4A_FLD0	CLKOUT1	TIMER3	GPIO6_16						
224	MFIO	1.8	-	A12	PR2_MII0_TXD1	MCASP1_AXR11	MCASP6_FSX	MCASP6_FSR	SPI3_CS0	VIN6A_D12	TIMER8	PR2_PRU1_GPI13	PR2_PRU1_GPO13	GPIO4_17			
225	GND	-	-	-	GND												
226	MFIO	1.8	-	B13	PR2_MII0_TXD2	MCASP1_AXR10	MCASP6_ACLKX	MCASP6_ACLKR	SPI3_D0	VIN6A_D13	TIMER7	PR2_PRU1_GPI12	PR2_PRU1_GPO12	GPIO5_12			
227	MFIO	1.8	-	E21	UART10_RXD	GPIO6_14	MCASP1_AXR8	DCAN2_TX	VOUT2_HSYNC	VIN4A_HSYNC0	I2C3_SDA	TIMER1	GPIO6_14				
228	MFIO	1.8	-	A11	PR2_MII0_TXD3	MCASP1_AXR9	MCASP6_AXR1	SPI3_D1	VIN6A_D14	TIMER6	PR2_PRU1_GPI11	PR2_PRU1_GPO11	GPIO5_11				
229	MFIO	1.8	-	B22	SPI2_D1	UART3_TXD	GPIO7_15										
230	GND	-	-	-	GND												
231	MFIO	1.8	-	D28	UART2_RXD	UART3_CTSN	UART3_RCTX	MMC4_DAT0	UART1_DCDN	GPIO7_26							
232	MFIO	1.8	-	AC10	USB2_DRVVBUS	TIMER15	GPIO6_13										

Pin	Type	Volt	fpga ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
233	MFIO	1.8	-	D26	UART2_TXD	UART3_RTSN	UART3_SD	MMC4_DAT1	UART1_DSRN	GPIO7_27							
234	MFIO	1.8	-	E25	GPIO7_24	UART1_CTSN	UART9_RXD	MMC4_CLK									
235	MFIO	1.8	-	G2	VIN2A_DE0	VIN2A_FLD0	VIN2B_FLD1	VIN2B_DE1	VOUT2_DE	EMU6	KBD_ROW1	EQEP1B_IN	PR1_EDIO_DATA_IN1	PR1_EDIO_DATA_OUT1	GPIO3_29		
236	MFIO	1.8	-	AE11	USB2_DP												
237	MFIO	1.8	-	G1	GPIO3_31	VIN2A_HSYNC0	VIN2B_HSYNC1	VOUT2_HSYNC	EMU8	UART9_RXD	SPI4_SCLK	KBD_ROW2	EQEP1_STROBE	PR1_UART0_CTS_N	PR1_EDIO_D_IN3	PR1_EDIO_D_OUT3	
238	MFIO	1.8	-	AF11	USB2_DM												
239	MFIO	1.8	-	F3	VIN2A_D1	VOUT2_D22	EMU11	UART9_RTSN	SPI4_CS0	KBD_ROW5	EHRPWM1_TRIPZ_IN	PR1_UART0_TXD	PR1_EDIO_DATA_IN6	PR1_EDIO_DATA_OUT6	GPIO4_2		
240	PWR	+5V	-	-	USB2_VBUS												
241	MFIO	1.8	-	F2	VIN2A_D0	VOUT2_D23	EMU10	UART9_CTSN	SPI4_D0	KBD_ROW4	EHRPWM1B	PR1_UART0_RXD	PR1_EDIO_DATA_IN5	PR1_EDIO_DATA_OUT5	GPIO4_1		
242	GND	-	-	-	GND												
243	MFIO	1.8	-	E1	VIN2A_CLK0	VOUT2_FLD	EMU5	KBD_ROW0	EQEP1A_IN	PR1_EDIO_DATA_IN0	PR1_EDIO_DATA_OUT0	GPIO3_28					
244	MFIO	1.8	-	J14	GPIO5_1	MCASP1_FSR	MCASP7_AXR3	VOUT2_D1	VIN4A_D1	I2C4_SCL							
245	MFIO	1.8	-	E2	VIN2A_D3	VOUT2_D20	EMU13	UART10_TXD	KBD_COL0	EHRPWM1_SYNCI	PR1_EDC_LATCH0_IN	PR1_PRU1_GPI0	PR1_PRU1_GPO0	GPIO4_4			
246	MFIO	1.8	-	F13	GPIO5_7	MCASP1_AXR5	MCASP4_AXR3	VOUT2_D5	VIN4A_D5								
247	MFIO	1.8	-	D1	VIN2A_D2	VOUT2_D21	EMU12	UART10_RXD	KBD_ROW6	ECAP1_IN_PWM1_OUT	PR1_ECAP0ECAP_CAPIN_APWM_O	PR1_EDIO_DATA_IN7	PR1_EDIO_DATA_OUT7	GPIO4_3			
248	MFIO	1.8	-	C12	GPIO5_8	MCASP1_AXR6	MCASP5_AXR2	VOUT2_D6	VIN4A_D6								
249	MFIO	1.8	-	D2	UART10_CTSN	VIN2A_D4	VOUT2_D19	EMU14	KBD_COL1	EHRPWM1_SYNCO	PR1_EDC_SYNC0_OUT	PR1_PRU1_GPI1	PR1_PRU1_GPO1	GPIO4_5			
250	MFIO	1.8	-	H7	GPIO3_30	VIN2A_FLD0	VIN2B_CLK1	VOUT2_CLK	EMU7	EQEP1_INDEX	PR1_EDIO_DATA_IN2	PR1_EDIO_DATA_OUT2					
251	MFIO	1.8	-	C1	VIN2A_D6	VOUT2_D17	EMU16	MII1_RXD1	KBD_COL3	EQEP2B_IN	PR1_MII_MT1_CLK	PR1_PRU1_GPI3	PR1_PRU1_GPO3	GPIO4_7			
252	MFIO	1.8	-	B14	GPIO5_0	MCASP1_ACLKR	MCASP7_AXR2	VOUT2_D0	VIN4A_D0	I2C4_SDA							
253	MFIO	1.8	-	D3	VIN2A_D10	MDIO_MCLK	VOUT2_D13	KBD_COL7	EHRPWM2B	PR1_MDIO_MDCLK	PR1_PRU1_GPI7	PR1_PRU1_GPO7	GPIO4_11				
254	MFIO	1.8	-	A15	MCASP2_AXR1	VOUT2_D11	VIN4A_D11										
255	MFIO	1.8	-	E4	VIN2A_D7	VOUT2_D16	EMU17	MII1_RXD2	KBD_COL4	EQEP2_INDEX	PR1_MII1_TXEN	PR1_PRU1_GPI4	PR1_PRU1_GPO4	GPIO4_8			
256	MFIO	1.8	-	B15	MCASP2_AXR0	VOUT2_D10	VIN4A_D10										
257	MFIO	1.8	-	F4	UART10_RTSN	VIN2A_D5	VOUT2_D18	EMU15	KBD_COL2	EQEP2A_IN	PR1_EDIO_SOF	PR1_PRU1_GPI2	PR1_PRU1_GPO2	GPIO4_6			

Pin	Type	Volt	fpga ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
258	MFIO	1.8	-	D15	MCASP8_AXR0	MCASP2_AXR4	VOUT2_D12	VIN4A_D12	GPIO1_4								
259	MFIO	1.8	-	F5	VIN2A_D8	VOUT2_D15	EMU18	MII1_RXD3	KBD_COL5	EQEP2_STROBE	PR1_MII1_TXD3	PR1_PRU1_GPI5	PR1_PRU1_GPO5	GPIO4_9			
260	MFIO	1.8	-	C23	MCASP8_AHCLKX	XREF_CLK3	MCASP2_AXR11	MCASP1_AXR7	MCASP4_AHCLKX	VOUT2_DE	HDQ0	VIN4A_DE0	CLKOUT3	TIMER16	GPIO6_20		
261	MFIO	1.8	-	E6	VIN2A_D9	VOUT2_D14	EMU19	MII1_RXD0	KBD_COL6	EHRPWM2A	PR1_MII1_TXD2	PR1_PRU1_GPI6	PR1_PRU1_GPO6	GPIO4_10			
262	MFIO	1.8	-	B16	MCASP8_AXR1	MCASP2_AXR5	VOUT2_D13	VIN4A_D13	GPIO6_7								
263	MFIO	1.8	-	F6	VIN2A_D11	MDIO_D	VOUT2_D12	KBD_ROW7	EHRPWM2_TRIPZONE_INPUT	PR1_MDIO_DATA	PR1_PRU1_GPI8	PR1_PRU1_GPO8	GPIO4_12				
264	MFIO	1.8	-	A17	MCASP8_FSX	MCASP2_AXR7	MCASP8_FSR	VOUT2_D15	VIN4A_D15	GPIO1_5							
265	MFIO	1.8	-	G6	VIN2A_VSYNC0	VIN2B_VSYNC1	VOUT2_VSYNC	EMU9	UART9_TXD	SPI4_D1	KBD_ROW3	EHRPWM1A	PR1_UART0_RTS_N	PR1_EDIO_DATA_IN4	PR1_EDIO_DATA_OUT4	GPIO4_0	
266	MFIO	1.8	-	B17	MCASP8_ACLKX	MCASP2_AXR6	MCASP8_ACLKR	VOUT2_D14	VIN4A_D14	GPIO2_29							
267	MFIO	1.8	-	B10	VOUT1_DE	VIN4A_DE0	VIN3A_DE0	SPI3_D1	GPIO4_20								
268	MFIO	1.8	-	A20	MCASP2_FSR	MCASP8_AXR3	VOUT2_D9	VIN4A_D9									
269	MFIO	1.8	-	D11	VOUT1_CLK	VIN4A_FLD0	VIN3A_FLD0	SPI3_CS0	GPIO4_19								
270	MFIO	1.8	-	B24	SPI2_CS0	UART3_RTSN	UART5_TXD	GPIO7_17									
271	MFIO	1.8	-	E11	VOUT1_VSYNC	VIN4A_VSYNC0	VIN3A_VSYNC0	SPI3_SCLK	PR2_PRU1_GPI17	PR2_PRU1_GPO17	GPIO4_23						
272	MFIO	1.8	-	A25	SPI1_SCLK	GPIO7_7											
273	MFIO	1.8	-	D12	MCASP1_AXR7	MCASP5_AXR3	VOUT2_D7	VIN4A_D7	TIMER4	GPIO5_9							
274	MFIO	1.8	-	B25	SPI1_D0	GPIO7_9											
275	MFIO	1.8	-	B27	UART1_RXD	MMC4_SDCD	GPIO7_22										
276	MFIO	1.8	-	A26	SPI2_SCLK	UART3_RXD	GPIO7_14										
277	GND	-	-	-	GND												
278	MFIO	1.8	-	B26	XREF_CLK2	MCASP2_AXR10	MCASP1_AXR6	MCASP3_AHCLKX	MCASP7_AHCLKX	VOUT2_CLK	VIN4A_CLK0	TIMER15	GPIO6_19				
279	MFIO	1.8	-	D27	UART3_RXD	UART2_CTSN	MMC4_DAT2	UART10_RXD	UART1_DTRN	GPIO1_16							
280	GND	-	-	-	GND												
281	MFIO	1.8	-	C28	UART3_TXD	UART2_RTSN	UART3_IRTX	MMC4_DAT3	UART10_TXD	UART1_RIN	GPIO1_17						
E1-1	PWR	5.0	-	-	VDD_5V0												

Pin	Type	Volt	fpga ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
E1-2	PWR	5.0	-	-	VDD_5V0												
E1-3	PWR	5.0	-	-	VDD_5V0												
E1-4	PWR	5.0	-	-	VDD_5V0												
E1-5	GND	-	-	-	GND												
E1-6	GND	-	-	-	GND												
E1-7	GND	-	-	-	GND												
E1-8	PWR	B34	-	-	VCCIO_34_EXT												
E1-9	PWR	B34	-	-	VCCIO_34_EXT												
E1-10	NC	-	-	-													
E2-1	PWR	5.0	-	-	VDD_5V0												
E2-2	PWR	5.0	-	-	VDD_5V0												
E2-3	PWR	5.0	-	-	VDD_5V0												
E2-4	PWR	5.0	-	-	VDD_5V0												
E2-5	GND	-	-	-	GND												
E2-6	GND	-	-	-	GND												
E2-7	PWR	B15	-	-	VCCO_15_EXT												
E2-8	PWR	B15	-	-	VCCO_15_EXT												
E2-9	OUT	1.8	-	-	VDD_1V8F												
E2-10	NC	-	-	-													
E3-1	NC	-	-	-													
E3-2	OUT	3.3	-	-	PS_3V3												
E3-3	OUT	3.3	-	-	PS_3V3												
E3-4	PMIO	-	-	-	AUXFAN_EN												
E3-5	FF	3.3	-	-	PB_RESETn												
E3-6	PMIO	-	-	-	PMIC_POWERGOOD												
E3-7	PMIO	-	-	-	PMIC_POWERHOLD												

Pin	Type	Volt	fpga ball	57xx ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10	Signal Option 11	Signal Option 12	Signal Option 13
E3-8	GND	-	-	-	GND												
E3-9	FPGA	B15	A17	-	IO_15_L15_N												
E3-10	FPGA	B15	B16	-	IO_15_L15_P												
E4-1	NC	-	-	-													
E4-2	OUT	-	-	-	VDD_1V8F												
E4-3	OUT	-	-	-	VDD_1V8F												
E4-4	MFIO	1.8	-	-	WAKEUP1	DCAN2_RX	GPIO1_1										
E4-5	GND	-	-	-	GND												
E4-6	FPGA	B15	A9	-	IO_15_L3_N	AD1N											
E4-7	FPGA	B15	B9	-	IO_15_L3_P	AD1P											
E4-8	FPGA	B15	A10	-	IO_15_L5_N	AD9P											
E4-9	FPGA	B15	B10	-	IO_15_L5_P	AD9N											
E4-10	FPGA	B15	C17	-	IO_15_L18_P												

Hirose 100 Pin Interface Description (J3)

The second interface connector for the MitySOM-AM57F is a Hirose DF40C-100DP-0.4V(51) 100 pin board-to-board interface which contains 6 types of signals:

- Power input and ground/return (PWR / GND)
- Pins mapped to the Xilinx Artix-7 Device (FPGA)
- Transceiver pins mapped to the Xilinx Artix-7 Device (XCVR)
- Multi-function signals mapped to the AM57XX device (MFIO)
- Module fixed-function pins (FF)
- Dedicated signals mapped to the Power Management IC (PMIC)

Table 7 contains a summary of the MitySOM-AM57F 100 Pin Hirose connector pin mapping which includes:

- Connector pin assignment
- Voltage domains
- FPGA or AM57XX ball for direct connect pins
- Signal Options / name for each pin

Table 7 J3 Pin-Out

Pin	Type	V	FPGA Ball	AM5728 Ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10
1	GND	-	-	-	GND									
2	GND	-	-	-	GND									
3	FF	-	-	AH19	HDMI1_DATA2Y									
4	MFIO	1.8	-	B21	HDMI1_HPD	SPI1_CS2	UART4_RXD	MMC3_SDCD	SPI2_CS2	DCAN2_TX	MDIO_MCLK	GPIO7_12		
5	FF	-	-	AG19	HDMI1_DATA2X									
6	MFIO	1.8	-	B20	HDMI1_CEC	SPI1_CS3	UART4_TXD	MMC3_SDWP	SPI2_CS3	DCAN2_RX	MDIO_D	GPIO7_13		
7	GND	-	-	-	GND									
8	MFIO	1.8	-	C25	HDMI1_DDC_SCL	I2C2_SDA								
9	FF	-	-	AH18	HDMI1_DATA1Y									
10	MFIO	1.8	-	F17	HDMI1_DDC_SDA	I2C2_SCL								
11	FF	-	-	AG18	HDMI1_DATA1X									
12	MFIO	1.8	-	A24	SPI1_CS0	GPIO7_10								
13	GND	-	-	-	GND									
14	MFIO	1.8	-	AG8	VIN1A_CLK0	VOUT3_D16	VOUT3_FLD	GPIO2_30						
15	FF	-	-	AH17	HDMI1_DATA0Y									
16	GND	-	-	-	GND									
17	FF	-	-	AG17	HDMI1_DATA0X									
18	MFIO	1.8	-	AA3	MCASP5_ACLKX	MCASP5_ACLKR	SPI4_SCLK	UART9_RXD	I2C5_SDA	VOUT2_D20	VIN4A_D20	VIN5A_D11	PR2_PRU1_GPI1	PR2_PRU1_GPO1
19	GND	-	-	-	GND									
20	MFIO	1.8	-	AB9	MCASP5_FSX	MCASP5_FSR	SPI4_D1	UART9_TXD	I2C5_SCL	VOUT2_D21	VIN4A_D21	VIN5A_D10	PR2_PRU1_GPI2	PR2_PRU1_GPO2
21	FF	-	-	AH16	HDMI1_CLOCKY									
22	MFIO	1.8	-	AD9	GPIO3_0	VIN1A_DE0	VIN1B_HSYNC1	VOUT3_D17	VOUT3_DE	UART7_RXD	TIMER16	SPI3_SCLK	KBD_ROW0	EQEP1A_IN
23	FF	-	-	AG16	HDMI1_CLOCKX									
24	MFIO	1.8	-	AD8	GPIO3_5	VIN1A_D1	VOUT3_D6	VOUT3_D22	UART8_TXD	EHRPWM1B				
25	GND	-	-	-	GND									

Pin	Type	V	FPGA Ball	AM5728 Ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10
26	MFIO	1.8	-	AF8	GPIO3_3	VIN1A_VSYNC0	VIN1B_DE1	VOUT3_VSYNC	UART7_RTSN	TIMER13	SPI3_CS0	EQEP1_STROBE		
27	FF	-	-	AC11	USB1_SSRX_N									
28	MFIO	1.8	-	AE8	GPIO3_4	VIN1A_D0	VOUT3_D7	VOUT3_D23	UART8_RXD	EHRPWM1A				
29	FF	-	-	AD11	USB1_SSRX_P									
30	MFIO	1.8	-	AF6	VIN1A_D13	VIN1B_D2	VOUT3_D10	GPMC_A25	KBD_ROW7	PR1_EDC_SYNC1_OUT	PR1_PRU0_GPI10	PR1_PRU0_GPO10	GPIO3_17	
31	GND	-	-	-	GND									
32	MFIO	1.8	-	AE6	VIN1A_D21	VIN1B_D2	VOUT3_D2	VIN3A_D5	KBD_COL6	PR1_EDIO_DATA_IN5	PR1_EDIO_DATA_OUT5	PR1_PRU0_GPI18	PR1_PRU0_GPO18	GPIO3_25
33	FF	-	-	AF12	USB1_SSTX_N									
34	MFIO	1.8	-	AA4	MCASP5_AXR1	SPI4_CS0	UART9_RTSN	UART3_TXD	VOUT2_D23	VIN4A_D23	VIN5A_D8	PR2_MDIO_DATA	PR2_PRU1_GPI4	PR2_PRU1_GPO4
35	FF	-	-	AE12	USB1_SSTX_P									
36	MFIO	1.8	-	AB3	MCASP5_AXR0	SPI4_D0	UART9_CTSN	UART3_RXD	VOUT2_D22	VIN4A_D22	VIN5A_D9	PR2_MDIO_MDCLK	PR2_PRU1_GPI3	PR2_PRU1_GPO3
37	GND	-	-	-	GND									
38	MFIO	1.8	-	AE9	GPIO3_2	VIN1A_HSYNC0	VIN1B_FLD1	VOUT3_HSYNC	UART7_CTSN	TIMER14	SPI3_D0	EQEP1_INDEX		
39	MFIO	1.8	-	C27	GPIO7_25	UART1_RTSN	UART9_TXD	MMC4_CMD						
40	MFIO	1.8	-	AF9	GPIO3_1	VIN1A_FLD0	VIN1B_VSYNC1	VOUT3_CLK	UART7_TXD	TIMER15	SPI3_D1	KBD_ROW1	EQEP1B_IN	
41	MFIO	1.8	-	AB10	USB1_DRVVBUS	TIMER16	GPIO6_12							
42	MFIO	1.8	-	AG7	GPIO3_6	VIN1A_D2	VOUT3_D5	VOUT3_D21	UART8_CTSN	EHRPWM1_TRIPZONE_INPUT				
43	FF	-	-	AC12	USB1_DM									
44	MFIO	1.8	-	AH7	VIN1B_CLK1	VIN3A_CLK0	GPIO2_31							
45	FF	-	-	AD12	USB1_DP									
46	MFIO	1.8	-	AG6	VIN1A_D6	VOUT3_D1	VOUT3_D17	EQEP2A_IN	PR1_PRU0_GPI3	PR1_PRU0_GPO3	GPIO3_10			
47	GND	-	-	-	GND									
48	MFIO	1.8	-	AH6	VIN1A_D3	VOUT3_D4	VOUT3_D20	UART8_RTSN	ECAP1_IN_PWM1_OUT	PR1_PRU0_GPI0	PR1_PRU0_GPO0	GPIO3_7		
49	FF	-	-	AH10	SATA1_TXP0									
50	MFIO	1.8	-	AG5	VIN1A_D11	VIN1B_D4	VOUT3_D12	GPMC_A23	KBD_ROW5	PR1_EDC_LATCH1_IN	PR1_PRU0_GPI8	PR1_PRU0_GPO8	GPIO3_15	
51	FF	-	-	AG10	SATA1_TXN0									

Pin	Type	V	FPGA Ball	AM5728 Ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10
52	MFIO	1.8	-	AH5	VIN1A_D5	VOUT3_D2	VOUT3_D18	EHRPWM1_SYNCO	PR1_PRU0_GPI2	PR1_PRU0_GPO2	GPIO3_9			
53	GND	-	-	-	GND									
54	MFIO	1.8	-	AG4	VIN1A_D8	VIN1B_D7	VOUT3_D15	KBD_ROW2	EQEP2_INDEX	PR1_PRU0_GPI5	PR1_PRU0_GPO5	GPIO3_12		
55	FF	-	-	AH9	SATA1_RXN0									
56	MFIO	1.8	-	AH4	VIN1A_D7	VOUT3_D0	VOUT3_D16	EQEP2B_IN	PR1_PRU0_GPI4	PR1_PRU0_GPO4	GPIO3_11			
57	FF	-	-	AG9	SATA1_RXP0									
58	MFIO	1.8	-	AG3	VIN1A_D10	VIN1B_D5	VOUT3_D13	KBD_ROW4	PR1_EDC_LATCH 0_IN	PR1_PRU0_GPI7	PR1_PRU0_GPO7	GPIO3_14		
59	GND	-	-	-	GND									
60	MFIO	1.8	-	AH3	VIN1A_D4	VOUT3_D3	VOUT3_D19	EHRPWM1_SYNCI	PR1_PRU0_GPI1	PR1_PRU0_GPO1	GPIO3_8			
61	MFIO	1.8	-	AE3	VIN1A_D17	VIN1B_D6	VOUT3_D6	VIN3A_D1	KBD_COL2	PR1_EDIO_DATA_IN1	PR1_EDIO_DATA_ OUT1	PR1_PRU0_G PI14	PR1_PRU0_G PO14	GPIO3_21
62	MFIO	1.8	-	AG2	VIN1A_D9	VIN1B_D6	VOUT3_D14	KBD_ROW3	EQEP2_STROBE	PR1_PRU0_GPI6	PR1_PRU0_GPO6	GPIO3_13		
63	MFIO	1.8	-	AF4	VIN1A_D15	VIN1B_D0	VOUT3_D8	GPMC_A27	KBD_COL0	PR1_EDIO_SOF	PR1_PRU0_GPI12	PR1_PRU0_G PO12	GPIO3_19	
64	MFIO	1.8	-	AF2	VIN1A_D12	VIN1B_D3	VOUT3_D11	GPMC_A24	KBD_ROW6	PR1_EDC_SYNC0_OUT	PR1_PRU0_GPI9	PR1_PRU0_G PO9	GPIO3_16	
65	MFIO	1.8	-	AE5	VIN1A_D18	VIN1B_D5	VOUT3_D5	VIN3A_D2	KBD_COL3	PR1_EDIO_DATA_IN2	PR1_EDIO_DATA_ OUT2	PR1_PRU0_G PI15	PR1_PRU0_G PO15	GPIO3_22
66	MFIO	1.8	-	AF1	VIN1A_D16	VIN1B_D7	VOUT3_D7	VIN3A_D0	KBD_COL1	PR1_EDIO_DATA_IN0	PR1_EDIO_DATA_ OUT0	PR1_PRU0_G PI13	PR1_PRU0_G PO13	GPIO3_20
67	MFIO	1.8	-	AD3	VIN1A_D23	VIN1B_D0	VOUT3_D0	VIN3A_D7	KBD_COL8	PR1_EDIO_DATA_IN7	PR1_EDIO_DATA_ OUT7	PR1_PRU0_G PI20	PR1_PRU0_G PO20	GPIO3_27
68	MFIO	1.8	-	AF3	VIN1A_D14	VIN1B_D1	VOUT3_D9	GPMC_A26	KBD_ROW8	PR1_EDIO_LATCH_IN	PR1_PRU0_GPI11	PR1_PRU0_G PO11	GPIO3_18	
69	GND	-	-	-	GND									
70	MFIO	1.8	-	AE2	VIN1A_D20	VIN1B_D3	VOUT3_D3	VIN3A_D4	KBD_COL5	PR1_EDIO_DATA_IN4	PR1_EDIO_DATA_ OUT4	PR1_PRU0_G PI17	PR1_PRU0_G PO17	GPIO3_24
71	XCVR	-	D6	-	FPGA_GXB_REF_CLK_P									
72	MFIO	1.8	-	AD2	VIN1A_D22	VIN1B_D1	VOUT3_D1	VIN3A_D6	KBD_COL7	PR1_EDIO_DATA_IN6	PR1_EDIO_DATA_ OUT6	PR1_PRU0_G PI19	PR1_PRU0_G PO19	GPIO3_26
73	XCVR	-	D5	-	FPGA_GXB_REF_CLK_N									
74	FF	-	-	-	AM57_BOOT_MODE									
75	GND	-	-	-	GND									
76	PWR	-	-	K14	OTP_VPP[1]									
77	XCVR	-	C3	-	FPGA_GXB_TX0_N									

Pin	Type	V	FPGA Ball	AM5728 Ball	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9	Signal Option 10
78	GND	-	-	-	GND									
79	XCVR		C4	-	FPGA_GXB_TX0_P									
80	FF		-	AC1	RESERVED (NC)									
81	GND	-	-	-	GND									
82	FF		-	AC2	RESERVED (NC)									
83	XCVR		D1	-	FPGA_GXB_RX0_N									
84	FF		-	AB1	RESERVED (NC)									
85	XCVR		D2	-	FPGA_GXB_RX0_P									
86	FF		-	AB2	RESERVED (NC)									
87	GND	-	-	-	GND									
88	FF		-	AA1	RESERVED (NC)									
89	XCVR		G3	-	FPGA_GXB_TX1_N									
90	FF		-	AA2	RESERVED (NC)									
91	XCVR		G4	-	FPGA_GXB_TX1_P									
92	GND	-	-	-	GND									
93	GND	-	-	-	GND									
94	FF		M9	-	FPGA_DXN									
95	XCVR		B1	-	FPGA_GXB_RX1_N									
96	FF		M10	-	FPGA_DXP									
97	XCVR		B2	-	FPGA_GXB_RX1_P									
98	FF		L9	-	FPGA_VN_0									
99	GND	-	-	-	GND									
100	FF		K10	-	FPGA_VP_0									

Note1: The OTP_VPP signal, K14, should typically be left floating. Please contact your Critical Link representative for further questions about the usage of this pin.

DEBUG INTERFACE

Both the JTAG interface signals for the FPGA and the JTAG and emulator signals for the AM57xx processor have been brought out to a Hirose connector (DF9-31P-1V(32)), J2, which is intended for use with an available breakout adapter, Critical Link part number 80-000286. This adapter is not included with individual modules but is included with each Critical Link Development Kit that is ordered. Additional adapters are available through Critical Link distribution partners.

Debug Interface Connector Description (J2)

Table 8: MitySOM-AM57F Debug Hirose Connector (J2)

Pin	I/O	Signal	Pin	I/O	Signal
1	-	GND	2	O	AM57xx EMU1
3	-	GND	4	O	AM57xx EMU0
5	-	GND	6	I	AM57xx TCK
7	-	GND	8	O	AM57xx RTCK
9	-	GND	10	O	AM57xx TDO
11	-	GND	12	-	AM57xx VCC / 1.8V
13	-	GND	14	I	AM57xx TDI
15	-	GND	16	I	AM57xx TRST
17	-	GND	18	I	AM57xx TMS
19	-	GND	20	-	GND
21	-	GND	22	O	FPGA VREF / VCCAUX / 1.8V
23	-	GND	24	I	FPGA TMS
25	-	GND	26	I	FPGA TCK
27	-	GND	28	O	FPGA TDO
29	-	GND	30	I	FPGA TDI
31	-	GND			

This header, J2, can be removed for production units; please contact Critical Link at info@criticallink.com for details.

ELECTRICAL CHARACTERISTICS

Table 9: Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_5	Voltage supply, 5 volt input.		4.5	5	5.25	Volts
I_5	Quiescent Current draw, 5 volt input			TBS[1,2]	TBS[1,2]	mA
$I_{5\text{-}max}$	Max current draw, positive 5 volt input.			TBS[1,2]	TBS[1,2]	mA
F_{CPU}	CPU internal clock Frequency (PLL output)		1500	1500	1500	MHz
F_{EMIFA}	DDR3 bus frequency, each bank		-	533	-	MHz
$I_{o3.3}$	Max output current 3.3V output				1000	mA
$I_{o1.8}$	Max output current 1.8V output				1500	mA
	1. Power utilization of the MitySOM-AM57F is heavily dependent on end-user application. Major factors include: ARM CPU PLL configuration, DSP Utilization FPGA utilization, and external DDR3L RAM utilization. 2. For power utilization information please visit our Redmine Wiki pages on support.criticallink.com					

ORDERING INFORMATION

The following table lists the standard module configurations. For shipping status, availability, and lead time of these or other configurations please contact Critical Link at info@criticallink.com.

Table 10: Standard Model Numbers

Module P/N	CPU	FPGA	NOR	RAM Bank 1	RAM Bank 2	Component Temperature Rating
5728-PJ-4AA-RC	AM5728	7A15T	32MB	1 GB	1 GB	0ºC to 70º C
5748-PJ-4AA-RC	AM5748	7A15T	32MB	1 GB	1 GB	0ºC to 70º C
5748-PJ-4AA-RI	AM5748	7A15T	32MB	1 GB	1 GB	-40ºC to 85º C
5749-PJ-4AA-RC	AM5749	7A15T	32MB	1 GB	1 GB	0ºC to 70º C
5749-PJ-4AA-RI	AM5749	7A15T	32MB	1 GB	1 GB	-40ºC to 85º C
5749-PM-4AA-RC	AM5749	7A50T	32MB	1 GB	1 GB	0ºC to 70º C
5749-PM-4AA-RI	AM5749	7A50T	32MB	1 GB	1 GB	-40ºC to 85º C

MECHANICAL INTERFACE

The dimensions of the MitySOM-AM57F are 88.000mm (~3.46in) x 69.417mm (~2.73in) and features two mounting holes at the rear of the module where the 100-pin connector, J3, is.

The mechanical outline of the MitySOM-AM57F is illustrated in Figure 4, as shown below.

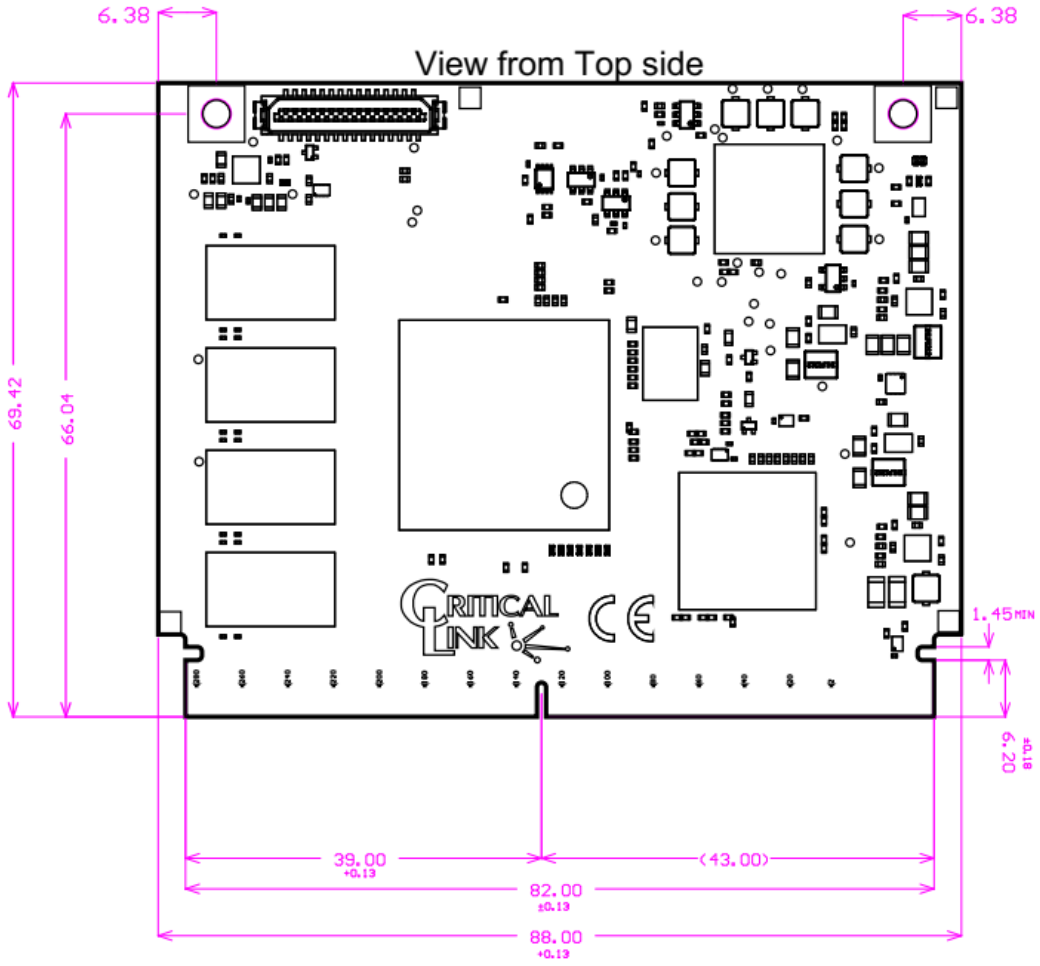

Figure 2 MitySOM-AM57F Dimensions

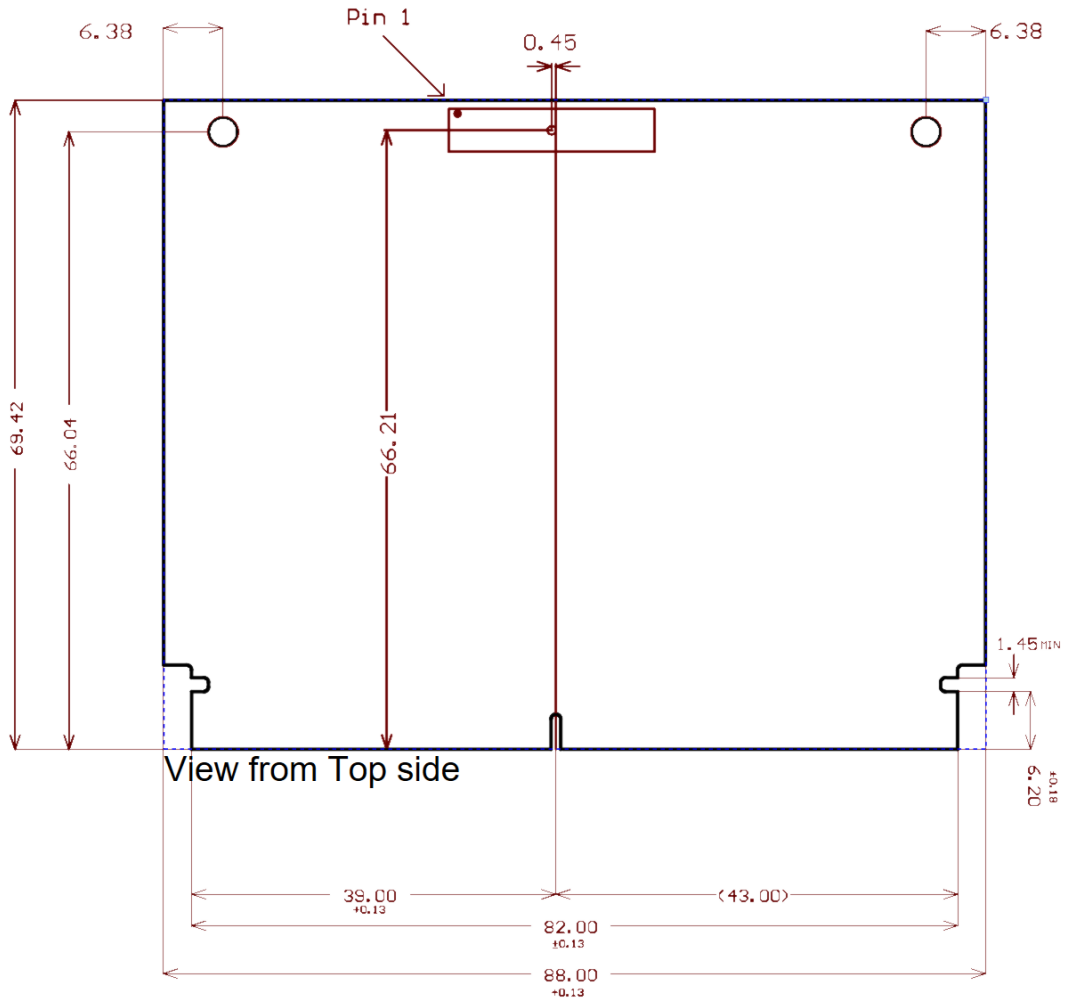

Figure 3 MitySOM-AM57F J3 Hirose 100 pin bottom side connector location

If a heat spreader/sink solution is required Critical Link recommends placing two additional mounting holes near the MXM connector as shown in Figure 4. In the figure, the dimensions are referenced from the left alignment pin position of the MXM connector, MM70-314-310B1-2-R300. The center of the mating connector for the 100 pin Hirose interface J3, DF40HC(3.0)-100DS-0.4V(58) is also shown.

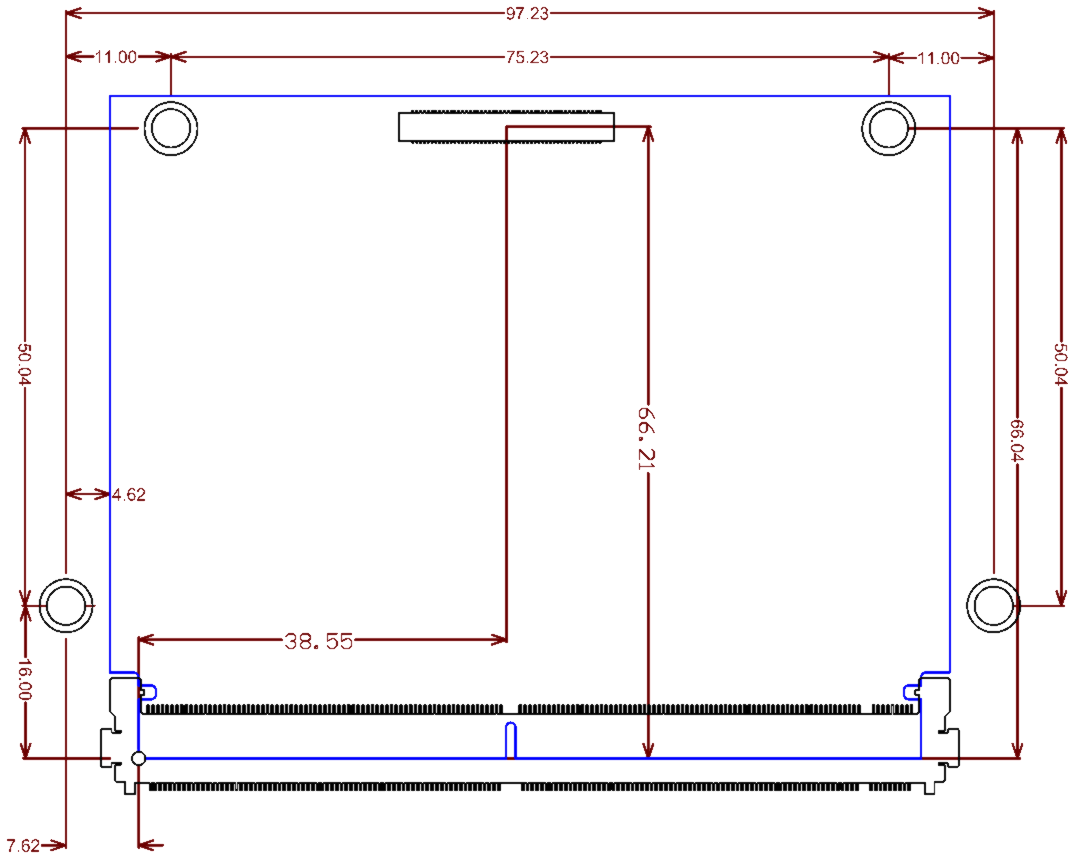

Figure 4 MitySOM-AM57F Carrier Card Outline with heat spreader mounting holes.

REVISION HISTORY

Rev	Date	Change Description
1A	17-JUN-2020	Initial Release
1B	7-AUG-2020	Update Fig 2, Update MMC1 pins voltage to 3.3V (table 6) and set FMC pins 80-90 as Reserved (NC) (table 7). Update AM57xx USB Interfaces section
1C	4-Nov-2020	Update Debug LEDs section to clarify usage. Update AM57xx Multifunction Input/Output (MFIO) Interfaces to clarify voltage domains. Update AM57xx USB Interfaces to clarify AC coupling. Swap USB SS TX/RX pinout Update Pin 125 (FPGA_DONE) Fix Pin 247 spelling (PR1_ECAP0ECAP_CAPIN_APWM_O) Fix Pin 19 text direction Changed PMIC to PMIO, “Dedicated signals mapped to the Power Management IC (PMIO)” Add missing mux options for Pin E4-4 (WAKEUP1) and update type to MFIO Update Max DDR size to 4GB
1D	14-Jan-2021	Green LED no longer shows cpu activity
1E	23-Sep-2021	Update IO pin counts
1F	2-Dec-2021	Updated Table 6 to correctly map N/P polarity of IO_34_L3_P/N, IO_34_L5_P/N, IO_34_L7_P/N, IO_34_L8_P/N, IO_34_L9_P/N, IO_34_L11_P/N, IO_34_L12_P/N, IO_34_L14_P/N, IO_34_L18_P/N,

		IO_34_L21_P/N Updated Table 6 to include MRCC and SRCC pin functions. Updated Table 6 to include ADXXN/P functions. Updated Figure 1 with more generic MXM connector recommendation
1G	9-Sep-2022	Update Mechanical section with additional figures.