



PowerPC 750CX RISC Microprocessor Datasheet

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IBM Microelectronics Division



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Table of Contents

| | |
|---|----|
| 1.0. Preface | 7 |
| 1.1. Special Design Level Considerations/Features | 7 |
| 2.0. Overview | 8 |
| 2.1. PowerPC 750CX RISC Microprocessor Block Diagram | 8 |
| 3.0. Features | 9 |
| 4.0. General Parameters | 11 |
| 5.0. Electrical and Thermal Characteristics | 11 |
| 5.1. DC Electrical Characteristics..... | 11 |
| 5.2. AC Electrical Characteristics..... | 14 |
| 5.2.1. Clock AC Specifications | 14 |
| 5.3. 60X Bus Input AC Specifications | 16 |
| 5.4. 60X Bus Output AC Specifications..... | 17 |
| 5.4.1. IEEE 1149.1 AC Timing Specifications | 19 |
| 6.0. PowerPC 750CX Microprocessor Dimension and Physical Signal Assignments | 22 |
| 7.0. System Design Information | 29 |
| 7.1. PLL Configuration..... | 29 |
| 7.2. PLL Power Supply Filtering..... | 31 |
| 7.3. Decoupling Recommendations..... | 31 |
| 7.4. Connection Recommendations | 31 |
| 7.5. Output Buffer DC Impedance..... | 32 |
| 7.5.1. Input-Output Usage | 33 |
| 7.6. Thermal Management Information..... | 36 |
| 7.7. Heat Sink Considerations | 36 |
| 7.8. Internal Package Conduction Resistance..... | 36 |
| 7.9. Operational and Design Considerations | 38 |
| 7.9.1. Level Protection | 38 |
| 7.9.2. 64 or 32-Bit Data Bus Mode | 38 |
| 7.9.3. 1.8V and 2.5V I/O Signal Support | 38 |
| 7.9.4. $\overline{DBW\bar{O}}$ /L2_TSTCLK | 39 |
| 7.9.5. PowerPC 750CX Revision Level Migration | 39 |
| 8.0. Ordering Information | 39 |
| 9.0. Processor Version Register (PVR) | 40 |
| 10.0. Document History | 41 |

List of Figures

| | |
|---|----|
| Figure 1. PowerPC 750CX RISC Microprocessor Block Diagram | 8 |
| Figure 2. SYSCLK Input Timing Diagram | 15 |
| Figure 3. Input Timing Diagram | 16 |
| Figure 4. Mode Select Input Timing Diagram | 17 |
| Figure 5. Output Valid Timing Definition | 18 |
| Figure 6. Output Timing Diagram for PowerPC 750CX RISC Microprocessor | 19 |
| Figure 7. JTAG Clock Input Timing Diagram | 20 |
| Figure 8. $\overline{\text{TRST}}$ Timing Diagram | 21 |
| Figure 9. Boundary-Scan Timing Diagram | 21 |
| Figure 10. Test Access Port Timing Diagram | 22 |
| Figure 11. Pinout of the 256 PBGA Package as Viewed from Solder Ball side | 23 |
| Figure 12. Side Profile View of PBGA | 24 |
| Figure 13. Side Profile View Showing Exposed Cavity | 24 |
| Figure 14. PowerPC 750CX Microprocessor Ball Placement | 25 |
| Figure 15. PLL Power Supply Filter Circuit | 31 |
| Figure 16. Driver Impedance Measurement | 32 |
| Figure 17. IBM RISCWatch™ JTAG to $\overline{\text{HRESET}}$, $\overline{\text{TRST}}$, and $\overline{\text{SRESET}}$ Signal Connector | 36 |
| Figure 18. PBGA Package with Thermal Model | 37 |
| Figure 19. IBM Part Number Key | 40 |

List of Tables

| | |
|---|----|
| Table 1: Absolute Maximum Ratings | 11 |
| Table 2: Recommended Operating Conditions ¹ | 12 |
| Table 3: Package Thermal Characteristics | 12 |
| Table 4: DC Electrical Specifications | 13 |
| Table 5: Power Consumption | 14 |
| Table 6: Clock AC Timing Specifications ^{1,6} | 15 |
| Table 7: 60X Bus Input Timing Specifications ^{1,6,8} | 16 |
| Table 8: 60X Bus Output AC Timing Specifications ^{1,4,6,7} | 17 |
| Table 9: JTAG AC Timing Specifications (Independent of SYSCLK) | 20 |
| Table 10: Signal Listing for the 256 PBGA Package | 26 |
| Table 11: Signals Removed from Previous PowerPC 750 Designs | 27 |
| Table 12: Signal Locations | 28 |
| Table 13: Voltage and Ground Assignments | 29 |
| Table 14: PowerPC 750CX Microprocessor PLL Configuration | 30 |
| Table 15: Driver Impedance Characteristics | 32 |
| Table 16: Input-Output Usage | 34 |
| Table 17: Summary of Design Migration | 39 |
| Table 18: Process Version Register (PVR) | 40 |
| Table 19: Document History | 41 |



1.0 Preface

The PowerPC 750CX RISC Microprocessor is an implementation of the PowerPC™ family of reduced instruction set computer (RISC) microprocessors. This document contains pertinent physical characteristics of the PowerPC 750CX RISC Microprocessor Single Chip Modules (SCM) and covers the following topics.

- Overview on page 8
- Features on page 9
- General Parameters on page 11
- Electrical and Thermal Characteristics on page 11
 - DC Electrical Characteristics on page 11
 - AC Electrical Characteristics on page 14
- PowerPC 750CX Microprocessor Dimension and Physical Signal Assignments on page 22
- System Design Information on page 29
- Ordering Information on page 39
- Processor Version Register (PVR) on page 40

1.1 Special Design Level Considerations/Features

The PowerPC 750CX supports several unique features including those listed below. Section 7.9 “Operational and Design Considerations,” on page 38 provides a more detailed explanation of these.

- Provides a 64 or 32-bit Data Bus mode (per setup of \overline{QACK} pin).
- Supports 1.8V and 2.5V I/O signals.
- Uses a reduced pin list from earlier PowerPC 750 designs (see Table 11, “Signals Removed from Previous PowerPC 750 Designs” on page 27).
- Data Bus Write Only (\overline{DBWO}) shares a common pin with L2_TESTCLK.
- $\overline{CKSTP_OUT}$ shares a common pin with CLK_OUT.

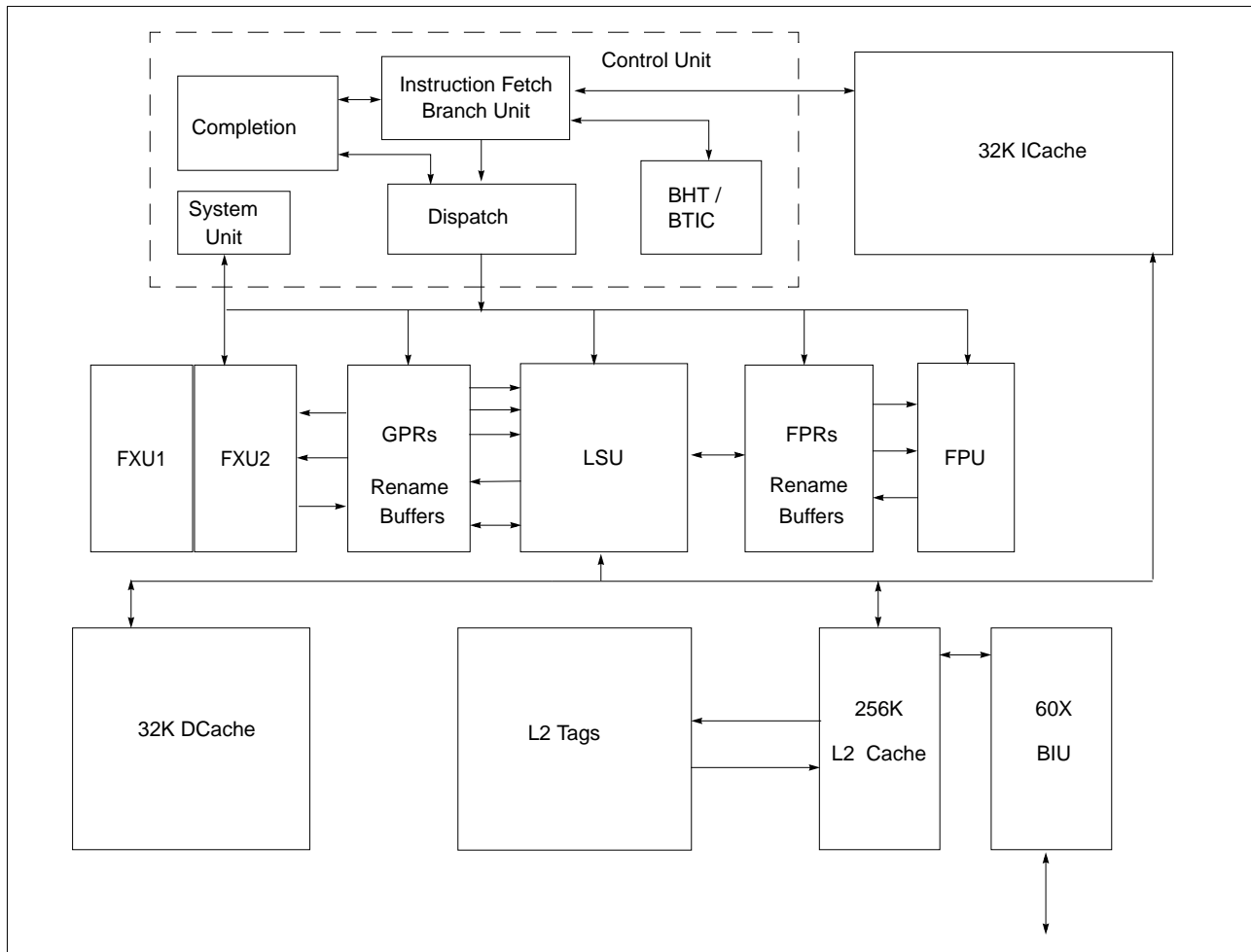
2.0 Overview

The PowerPC 750CX RISC Microprocessor is targeted for high performance, low power systems and a 60X bus. The PowerPC 750CX RISC Microprocessor also includes an internal (256KByte) L2 cache with on-board Error Correction Circuitry (ECC).

2.1 PowerPC 750CX RISC Microprocessor Block Diagram

Figure 1 shows a block diagram of the PowerPC 750CX RISC Microprocessor.

Figure 1. PowerPC 750CX RISC Microprocessor Block Diagram



3.0 Features

This section summarizes the features of the PowerPC 750CX's implementation of the PowerPC architecture. Major features of the PowerPC 750CX are as follows.

- Branch processing unit
 - Four instructions fetched per clock
 - One branch processed per cycle (plus resolving 2 speculations)
 - Up to 1 speculative stream in execution, 1 additional speculative stream in fetch
 - 512-entry branch history table (BHT) for dynamic prediction
 - 64-entry, 4-way set associative branch target instruction cache (BTIC) for eliminating branch delay slots
- Dispatch unit
 - Full hardware detection of dependencies (resolved in the execution units)
 - Dispatch two instructions to six independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, or floating-point)
 - 4-stage pipeline: fetch, dispatch, execute, and complete
 - Serialization control (predispatch, postdispatch, execution, serialization)
- Decode
 - Register file access
 - Forwarding control
 - Partial instruction decode
- Load/store unit
 - One cycle load or store cache access (byte, half-word, word, double-word)
 - Effective address generation
 - Hits under misses (one outstanding miss)
 - Single-cycle misaligned access within double word boundary
 - Alignment, zero padding, sign extend for integer register file
 - Floating-point internal format conversion (alignment, normalization)
 - Sequencing for load/store multiples and string operations
 - Store gathering
 - Cache and TLB instructions
 - Big and little-endian byte addressing supported
 - Misaligned little-endian support in hardware
- Fixed-point units
 - Fixed-point unit 1 (FXU1); multiply, divide, shift, rotate, arithmetic, logical
 - Fixed-point unit 2 (FXU2); shift, rotate, arithmetic, logical
 - Single-cycle arithmetic, shift, rotate, logical
 - Multiply and divide support (multi-cycle)
 - Early out multiply
 - Thirty-two, 32-bit general purpose registers
 - Secondary FXU executes integer add/compare instructions
- Floating-point unit
 - Support for IEEE-754 standard single and double-precision floating-point arithmetic
 - Optimized for single-precision multiply/add
 - Thirty-two, 64-bit floating point registers
 - Enhanced reciprocal estimates
 - 3-cycle latency, 1-cycle throughput, single-precision multiply-add
 - 3-cycle latency, 1-cycle throughput, double-precision add
 - 4-cycle latency, 2-cycle throughput, double-precision multiply-add

- Floating-point unit (continued)
 - Hardware support for divide
 - Hardware support for denormalized numbers
 - Time deterministic non-IEEE mode
- System unit
 - Executes CR logical instructions and miscellaneous system instructions
 - Special register transfer instructions
- L1 Cache structure
 - 32K, 32-byte line, 8-way set associative instruction cache
 - 32K, 32-byte line, 8-way set associative data cache
 - Single-cycle cache access
 - Pseudo-LRU replacement
 - Copy-back or write-through data cache (on a page per page basis)
 - 3-state (MEI) memory coherency
 - Hardware support for data coherency
 - Non-blocking instruction and data cache (one outstanding miss under hits)
 - No snooping of instruction cache
- Memory management unit
 - 128 entry, 2-way set associative instruction TLB
 - 128 entry, 2-way set associative data TLB
 - Hardware reload for TLB's
 - 4 instruction BATs and 4 data BATs
 - Virtual memory support for up to 4 exabytes (2^{52}) virtual memory
 - Real memory support for up to 4 gigabytes (2^{32}) of physical memory
 - Support for big/little-endian addressing
- Level 2 (L2) cache
 - Internal L2 cache controller and 4K-entry tags; 256K data SRAMs
 - Copy-back or write-through data cache on a page basis, or for all L2
 - 64-byte sectored line size
 - L2 frequency at core speed
 - On-board ECC
- Bus interface
 - Compatible with 60X processor interface (some pin functions removed, see Table 11, "Signals Removed from Previous PowerPC 750 Designs" on page 27)
 - 32-bit address bus
 - 64-bit data bus (or 32-bit mode)
 - Core-to-bus frequency multipliers of 2x, 2.5x, 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x, and 10x supported
- Power
 - under 4 watts typical @ 400MHz
- Testability
 - LSSD scan design
 - Powerful diagnostic and test interface through Common On-Chip Processor (COP) and IEEE 1149.1 (JTAG) interface

4.0 General Parameters

The following list provides a summary of the general parameters of the PowerPC 750CX.

| | |
|-------------------|--|
| Technology | 0.18 μ m CMOS Copper technology, six-layer metallization |
| Die Size | 42.7 sq. mm |
| Transistor count | 20 million - including L2 cache |
| Logic design | Fully-static |
| Package | Surface mount 256-lead plastic ball grid array (PBGA) 27x27mm |
| Core power supply | 1.8V +/- 5% |
| I/O power supply | 1.8V +/- 5% 2.5V +/- 5% |

5.0 Electrical and Thermal Characteristics

This section provides both AC and DC electrical specifications and thermal characteristics for the PowerPC 750CX.

5.1 DC Electrical Characteristics

The tables in this section describe the PowerPC 750CX RISC Microprocessor's DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1: Absolute Maximum Ratings

| Characteristic | Symbol | Value (BVSEL = 0) | Value (BVSEL = 1) | Unit |
|---------------------------|-----------|-------------------|-------------------|------|
| Core supply voltage | V_{DD} | -0.3 to 2.0 | -.03 to 2.00 | V |
| PLL supply voltage | AV_{DD} | -0.3 to 2.0 | -0.3 to 2.00 | V |
| 60X bus supply voltage | OV_{DD} | -0.3 to 2.0 | -0.3 to 2.75 | V |
| Input voltage | V_{IN} | -0.3 to 2.0 | -0.3 to 2.75 | V |
| Storage temperature range | T_{STG} | -55 to 150 | -55 to 150 | C |

Note:

1. Functional and tested operating conditions are given in Table 2, "Recommended Operating Conditions¹" on page 12. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed above may affect device reliability or cause permanent damage to the device.
2. Caution: V_{IN} must not exceed OV_{DD} by more than 0.6V at any time, including during power-on reset.
3. Caution: OV_{DD} must not exceed V_{DD}/AV_{DD} by more than 2.0V, except for up to 20ms during power on/off reset.
4. Caution: V_{DD}/AV_{DD} must not exceed OV_{DD} by more than 1.2V, except for up to 20ms during power up/down.
5. Caution: AV_{DD} must not exceed V_{DD} by more than 1.2V, except for up to 20ms during power up/down reset.

Table 2 provides the recommended operating conditions for the PowerPC 750CX.

Table 2: Recommended Operating Conditions¹

| Characteristic | Symbol | Value | Unit |
|------------------------------------|-----------|------------------|------|
| Core supply voltage | V_{DD} | 1.70 to 1.90 | V |
| PLL supply voltage | AV_{DD} | 1.70 to 1.90 | V |
| 60X bus supply voltage (1.8V mode) | OV_{DD} | 1.70 to 1.90 | V |
| 60X bus supply voltage (2.5V mode) | OV_{DD} | 2.375 to 2.625 | V |
| Input voltage | V_{IN} | GND to OV_{DD} | V |
| Die-junction temperature | T_J | 0 to 105 | C |

Note: These are recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

1. See Figure 19, for applicaiton conditions

Table 3 provides the package thermal characteristics for the PowerPC 750CX.

Table 3: Package Thermal Characteristics

| Characteristic | Symbol | Value | Unit |
|---|---------------|-------|------|
| PBGA package thermal resistance, junction to ambient, thermal resistance, convection only * | θ_{JA} | 15.9 | C/W |
| PBGA package thermal resistance, junction-to-ambient thermal resistance, 100 linear ft. per minute* | θ_{JA} | 13.9 | C/W |
| PBGA package thermal resistance, junction-to-board thermal resistance | θ_{JB} | 7.4 | C/W |
| PBGA package thermal resistance, junction-to-case thermal resistance | θ_{JC} | 0.7 | C/W |

Note: * Assumes that the package is soldered to a 2S2P board.

Table 4 provides DC electrical characteristics for the PowerPC 750CX.

Table 4: DC Electrical Specifications
See Table 2 on page 12 for recommended operating conditions.

| Characteristic | Symbol | Voltage | | Unit | Notes |
|---|----------------------|---------|-------|---------|-------|
| | | Min | Max | | |
| Input high voltage (all inputs except SYSCLK) | $V_{IH(1.8V)}$ | 1.24 | 1.90 | V | 2,4 |
| | $V_{IH(2.5V)}$ | 1.70 | 2.625 | V | 2 |
| Input low voltage (all inputs except SYSCLK) | $V_{IL(1.8V)}$ | GND | 0.60 | V | 4 |
| | $V_{IL(2.5V)}$ | GND | 0.70 | V | |
| SYSCLK input high voltage | $CV_{IH(1.8V)}$ | 1.20 | 1.90 | V | |
| | $CV_{IH(2.5V)}$ | 1.90 | 2.625 | V | |
| SYSCLK input low voltage | $CV_{IL(1.8V)}$ | GND | 0.4 | V | |
| Input leakage current, $V_{IN} = OV_{DD} = 2.5V$ | I_{IN} | – | 20 | μA | 3 |
| Input leakage current, $V_{IN} = OV_{DD} = 1.8V$ | I_{IN} | – | 20 | μA | 3 |
| Hi-Z (off state) leakage current, $V_{IN} = OV_{DD} = 2.5V$ | I_{TSI} | – | 20 | μA | 3 |
| Hi-Z (off state) leakage current, $V_{IN} = OV_{DD} = 1.8V$ | I_{TSI} | – | 20 | μA | 3 |
| Output high voltage, $I_{OH} = -4mA$ | $V_{OH(1.8V)}$ | 1.30 | – | V | |
| | $V_{OH(2.5V)}$ | 2.00 | – | V | |
| Output low voltage, $I_{OL} = 4mA$ | $V_{OL(1.8V, 2.5V)}$ | – | 0.4 | V | |
| Capacitance, $V_{IN} = 0V$, $f = 1MHz$ | C_{IN} | – | 5.0 | pF | 1 |

Note:

1. Capacitance values are guaranteed by design and characterization, and are not tested.
2. Maximum input high voltage for short duration (not continuous operation).
3. Additional input current may be attributed to the Level Protection Keeper Lock circuitry. For details, see Section 7.9 on Page 38.
4. V_{IH} and V_{IL} minimum levels are set as a percentage of V_{DD} . V_{IH} is 65% and V_{IL} is 35% respectively.

Table 5 provides the power consumption for the PowerPC 750CX.

Table 5: Power Consumption

See Table 2 on page 12 for recommended operating conditions.

| | Representative Processor Frequency | | | | Unit | Notes |
|--|------------------------------------|--------|--------|--------|------|---------|
| | 366MHz | 400MHz | 466MHz | 500MHz | | |
| Full-On Mode | | | | | | |
| Typical ($V_{DD} = 1.8V$) ($OV_{DD}=1.8$)(65C) | 3.3 | 3.5 | 4.0 | 4.3 | W | 1,3,4,5 |
| Maximum ($V_{DD} = 1.9V$) ($OV_{DD}=1.9$)(105C) | 6.7 | 7.1 | 7.7 | 8.3 | W | 1,2,4,5 |
| Typical ($V_{DD} = 1.8V$) ($OV_{DD}=2.5$)(65C) | 3.3 | 3.5 | 4.0 | 4.3 | W | 1,3,4,5 |
| Maximum ($V_{DD} = 1.9V$) ($OV_{DD}=2.62$)(105C) | 6.7 | 7.1 | 7.7 | 8.3 | W | 1,2,4,5 |
| Doze Mode | | | | | | |
| Maximum ($V_{DD} = 1.9V$) ($OV_{DD}=1.9$)(105C) | 3.7 | 4.0 | 4.5 | 4.6 | W | 1,2,4,5 |
| Nap Mode | | | | | | |
| Maximum ($V_{DD} = 1.9V$) ($OV_{DD}=1.9$)(105C) | 1.5 | 1.5 | 1.6 | 1.7 | W | 1,2,4,5 |
| Sleep Mode | | | | | | |
| Maximum ($V_{DD} = 1.9V$) ($OV_{DD}=1.9$)(105C) | 1.4 | 1.4 | 1.5 | 1.6 | W | 1,2,4,5 |
| Note: 1. These values apply for all valid 60X buses. The values do not include I/O Supply Power (OV_{DD}) or PLL/DLL supply power (AV_{DD}). OV_{DD} power is system dependent, but is typically <10% of V_{DD} power. 2. Maximum power is measured at $V_{DD} = 1.90V$ and assumes worst case process parameters. 3. Typical power is an estimate of the average value measured at $V_{DD} = AV_{DD} = 1.8V$, $OV_{DD} = 1.80/2.5V$ in a system executing typical applications and benchmark sequences. 4. Full-on mode uses a worst case instruction mix. 5. Guaranteed by design and characterization, and is not tested. | | | | | | |

5.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the PowerPC 750CX. After fabrication, parts are sorted by maximum processor core frequency as shown in the Section 5.2.1 on Page 14, and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG(0-3) signals.

5.2.1 Clock AC Specifications

Table 6 provides the clock AC timing specifications as defined in Figure 2.

Table 6: Clock AC Timing Specifications^{1,6}

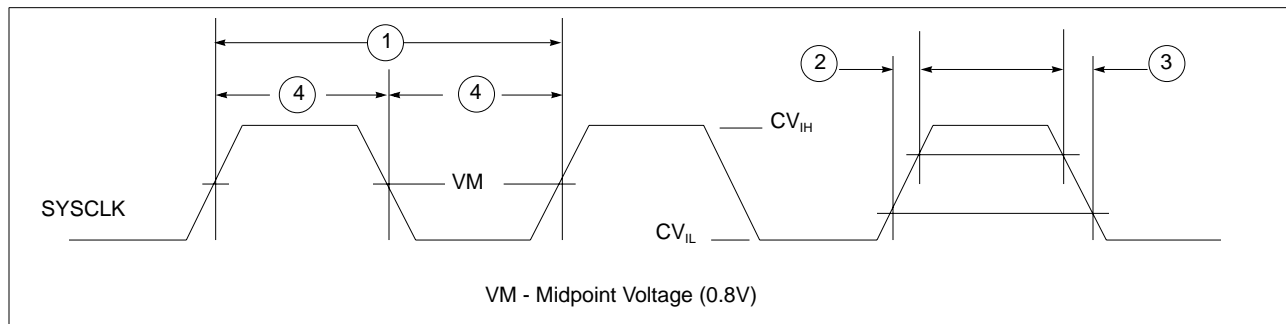
See Table 2 on page 12, for recommended operating conditions.

| Num | Characteristic | Value | | Unit | Notes |
|-----|---------------------------------------|-------|------|---------|-------|
| | | Min | Max | | |
| | Processor frequency | 300 | 500 | MHz | 6 |
| | SYSCLK frequency | 31 | 133 | MHz | 1 |
| 1 | SYSCLK cycle time | 7.5 | 32 | ns | |
| 2,3 | SYSCLK rise and fall time (slew rate) | 1.0 | 2.0 | volt/ns | 2,3 |
| 4 | SYSCLK duty cycle measured at 0.8V | 25 | 75 | % | 3 |
| | SYSCLK jitter | – | ±150 | ps | 4,3 |
| | Internal PLL relock time | – | 100 | µs | 5 |

Note:

1. Caution: The SYSCLK frequency and the PLL_CFG[0-3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0-3] signal description in Section "PLL Configuration," on page 28 for valid PLL_CFG[0-3] settings.
2. Rise and fall times for the SYSCLK input are measured from 0.4 to 1.2V.
3. Timing is guaranteed by design and characterization, and is not tested.
4. The total input jitter (short term and long term combined) must be under ±150ps.
5. Relock timing is guaranteed by design and characterization, and is not tested. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that HRESET must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.
6. For applications with processor frequencies below 300MHz, application conditions need to be investigated.

Figure 2. SYSCLK Input Timing Diagram



5.3 60X Bus Input AC Specifications

Table 7 provides the 60X bus input AC timing specifications for the PowerPC 750CX as defined in Figure 3 and Figure 4.

Table 7: 60X Bus Input Timing Specifications^{1,6,8}

See Table 2 on page 12 for operating conditions.

| Num | Characteristic | 1.8V Mode | | 2.5V Mode | | Unit | Notes |
|-----|--|-----------|------|-----------|------|---------------------|-------|
| | | Min | Max. | Min. | Max. | | |
| 10a | Address/Data/Transfer attribute inputs valid to SYSCLK (input setup) | 1.4 | — | 1.4 | — | ns | 2 |
| 10b | All other inputs valid to SYSCLK (input setup) | 1.4 | — | 1.4 | — | ns | 3 |
| 10c | Mode select input setup to $\overline{\text{HRESET}}$ ($\overline{\text{QACK}}$) | 8 | — | 8 | — | t_{sysclk} | 4,5,7 |
| 10d | TS to SYSCLK (input setup) | 1.6 | — | 1.6 | — | — | — |
| 10e | DBW0 to SYSCLK (input setup) | 2.1 | — | 2.1 | — | — | — |
| 11a | SYSCLK to inputs invalid (input hold) | 1.2 | — | 1.2 | — | ns | 2 |
| 11b | $\overline{\text{HRESET}}$ to mode select input hold ($\overline{\text{QACK}}$) | 0 | — | 0 | — | ns | 4,7 |

Note:

- Input specifications are measured from the midpoint voltage (0.9V) of the signal in question to the midpoint voltage of the rising edge of the input SYSCLK. Input and output timings are measured at the pin (see Figure 3).
- Address/Data Transfer Attribute inputs are composed of all bidirectional and input signals except those listed in Note 3.
- All other signal inputs are composed of the following: $\overline{\text{TA}}$, $\overline{\text{QACK}}$, and $\overline{\text{ARTRY}}$.
- The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 4 on page 17).
- t_{sysclk} is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
- These values are guaranteed by design, and are not tested.
- This specification is for configuration mode select only. Also note that the $\overline{\text{HRESET}}$ must be held asserted for a **minimum of 255 bus clocks** after the PLL relock time during the power-on reset sequence.
- These timings are valid for processor frequencies up to 466MHz. 500MHz timing behavior and characterization is being evaluated at this time.

Figure 3 provides the input timing diagram for the PowerPC 750CX.

Figure 3. Input Timing Diagram

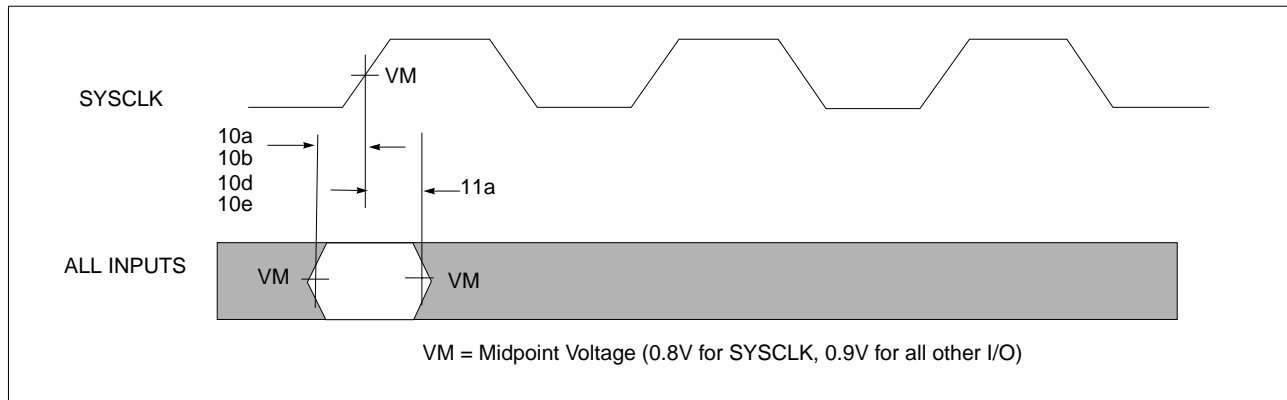
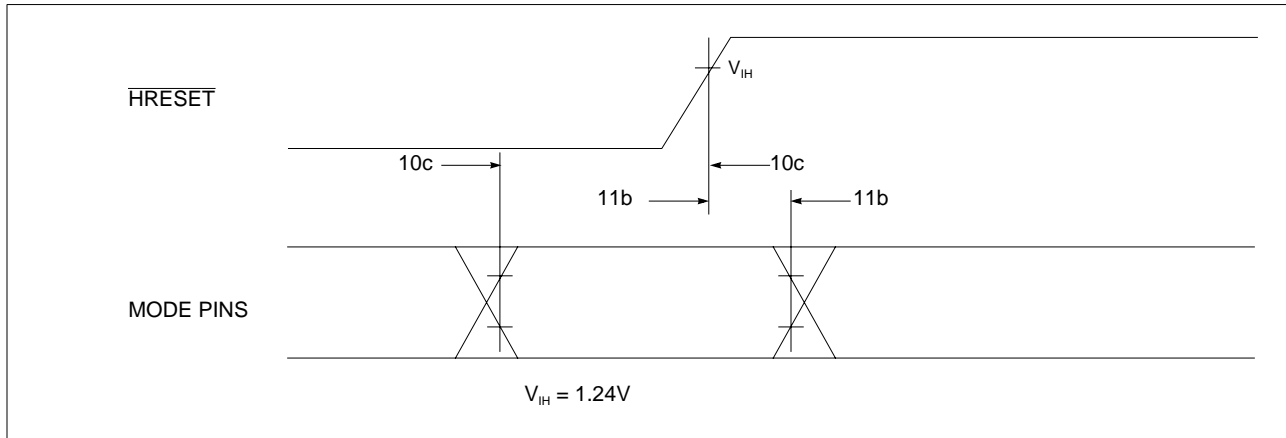


Figure 4 provides the mode select input timing diagram for the PowerPC 750CX.

Figure 4. Mode Select Input Timing Diagram



5.4 60X Bus Output AC Specifications

Table 8 provides the 60X bus output AC timing specifications for the PowerPC 750CX as defined in Figure 6 on page 19.

Table 8: 60X Bus Output AC Timing Specifications^{1,4,6,7}
See Table 2 on page 12 for operating conditions.

| Num | Characteristic | 1.8V Mode | | 2.5V Mode | | Unit | Notes |
|-----|---|---------------------------------|------|---------------------------------|------|---------------------|---------|
| | | Min. | Max. | Min. | Max. | | |
| 12 | SYSCLK to Output Driven (Output Enable Time) | 0.3 | | 0.3 | | ns | |
| 13 | SYSCLK to Output Valid | – | 2.31 | – | 2.61 | ns | |
| 14 | SYSCLK to Output Invalid (Output Hold) | 0.400 | | 0.400 | | ns | 2 |
| 15 | SYSCLK to Output High Impedance (all signals except $\overline{\text{ARTRY}}$) | – | 2.5 | – | 2.5 | ns | |
| 16 | SYSCLK to $\overline{\text{ARTRY}}$ high impedance before precharge | – | 3.0 | – | 3.0 | ns | |
| 17 | SYSCLK to $\overline{\text{ARTRY}}$ precharge enable | $0.2 * t_{\text{SYSCLK}} + 1.0$ | | $0.2 * t_{\text{SYSCLK}} + 1.0$ | | ns | 2, 3, 5 |
| 18 | Maximum delay to $\overline{\text{ARTRY}}$ precharge | | 1 | | 1 | t_{SYSCLK} | 3, 5 |
| 19 | SYSCLK to $\overline{\text{ARTRY}}$ high impedance after precharge | | 2 | | 2 | t_{SYSCLK} | 3, 5 |

Note:

- All output specifications are measured from the midpoint voltage (0.8V) of the rising edge of SYSCLK to the midpoint voltage of the signal in question defined in figure 5. Both input and output timings are measured at the pin. Timings are determined by design.
- This minimum parameter assumes $CL = 0\text{pF}$.
- t_{SYSCLK} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration of the parameter in question.
- Output signal transitions are defined in figure 5.
- Nominal precharge width for $\overline{\text{ARTRY}}$ is $1.0 t_{\text{SYSCLK}}$.
- Guaranteed by design and characterization, and not tested.
- These timings are valid for processors up to 466MHz. 500MHz processor timing behavior and characterization are being evaluated at this time.

Figure 5. Output Valid Timing Definition

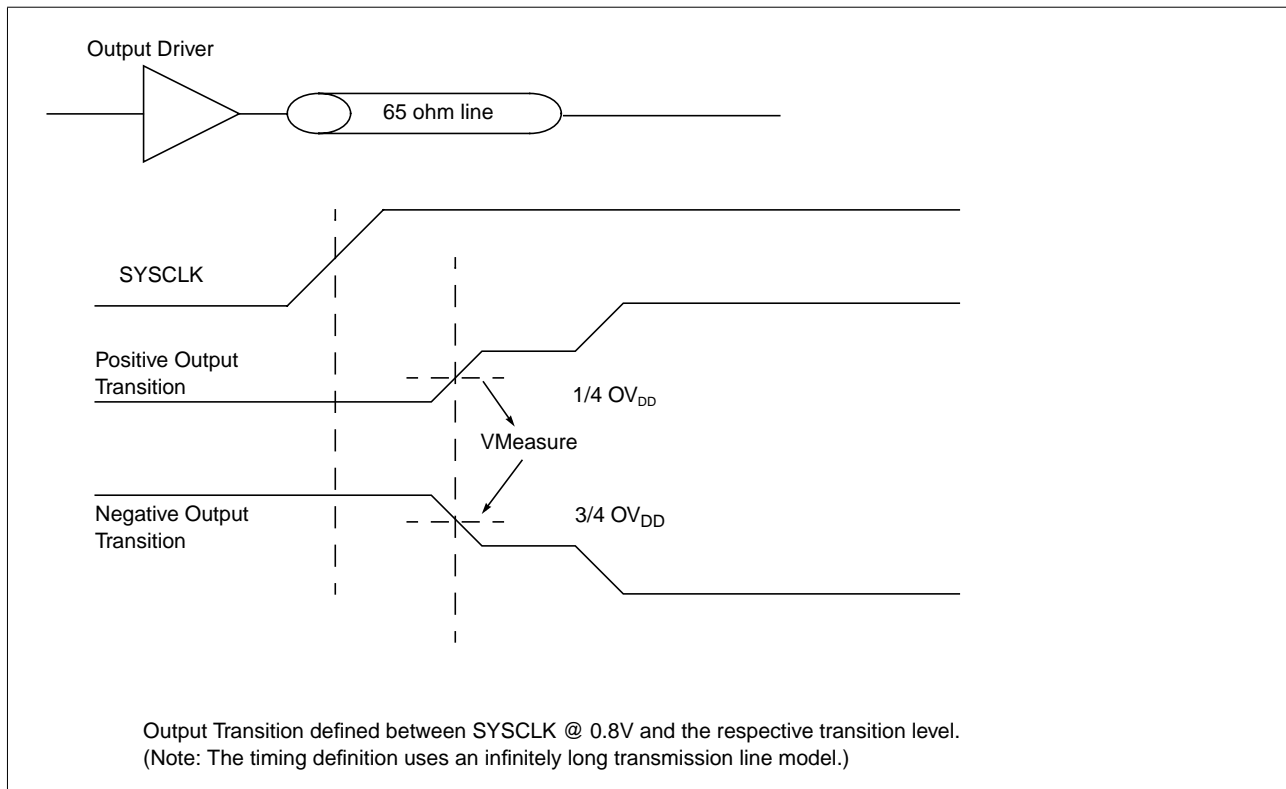
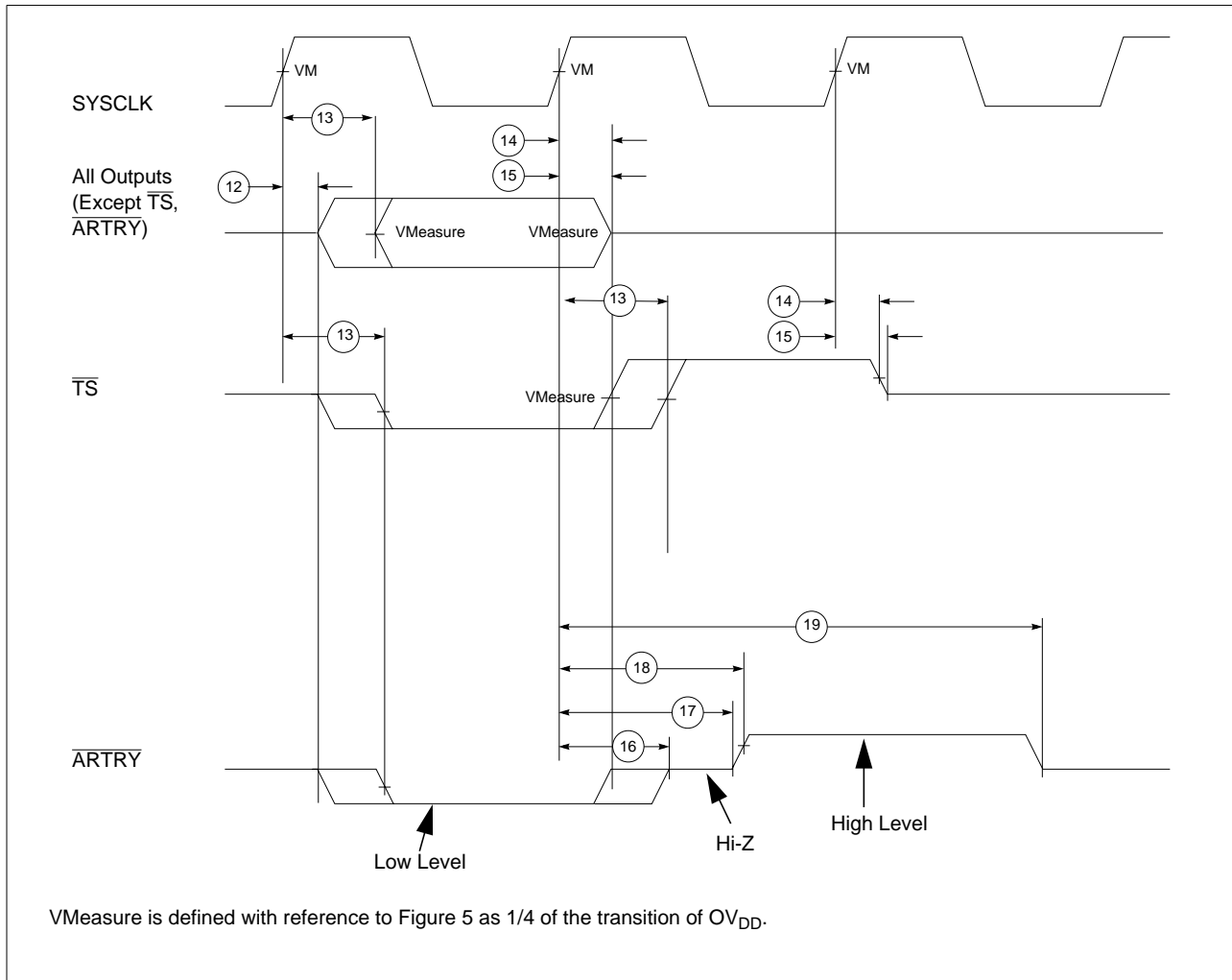


Figure 6. Output Timing Diagram for PowerPC 750CX RISC Microprocessor



5.4.1 IEEE 1149.1 AC Timing Specifications

Table 9 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 7, Figure 8, Figure 9, and Figure 10. The five JTAG signals are; TDI, TDO, TMS, TCK, and \overline{TRST} .

Table 9: JTAG AC Timing Specifications (Independent of SYSCLK)

See Table 2 on page 12 for operating conditions..

| Num | Characteristic | Min | Max | Unit | Notes |
|-----|---|-----|-----|------|-------|
| | TCK frequency of operation | 0 | 25 | MHz | |
| 1 | TCK cycle time | 40 | — | ns | |
| 2 | TCK clock pulse width measured at 1.1V | 15 | — | ns | |
| 3 | TCK rise and fall times | 0 | 2 | ns | 4 |
| 4 | Specification obsolete, intentionally omitted | | | | |
| 5 | $\overline{\text{TRST}}$ assert time | 25 | — | ns | 1 |
| 6 | Boundary-scan input data setup time | 0 | — | ns | 2 |
| 7 | Boundary-scan input data hold time | 13 | — | ns | 2 |
| 8 | TCK to output data valid | — | 8 | ns | 3, 5 |
| 9 | TCK to output high impedance | 3 | 19 | ns | 3, 4 |
| 10 | TMS, TDI data setup time | 0 | — | ns | |
| 11 | TMS, TDI data hold time | 15 | — | ns | |
| 12 | TCK to TDO data valid | 2.5 | 12 | ns | 5 |
| 13 | TCK to TDO high impedance | 3 | 9 | ns | 4 |
| 14 | TCK to output data invalid (output hold) | 0 | — | ns | |

Note:

1. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. Guaranteed by design.
2. Non-JTAG signal input timing with respect to TCK.
3. Non-JTAG signal output timing with respect to TCK.
4. Guaranteed by characterization and not tested.
5. Minimum specification guaranteed by characterization and not tested.

Figure 7 provides the JTAG clock input timing diagram.

Figure 7. JTAG Clock Input Timing Diagram

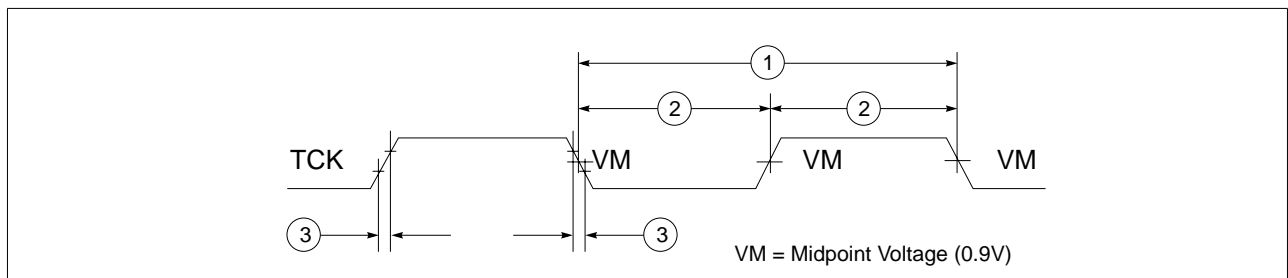


Figure 8 provides the $\overline{\text{TRST}}$ timing diagram.

Figure 8. $\overline{\text{TRST}}$ Timing Diagram

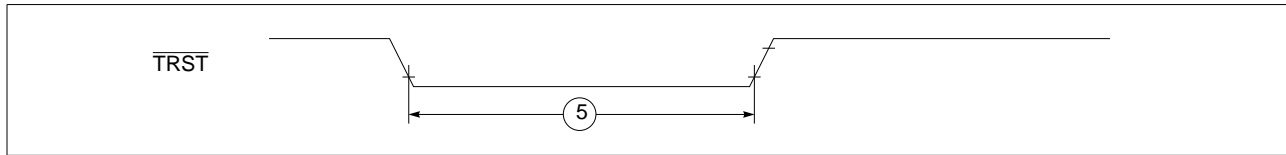


Figure 9 provides the boundary-scan timing diagram.

Figure 9. Boundary-Scan Timing Diagram

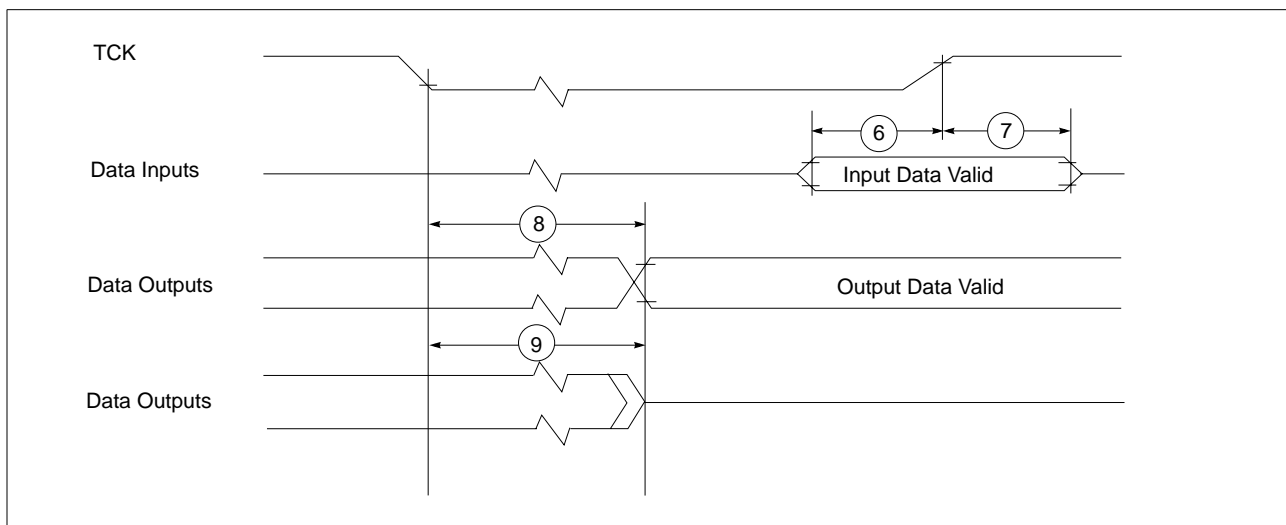
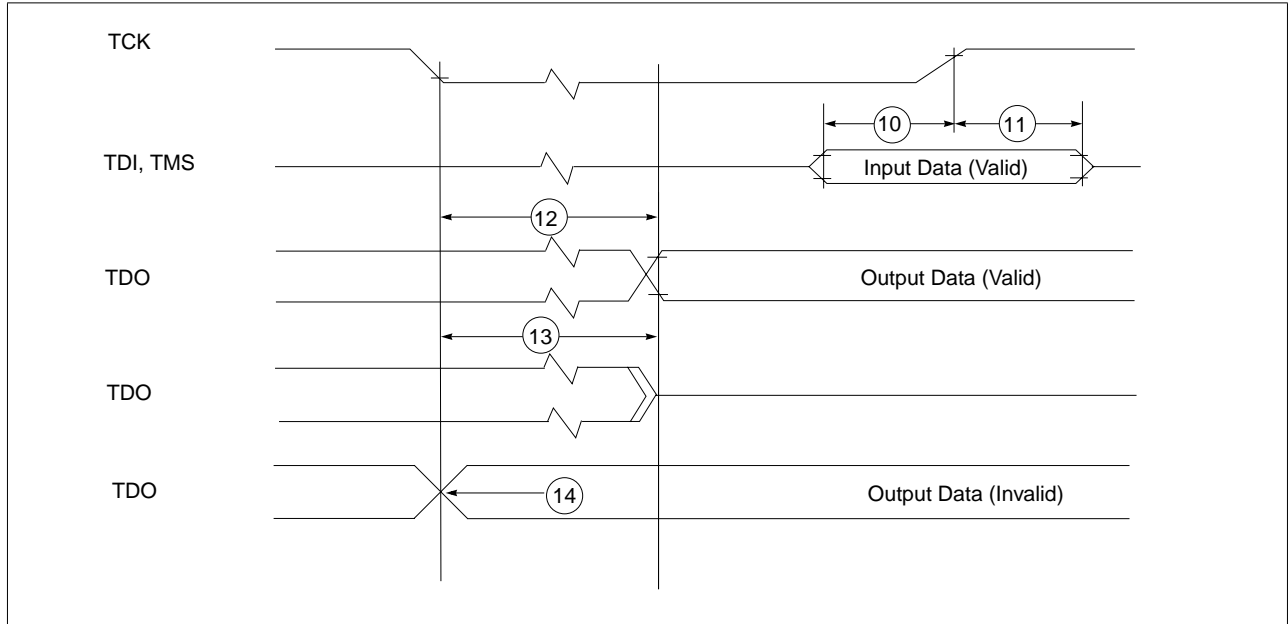


Figure 10 provides the test access port timing diagram.

Figure 10. Test Access Port Timing Diagram



6.0 PowerPC 750CX Microprocessor Dimension and Physical Signal Assignments

IBM offers a plastic ball grid array, PBGA, which supports 256 balls as the PowerPC 750CX package.

The following sections contain several views of the package, pin information, and a pin listing.

Figure 11 shows the pinout of the 256 PBGA package as viewed from the solder ball surface. Figure 12 shows the side profile of the 256 PBGA package including the height from the top of the copper heat spreader to the bottom of the solder balls. Figure 13 provides a more detailed side profile including the encapsulant (glob) referenced.

Figure 11. Pinout of the 256 PBGA Package as Viewed from Solder Ball side

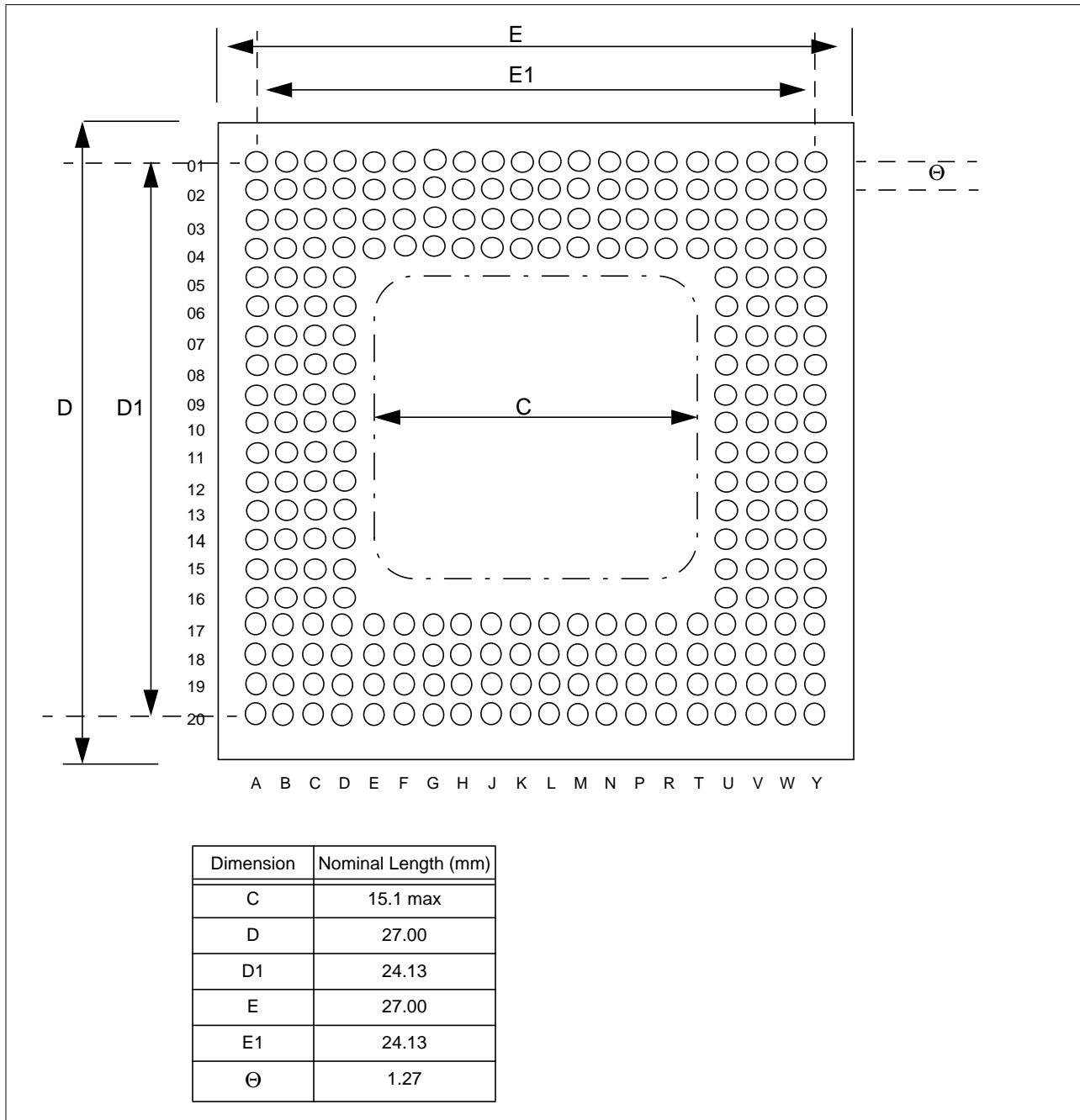


Figure 12. Side Profile View of PBGA

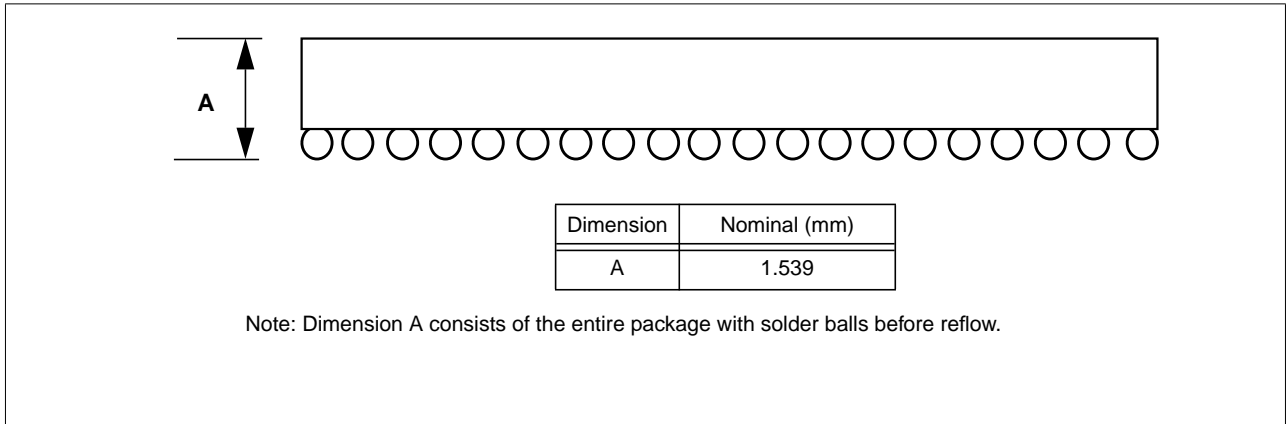
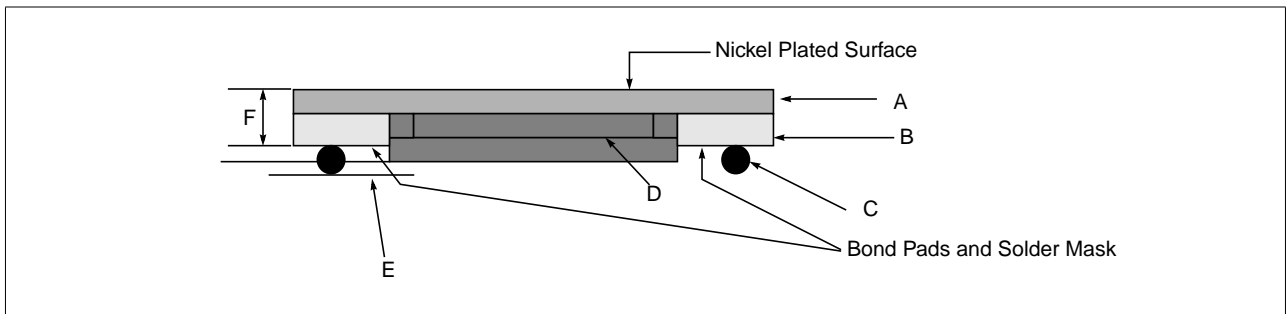


Figure 13. Side Profile View Showing Exposed Cavity



| Item | Description | Length (mm) | Height (mm) |
|------|--|-------------|-------------|
| A | Cu Heat Spreader | 27 | .356 |
| B | Laminate including plating | 27 | .585 |
| C | Solder ball | N/A | .60 |
| D | Chip Cavity | 15.1 max | N/A |
| E | Minimum Glop to Solder Ball Height | N/A | .244 |
| F | Cu Heat Spreader, Laminate, Bond Pads, and Plating | N/A | .955 |

Figure 14. PowerPC 750CX Microprocessor Ball Placement

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|---|----------------------------|--------------------------------|-------------------------------|--------------------------|------|------|------|------|------|------|------|------|------|------|------|------|------|--------------------------|------------------------|--------------------------|
| A | g | g | dh3 | g | dh9 | dh11 | dh13 | dh15 | dh16 | dh19 | dh20 | dh23 | dh24 | dh26 | dh28 | dh30 | g | a4 | g | g |
| B | g | g | vdd | dh4 | dh6 | dh8 | dh12 | g | dh18 | g | g | dh21 | g | dh27 | dh31 | a1 | a3 | vdd | g | g |
| C | dh2 | vdd | g | vdd | ovdd | dh7 | dh10 | dh14 | dh17 | g | g | dh22 | dh25 | dh29 | a0 | ovdd | vdd | g | vdd | a5 |
| D | ovdd | dh1 | vdd | g | vdd | dh5 | ovdd | vdd | ovdd | vdd | vdd | ovdd | vdd | ovdd | a2 | vdd | g | vdd | a6 | g |
| E | $\overline{\text{hreset}}$ | dh0 | $\overline{\text{dbw0}}$ * | vdd | | | | | | | | | | | | | vdd | ovdd | a8 | a11 |
| F | pllcfg0 | $\overline{\text{ssd_mode}}$ | $\overline{\text{mcp}}$ | l1_tstclk | | | | | | | | | | | | | a7 | a9 | a10 | a13 |
| G | pllcfg2 | pllcfg1 | sysclk | ovdd | | | | | | | | | | | | | ovdd | a12 | a14 | a15 |
| H | bvsel | pllcfg3 | avdd | vdd | | | | | | | | | | | | | vdd | tt_0 | g | tt_1 |
| J | g | $\overline{\text{int}}$ | $\overline{\text{ckstp_in}}$ | ovdd | | | | | | | | | | | | | ovdd | tt_3 | $\overline{\text{ts}}$ | tt_2 |
| K | $\overline{\text{sreset}}$ | $\overline{\text{qack}}$ | g | vdd | | | | | | | | | | | | | vdd | g | g | tt_4 |
| L | $\overline{\text{qreq}}$ | g | g | vdd | | | | | | | | | | | | | vdd | g | g | tsiz0 |
| M | $\overline{\text{dbg}}$ | $\overline{\text{tea}}$ | $\overline{\text{artry}}$ | ovdd | | | | | | | | | | | | | ovdd | tsiz2 | tsiz1 | $\overline{\text{ta}}$ |
| N | $\overline{\text{br}}$ | g | tdo | vdd | | | | | | | | | | | | | vdd | $\overline{\text{aack}}$ | g | $\overline{\text{tbst}}$ |
| P | $\overline{\text{bg}}$ | $\overline{\text{ckstp_out}}$ | tdi | ovdd | | | | | | | | | | | | | ovdd | a19 | a17 | a16 |
| R | $\overline{\text{wt}}$ | $\overline{\text{gbl}}$ | tms | $\overline{\text{trst}}$ | | | | | | | | | | | | | a24 | a22 | a21 | a18 |
| T | dl31 | $\overline{\text{ci}}$ | tck | vdd | | | | | | | | | | | | | vdd | ovdd | a23 | a20 |
| U | ovdd | dl30 | vdd | g | vdd | dl26 | ovdd | vdd | ovdd | vdd | vdd | ovdd | vdd | ovdd | a29 | vdd | g | vdd | a25 | g |
| V | dl29 | vdd | g | vdd | ovdd | dl24 | dl21 | dl17 | dl14 | g | g | dl9 | dl6 | dl2 | a31 | ovdd | vdd | g | vdd | a26 |
| W | g | g | vdd | dl27 | dl25 | dl23 | dl19 | g | dl13 | g | g | dl10 | g | dl4 | dl0 | a30 | a28 | vdd | g | g |
| Y | g | g | dl28 | g | dl22 | dl20 | dl18 | dl16 | dl15 | dl12 | dl11 | dl8 | dl7 | dl5 | dl3 | dl1 | g | a27 | g | g |

(Above view is looking down from above the PowerPC 750CX placed and soldered on the system board.)

** $\overline{\text{DBW0}}$ multiplexed with L2_TSTCLK function, see Section 7.9.4 on Page 39 for details.

Table 10: Signal Listing for the 256 PBGA Package

| Signal Name | Pin Count | Active | I/O | Notes |
|---|-----------|--------|--------|--|
| A0-A31 | 32 | High | I/O | |
| AACK | 1 | Low | Input | |
| ARTRY | 1 | Low | I/O | |
| BG | 1 | Low | Input | |
| BR | 1 | Low | Output | |
| C \bar{I} | 1 | Low | Output | |
| CKSTP_IN | 1 | Low | Input | |
| CKSTP_OUT ² | 1 | Low | Output | |
| DBG | 1 | Low | Input | |
| DH0-DH31 | 32 | High | I/O | |
| DL0-DL31 | 32 | High | I/O | |
| G $\bar{B}L$ | 1 | Low | I/O | |
| HRESET | 1 | Low | Input | |
| I $\bar{N}T$ | 1 | Low | Input | |
| L1_TSTCLK ¹ | 1 | High | Input | |
| DBW \bar{O} /L2_TSTCLK ^{1,2,3} | 1 | High | Input | |
| LSSD_MODE ¹ | 1 | Low | Input | |
| MCP | 1 | Low | Input | |
| PLL_CFG[0-3] | 4 | High | Input | |
| QACK ² | 1 | Low | Input | OPTIONAL: 64/ 32-Bit Data Bus mode select. This function will be set when HRESET transitions (low to high). QACK: low = 64-bit mode, high = 32-bit mode. |
| QREQ | 1 | Low | Output | |
| SRESET | 1 | Low | Input | |
| SYSCLK | 1 | — | Input | |
| TA | 1 | Low | Input | |
| TB $\bar{S}T$ | 1 | Low | I/O | |
| TCK | 1 | High | Input | |
| TDI | 1 | High | Input | |
| TDO | 1 | High | Output | |
| TEA | 1 | Low | Input | |
| TMS | 1 | High | Input | |
| TR $\bar{S}T$ | 1 | Low | Input | |

Note:

1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
2. The CKSTP_OUT signal in test mode allows viewing the PowerPC 750CX RISC Microprocessor internal clocks. The QACK signal allows selection of 32-bit mode. (See the *PowerPC 750CX RISC Microprocessor User's Manual* for more information.)
3. L2-TSTCLK in normal mode is DBW \bar{O} , for details, see Section 7.9.4 on Page 39.

Table 10: Signal Listing for the 256 PBGA Package (cont.)

| Signal Name | Pin Count | Active | I/O | Notes |
|------------------|-----------|--------|--------|---|
| TS | 1 | Low | I/O | |
| TSIZ0-TSIZ2 | 3 | High | Output | |
| TT0-TT4 | 5 | High | I/O | |
| \overline{WT} | 1 | Low | Output | |
| BVSEL | 1 | High | Input | Pin set LOW = 1.8V , pin set HIGH = 2.5V (this is supported for DD2.X) |
| AV _{DD} | 1 | | | Supply for PLL |
| OV _{DD} | 24 | | | Supply for Receiver/Drivers |
| V _{DD} | 40 | | | Supply for Core |
| Ground | 53 | | | Common Ground |

Note:

1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
2. The CKSTP_OUT signal in test mode allows viewing the PowerPC 750CX RISC Microprocessor internal clocks.
The QACK signal allows selection of 32-bit mode. (See the *PowerPC 750CX RISC Microprocessor User's Manual* for more information.)
3. L2-TSTCLK in normal mode is \overline{DBWO} , for details, see Section 7.9.4 on Page 39.

Table 11: Signals Removed from Previous PowerPC 750 Designs

| Signal Name | Pin Count | Active | I/O | Notes |
|-------------|-----------|--------|--------|-------|
| ABB | 1 | Low | I/O | |
| DBB | 1 | Low | I/O | |
| DBDIS | 1 | Low | Input | |
| RSRV | 1 | Low | Output | |
| SMI | 1 | Low | Input | |
| TBEN | 1 | High | Input | |
| VOLTDDET | 1 | High | Output | |
| AP0-3 | 4 | High | I/O | |
| DP0-7 | 8 | High | I/O | |
| DRTRY | 1 | Low | Input | |
| TLBISYNC | 1 | Low | Input | |



Table 12: Signal Locations

| Signal | Ball Location | Signal | Ball Location | Signal | Ball Location | Signal | Ball Location |
|--------|---------------|--------|---------------|--------|---------------|---|---------------|
| A0 | C15 | DH0 | E2 | DL0 | W15 | AACK | N18 |
| A1 | B16 | DH1 | D2 | DL1 | Y16 | ARTRY | M3 |
| A2 | D15 | DH2 | C1 | DL2 | V14 | BG | P1 |
| A3 | B17 | DH3 | A3 | DL3 | Y15 | BR | N1 |
| A4 | A18 | DH4 | B4 | DL4 | W14 | BVSEL | H1 |
| A5 | C20 | DH5 | D6 | DL5 | Y14 | CI | T2 |
| A6 | D19 | DH6 | B5 | DL6 | V13 | CKSTP_IN | J3 |
| A7 | F17 | DH7 | C6 | DL7 | Y13 | CKSTP_OUT | P2 |
| A8 | E19 | DH8 | B6 | DL8 | Y12 | DBG | M1 |
| A9 | F18 | DH9 | A5 | DL9 | V12 | GBL | R2 |
| A10 | F19 | DH10 | C7 | DL10 | W12 | HRESET | E1 |
| A11 | E20 | DH11 | A6 | DL11 | Y11 | INT | J2 |
| A12 | G18 | DH12 | B7 | DL12 | Y10 | L1_TSTCLK | F4 |
| A13 | F20 | DH13 | A7 | DL13 | W9 | DBWO/L2_TSTCLK ¹ | E3 |
| A14 | G19 | DH14 | C8 | DL14 | V9 | LSSD_MODE | F2 |
| A15 | G20 | DH15 | A8 | DL15 | Y9 | MCP | F3 |
| A16 | P20 | DH16 | A9 | DL16 | Y8 | PLL_CFG0 | F1 |
| A17 | P19 | DH17 | C9 | DL17 | V8 | PLL_CFG1 | G2 |
| A18 | R20 | DH18 | B9 | DL18 | Y7 | PLL_CFG2 | G1 |
| A19 | P18 | DH19 | A10 | DL19 | W7 | PLL_CFG3 | H2 |
| A20 | T20 | DH20 | A11 | DL20 | Y6 | QACK (Also used for 64/32-bit DB select.) | K2 |
| A21 | R19 | DH21 | B12 | DL21 | V7 | QREQ | L1 |
| A22 | R18 | DH22 | C12 | DL22 | Y5 | SRESET | K1 |
| A23 | T19 | DH23 | A12 | DL23 | W6 | SYSCLK | G3 |
| A24 | R17 | DH24 | A13 | DL24 | V6 | TA | M20 |
| A25 | U19 | DH25 | C13 | DL25 | W5 | TBST | N20 |
| A26 | V20 | DH26 | A14 | DL26 | U6 | TCK | T3 |
| A27 | Y18 | DH27 | B14 | DL27 | W4 | TDI | P3 |
| A28 | W17 | DH28 | A15 | DL28 | Y3 | TDO | N3 |
| A29 | U15 | DH29 | C14 | DL29 | V1 | TEA | M2 |
| A30 | W16 | DH30 | A16 | DL30 | U2 | TMS | R3 |
| A31 | V15 | DH31 | B15 | DL31 | T1 | TRST | R4 |
| | | | | | | TS | J19 |
| | | | | | | TSIZ0 | L20 |
| | | | | | | TSIZ1 | M19 |
| | | | | | | TSIZ2 | M18 |
| | | | | | | TT0 | H18 |
| | | | | | | TT1 | H20 |
| | | | | | | TT2 | J20 |
| | | | | | | TT3 | J18 |
| | | | | | | TT4 | K20 |
| | | | | | | WT | R1 |

1. See Section 7.9.4 on Page 39 for a detailed discussion.

Table 13: Voltage and Ground Assignments

| AV _{DD} | OV _{DD} | V _{DD} | V _{DD} | GND | GND |
|------------------|------------------|-----------------|-----------------|-----|-----|
| H3 | M4 | B3 | L4 | A1 | L3 |
| | M17 | B18 | L17 | A2 | L18 |
| | P4 | C2 | N4 | A4 | L19 |
| | P17 | C4 | N17 | A17 | N2 |
| | T18 | C17 | T4 | A19 | N19 |
| | U1 | C19 | T17 | A20 | U4 |
| | U7 | D3 | U3 | B1 | U17 |
| | U9 | D5 | U5 | B2 | U20 |
| | U12 | D8 | U8 | B8 | V3 |
| | U14 | D10 | U10 | B10 | V10 |
| | V5 | D11 | U11 | B11 | V11 |
| | V16 | D13 | U13 | B13 | V18 |
| | C5 | D16 | U16 | B19 | W1 |
| | C16 | D18 | U18 | B20 | W2 |
| | D1 | E4 | V2 | C3 | W8 |
| | D7 | E17 | V4 | C10 | W10 |
| | D9 | H4 | V17 | C11 | W11 |
| | D12 | H17 | V19 | C18 | W13 |
| | D14 | K4 | W3 | D4 | W19 |
| | E18 | K17 | W18 | D17 | W20 |
| | G4 | | | D20 | Y1 |
| | G17 | | | H19 | Y2 |
| | J4 | | | J1 | Y4 |
| | J17 | | | K3 | Y17 |
| | | | | K18 | Y19 |
| | | | | K19 | Y20 |
| | | | | L2 | |

7.0 System Design Information

This section provides electrical and thermal design recommendations for successful application of the PowerPC 750CX.

7.1 PLL Configuration

The PowerPC 750CX PLL is configured by the PLL_CFG[0-3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the PowerPC 750CX is shown in the following table for nominal frequencies.

Table 14: PowerPC 750CX Microprocessor PLL Configuration

| PLL_CFG (0:3) | | Processor to Bus Frequency Ratio (r) | Frequency Range Supported by VCO having an example range of $VCO_{MIN} = 500$ to $VCO_{MAX} = 1GHz^6$ | | | |
|------------------|-----|---|--|------------------|--------|------------------|
| bin | dec | | SYSCLK | | Core | |
| | | | Min | Max | Min | Max |
| 0000 | 0 | 2.5x | 120 | 133 ⁵ | 300 | 333 |
| 0001 | 1 | 7.5x | 40 | 67 | 300 | 500 ⁶ |
| 0010 | 2 | 7x | 43 | 71 | | |
| 0011 | 3 | PLL Bypass ³ | N/A | N/A | N/A | N/A |
| 0100 | 4 | 2x | Note 1 | Note 1 | Note 1 | Note 1 |
| 0101 | 5 | 6.5x | 46 | 77 | 300 | 500 ⁶ |
| 0110 | 6 | 10x | 31 ² | 50 | 310 | 500 ⁶ |
| 0111 | 7 | 4.5x | 66 | 111 | 300 | 500 ⁶ |
| 1000 | 8 | 3x | 100 | 133 ⁵ | | |
| 1001 | 9 | 5.5x | 55 | 109 | | |
| 1010 | 10 | 4x | 75 | 150 | | |
| 1011 | 11 | 5x | 40 | 120 | | |
| 1100 | 12 | 8x | 37 | 75 | | |
| 1101 | 13 | 6x | 50 | 100 | | |
| 1110 | 14 | 3.5x | 85 | 172 | | |
| 1111 | 15 | Off ⁴ | N/A | N/A | | |

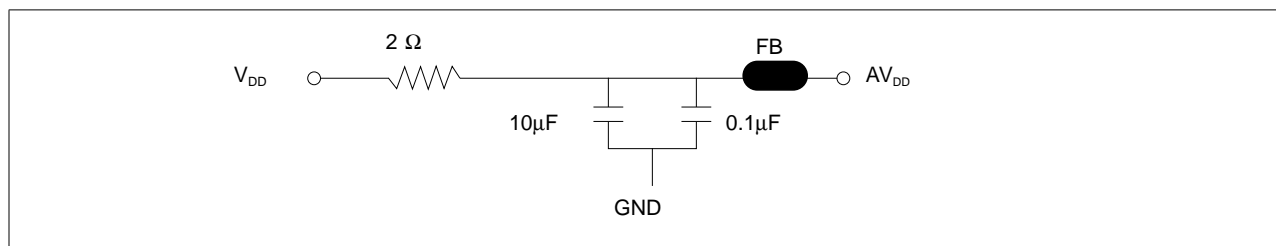
Note:

1. The 2X Processor to Bus Ratio is currently not supported.
2. SYSCLK min is limited by the lowest frequency that manufacturing will support, see section "Clock AC Specifications" on page 14 for valid SYSCLK and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only. **Note:** The AC timing specifications given in the document do not apply in PLL-bypass mode.
4. In Clock - off mode, no clocking occurs inside the PowerPC 750CX regardless of the SYSCLK input.
5. The SYSCLK limit is 133MHz, as specified in Table 6 on page 15. Applications requiring SYSCLK over 133MHz will be investigated by application conditions.
6. VCO_{MAX} is specified in this table by the maximum core processor speed. The VCO maximum of 1GHz reflects a processor core speed of 500MHz.

7.2 PLL Power Supply Filtering

The AV_{DD} power signal is provided on the PowerPC 750CX to provide power to the clock generation phase-locked loop. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered using a circuit similar to the one shown in Figure 15. The circuit should be placed as close as possible to the AV_{DD} pin to ensure it filters out as much noise as possible. The referenced ferrite bead, FB, shown in Figure 14 should supply an impedance of approximately 30 ohms in the 100 MHz region.

Figure 15. PLL Power Supply Filter Circuit



7.3 Decoupling Recommendations

Due to the PowerPC 750CX's feature large address and data buses, and high operating frequencies, the PowerPC 750CX can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the PowerPC 750CX system, and the PowerPC 750CX itself requires a clean, tightly regulated source of power.

Therefore, it is strongly recommended that the system designer place at least one decoupling capacitor with a low ESR (effective series resistance) rating at each V_{DD} and OV_{DD} pin of the PowerPC 750CX. It is also recommended that these decoupling capacitors receive their power from separate V_{DD} , OV_{DD} , and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should range in value from 220pF to 10uF to provide both high and low-frequency filtering, and should be placed as close as possible to their associated V_{DD} or OV_{DD} pins. Suggested values for the V_{DD} pins: 220pF (ceramic X7R), 0.01uF(ceramic X7R), and 0.1uF(ceramic X7R). Suggested values for the OV_{DD} pins: 0.01uF(ceramic X7R), 0.1uF(ceramic X7R), and 10uF (tantalum). Only SMT (surface-mount technology) capacitors should be used to minimize lead inductance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance.

Suggested bulk capacitors: 100uF(AVX TPS tantalum) or 330uF(AVX TPS tantalum).

7.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD} . Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

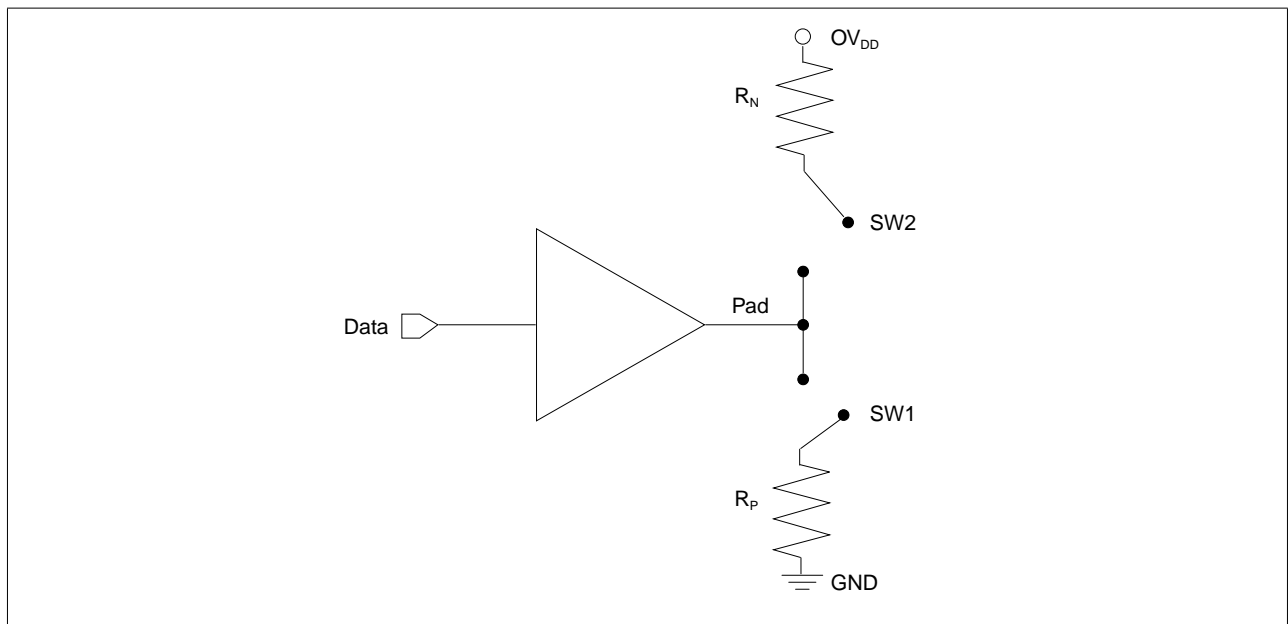
Power and ground connections must be made to all external V_{DD} , OV_{DD} , and GND pins of the PowerPC 750CX.

7.5 Output Buffer DC Impedance

The PowerPC 750CX 60X drivers were characterized over various process, voltage, and temperature conditions. To measure Z_0 , an external resistor is connected to the chip pad, either to OV_{DD} or GND. Then the value of the resistor is varied until the pad voltage is $OV_{DD}/2$; see Figure 16 below.

The output impedance is actually the average of two resistances: the resistance of the pull-up and the resistance of pull-down devices. When Data is held low, SW1 is closed (SW2 is open), and R_N is trimmed until $\text{Pad} = OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When Data is held high, SW2 is closed (SW1 is open), and R_P is trimmed until $\text{Pad} = OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. With a properly designed driver R_P and R_N are close to each other in value, then $Z_0 = (R_P + R_N)/2$.

Figure 16. Driver Impedance Measurement



The following table summarizes the impedance a board designer would design to for a typical process.

Table 15: Driver Impedance Characteristics

| Process | 60X Impedance (Ω) | V_{DD}, OV_{DD} (V) | Temperature (C) |
|---------|----------------------------|-----------------------|-----------------|
| Worst | 65 | 1.70 | 105 |
| Typical | 50 | 1.8 | 65 |
| Best | 40 | 1.90 | 0 |
| Worst | 65 | 2.38 | 105 |
| Typical | 50 | 2.5 | 65 |
| Best | 40 | 2.62 | 0 |

7.5.1 Input-Output Usage

Table 16 provides details on the input-output usage of the PowerPC 750CX RISC Microprocessor signals. The column titled “Usage Group” refers to the general functional category of the signal.

In the PowerPC 750CX RISC Microprocessor, certain input-output signals have pullups and pulldowns, which may or may not be enabled. The column titled “I/O with Internal Resistors” defines which signals have these pullups or pulldowns, and their active or inactive state.

The column titled “Level Protect” defines which signals have the designated function added to their I/O cell. Refer to Section 7.9.1 “Level Protection,” on page 38 for more information.

Table 16: Input-Output Usage

| PowerPC 750CX Signal Name | Active Level | Input/Output | Usage Group | I/O with Internal Resistors | Level Protect | Required External Resistor | Comments |
|--|--------------|--------------|---------------------|-----------------------------|---------------|----------------------------|--------------------------------------|
| A0-31 | N/A | BIDI | Address Bus | | Keeper | | See Note 1 |
| $\overline{\text{AACK}}$ | Low | IN | Address Termination | | Keeper | | Has to be actively driven |
| $\overline{\text{ARTRY}}$ | Low | BIDI | Address Termination | | Keeper | Resistor by design | Needs pullup DD2.0 also |
| $\overline{\text{BG}}$ | Low | IN | Address Arbitration | | Keeper | | Active driver or pulldown |
| $\overline{\text{BR}}$ | Low | OUT | Address Arbitration | | Keeper | | Chip actively drives |
| BVSEL | N/A | IN | I/O Level | | Keeper | 5K DD1.0, 2.0, 2.1, 2.2 | Sel high or low as design |
| $\overline{\text{CI}}$ | Low | OUT | Transfer Attributes | | Keeper | | See Note 1 |
| $\overline{\text{CKSTP_IN}}$ | Low | IN | Interrupt/Resets | | Keeper | | Has to be actively driven |
| $\overline{\text{CKSTP_OUT}}$ | Low | OUT | Interrupt/Resets | | Keeper | | No requirement |
| $\overline{\text{DBG}}$ | Low | IN | Data Arbitration | | Keeper | | Active driver or tie low |
| DH0-31 | N/A | BIDI | Data Bus | | Keeper | | See Note 1 |
| DL0-31 | N/A | BIDI | Data Bus | | Keeper | | See Note 1 |
| GBL | Low | BIDI | Transfer Attributes | | Keeper | | See Note 1 |
| $\overline{\text{HRESET}}$ | Low | IN | Interrupt/Resets | | Keeper | | Active driver and see Note 2. |
| $\overline{\text{INT}}$ | Low | IN | Interrupt/Resets | | Keeper | | Active driver or pullup |
| L1_TSTCLK | N/A | IN | LSSD | Not enabled | | 5K DD1.0, 2.0, 2.1, 2.2 | Pullup required |
| L2_TSTCLK/ $\overline{\text{DBWO}}$ | Low | IN | LSSD | Not enabled | | 5K DD1.0, 2.0, 2.1, 2.2 | Pullup required |
| $\overline{\text{LSSD_MODE}}$ | Low | IN | LSSD | Not enabled | | 5K DD1.0, 2.0, 2.1, 2.2 | Pullup required |
| MCP | Low | IN | Interrupt/Resets | | Keeper | | Active driver or pullup |
| PLL_CFG (0-3) | N/A | IN | Clock Control | | Keeper | As required | Pullup/pulldown, as required |
| $\overline{\text{QACK}}$ | Low | IN | Status/Control | | Keeper | | Has to be actively driven |
| $\overline{\text{QREQ}}$ | Low | OUT | Status/Control | | Keeper | | Chip actively drives |
| $\overline{\text{SRESET}}$ | Low | IN | Interrupt/Resets | | Keeper | | Active driver or pullup, see Note 2. |

Note:

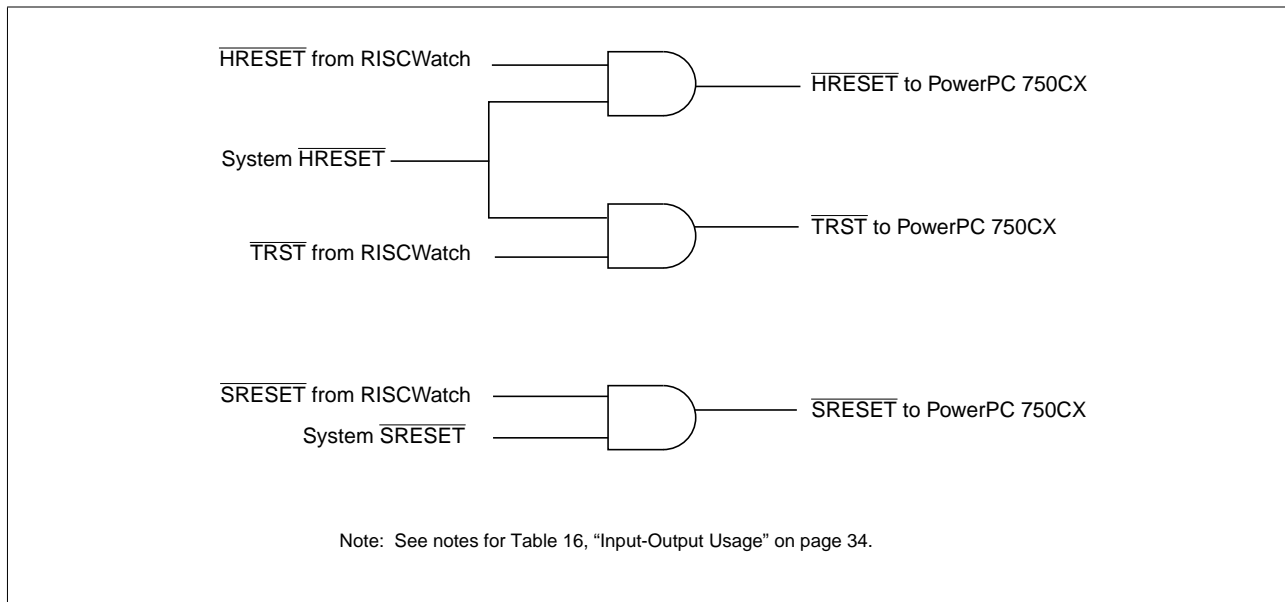
1. Depends on the system design
2. HRESET, SRESET, and TRST are signals used for ESP and RISCWatch to enable proper operation of the debuggers. Logical AND gates should be placed between these signals and PowerPC 750CX RISC Microprocessor. (Refer to Figure 17 on page 36.)

Table 16: Input-Output Usage (cont.)

| PowerPC 750CX Signal Name | Active Level | Input/ Output | Usage Group | I/O with Internal Resistors | Level Protect | Required External Resistor | Comments |
|---------------------------|--------------|---------------|---------------------|-----------------------------|------------------|----------------------------|---|
| SYSCLK | Low | IN | Clock Control | | Keeper | No resistor by design | Active driver |
| \overline{TA} | Low | IN | Data Termination | | Keeper | | Active driver |
| \overline{TBST} | Low | BIDI | Transfer Attributes | | Keeper | | See Note 1 |
| TCK | High | IN | JTAG | Not enabled | | Ext. pulldown | |
| TDI | High | IN | JTAG | Enabled high | Internal-Enabled | | 50 μ a@2.5V, 25 μ a@1.8V is the pullup current for the internal resistor. |
| TDO | High | OUT | JTAG | | Keeper | | |
| \overline{TEA} | Low | IN | Data Termination | | Keeper | | Active driver or pullup |
| TMS | High | IN | JTAG | Enabled high | Internal-Enabled | | 50 μ a@2.5V, 25 μ a@1.8V is the pullup current for the internal resistor. |
| \overline{TRST} | Low | IN | JTAG | Enabled high | Internal-Enabled | | See Note 2 50 μ a@2.5V, 25 μ a@1.8V is the pullup current for the internal resistor. |
| \overline{TS} | Low | BIDI | Address Start | | Keeper | 5K DD1.0, 2.0, 2.1, 2.2 | Pullup required |
| TSIZ0_TSIZ2 | N/A | OUT | Transfer Attributes | | Keeper | | See Note 1 |
| TT0-4 | N/A | IN | Transfer Attributes | | Keeper | | See Note 1 |
| \overline{WT} | Low | OUT | Transfer Attributes | | Keeper | | See Note 1 |

Note:

1. Depends on the system design
2. \overline{HRESET} , \overline{SRESET} , and \overline{TRST} are signals used for ESP and RISCWatch to enable proper operation of the debuggers. Logical AND gates should be placed between these signals and PowerPC 750CX RISC Microprocessor. (Refer to Figure 17 on page 36.)

Figure 17. IBM RISCWatch™ JTAG to $\overline{\text{HRESET}}$, $\overline{\text{TRST}}$, and $\overline{\text{SRESET}}$ Signal Connector


7.6 Thermal Management Information

This section provides thermal management information for the PBGA package for air cooled applications. Proper thermal control design is primarily dependent upon the system-level design and air flow.

7.7 Heat Sink Considerations

The PowerPC 750CX RISC Microprocessor package will support a maximum normal load of 2.2 kilograms. This load includes the heat sink and any forces used to position or fasten the heat sink.

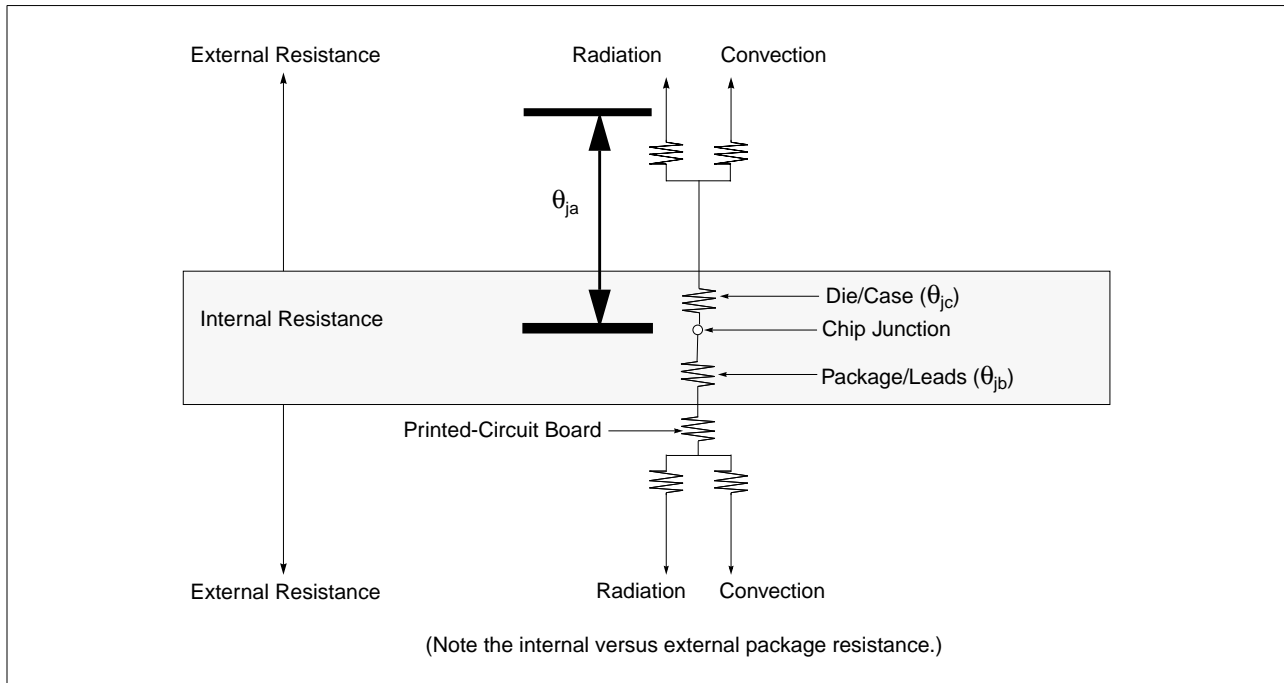
7.8 Internal Package Conduction Resistance

For the PBGA, described in Table 3 on page 12, the primary intrinsic conduction thermal resistance paths are as follows.

- Die junction-to-case thermal resistance
- Die junction-to-lead thermal resistance
- Die junction-to-ambient thermal resistance

Figure 18 depicts the primary heat transfer path for this package.

Figure 18. PBGA Package with Thermal Model



7.9 Operational and Design Considerations

7.9.1 Level Protection

A level protection feature is included in the PowerPC 750CX RISC Microprocessor in releases DD2.0 and later. The level protection feature is available only in the 1.8V bus mode. This feature prevents ambiguous floating reference voltages by pulling the respective signal line to the last valid or nearest valid state.

For example, if the I/O voltage level is closer to OV_{DD} , the circuit pulls the I/O level to OV_{DD} ; if the I/O level is closer to GND, the I/O level is pulled low. This self-latching circuitry “keeps” the floating inputs defined and avoids meta-stability. In Table 16, these signals are defined as “keeper” in the “Level Protect” column.

The level protect circuitry provides no additional leakage current to the signal I/O; however, some amount of current must be applied to the “keeper” node to overcome the level protection latch. This current is process dependent, but in no case is the current required over 100 μ A.

This feature allows the system designer to limit the number of resistors in the design and optimize placement and reduce costs.

7.9.2 64 or 32-Bit Data Bus Mode

Typical operation is considered to be in 64-bit Data Bus mode. Mode setting is determined by the state of the mode signal (\overline{QACK}) at the transition of \overline{HRESET} from its active to inactive state (low to high). If \overline{QACK} is **low** when \overline{HRESET} transitions from active to inactive, 64-bit mode is selected. If \overline{QACK} is **high** when \overline{HRESET} transitions from active to inactive, 32-bit mode is selected.

7.9.3 1.8V and 2.5V I/O Signal Support

Selection between 1.8V and 2.5V I/O is accomplished using the BVSEL pin. If BVSEL is set low then the 1.8V mode is enabled. If BVSEL is set high, then the 2.5V mode is enabled. Due to bus timings restrictions, only uniprocessor implementations are recommended. No multiprocessor support is advised.

7.9.4 $\overline{DBWO}/L2_TSTCLK$

One pin has two functions: \overline{DBWO} and L2_TSTCLK dependent upon the $\overline{LSSD_MODE}$ pin. When the $\overline{LSSD_MODE}$ pin is low, the $\overline{DBWO}/L2_TSTCLK$ pin is set to L2_TSTCLK function which is used during the manufacturing process for testing.

When the $\overline{LSSD_MODE}$ pin is pulled to the high state, the $\overline{DBWO}/L2_TSTCLK$ pin is set to \overline{DBWO} which is identical to those descriptions given in earlier versions of the PowerPC 750CX RISC Microprocessor's User's Manuals.

7.9.5 PowerPC 750CX Revision Level Migration

The following table summarizes the design changes for the respective PowerPC 750CX design revision levels.

Table 17: Summary of Design Migration

| | DD1.0 | DD2.0 | DD2.1 | DD2.2 |
|-----------------------|----------------------------------|--|--|--|
| PVR | 0x00080100 | 0x00080100 | 0x00082201 | 0x00082202 |
| L1 Data Bus Width | 64-Bits | 256-Bits | 256-Bits | 256-Bits |
| DPM | Enabled | Disabled | Disabled | Disabled |
| Test Pin | $\overline{CHKSTP_OUT}$ removed | CLKOUT/ $\overline{CHKSTP_OUT}$ share a pin | CLKOUT/ $\overline{CHKSTP_OUT}$ share a pin | CLKOUT/ $\overline{CHKSTP_OUT}$ share a pin |
| 32-Bit Mode | Not available | Available | Available | Available |
| Floating Bus | Pull-ups required | No pull-ups | No pull-ups | No pull-ups |
| \overline{DBWO} Pin | Absent | Absent | Present | Present |

8.0 Ordering Information

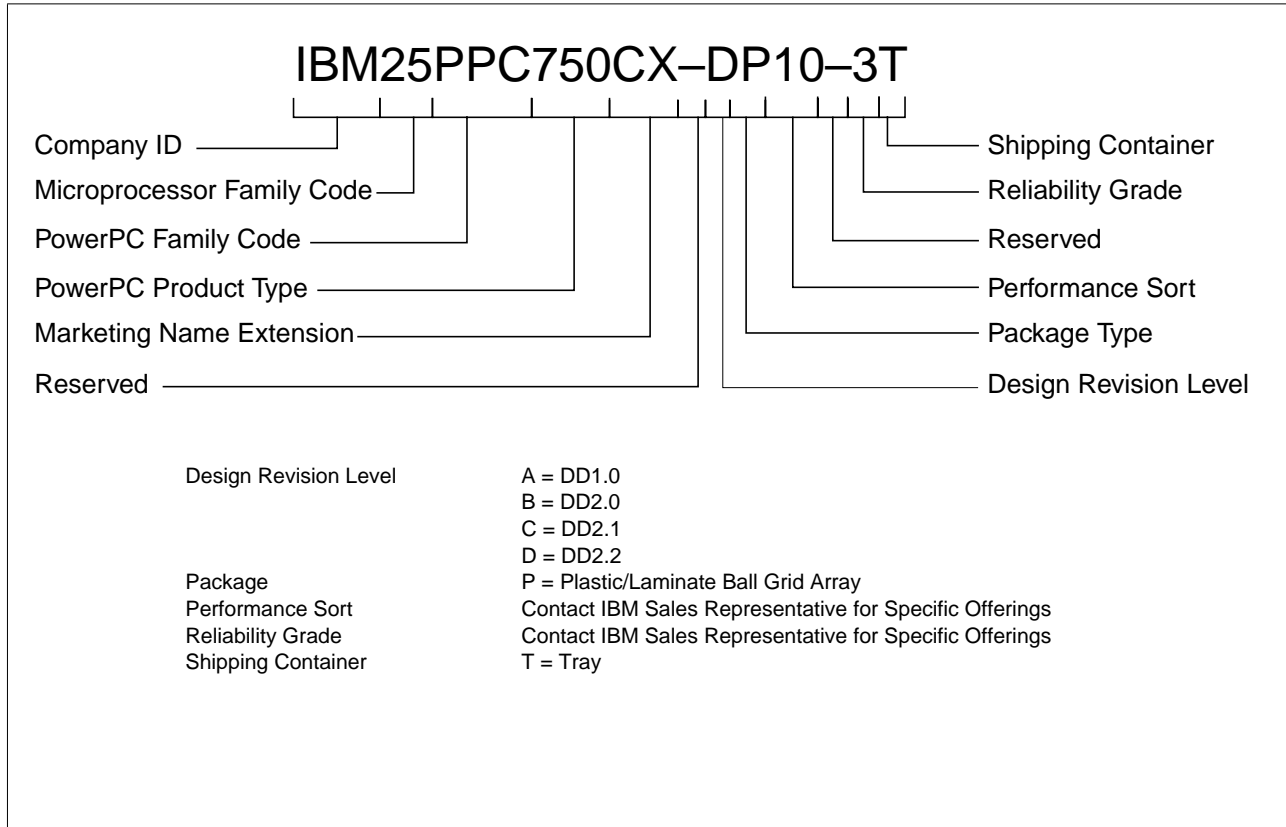
This section provides the part numbering nomenclature for the PowerPC 750CX. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local IBM sales office.

In addition to the processor frequency and bus ratio, the part numbering scheme also consists of a part modifier. The part modifier allows for the availability of future enhanced parts (i.e., lower voltage, lower power, higher performance, etc.).

Each part number also contains a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

Figure 19 provides the IBM part numbering nomenclature for the PowerPC 750CX.

Figure 19. IBM Part Number Key



9.0 Processor Version Register (PVR)

The PowerPC 750CX RISC Microprocessor has the following PVR values for the respective design revision levels.

Table 18: Process Version Register (PVR)

| Design Revision Level | PVR |
|-----------------------|----------|
| DD1.0 | 00080100 |
| DD2.0 | 00080100 |
| DD2.1 | 00082201 |
| DD2.2 | 00082202 |

10.0 Document History

Table 19: Document History

| Date | Version | Page | Description |
|----------|---------|------|--|
| 3/31/00 | 1.0 | | Initial Release. |
| 4/6/00 | | | First Revision. |
| 4/10/00 | | | Added Table 13. |
| 4/25/00 | | | Added Note 5, Table 1. |
| 11/13/00 | 1.1 | 9 | Minor edits to Features section. |
| | | 13 | Updated Table 4, "DC Electrical Specifications," on page 13 (Output High Voltage) |
| | | 14 | Updated Table 5, "Power Consumption" (Full-on Mode values). |
| | | 17 | Figure 4, "Mode Select Input Timing Diagram," V_{IH} changed to 1.24V. Edited corresponding Table 8, note #1. |
| | | 21 | Edited table note #1 in Table 8, "TRST Timing Diagram". |
| | | 22 | Heading title changed (Section 6.0 on Page 22) and updated mechanical drawing dimensions. |
| | | 23 | Updated Figure 11, "Pinout of the 256 PBGA Package as Viewed from Solder Ball side." |
| | | 24 | Updated Figure 12, "Side Profile View of PBGA." |
| | | 24 | Updated Figure 13, "Side Profile View Showing Exposed Cavity." |
| | | 25 | Corrections to Figure 14, "PowerPC 750CX Microprocessor Ball Placement." |
| | | 34 | Updated Table 16, "Input-Output Usage" to include DD2.2. |
| | | 35 | Changed QREG to QREQ. |
| | | 38 | Edited Section 7.9.1, "Level Protection," on page 38 (redundant with Section 7.5.1, "Input-Output Usage," on page 33). |
| | | 39 | Edited Section 7.9.4, "DBWO/L2_TSTCLK". |
| | | 39 | Added Section 7.9.5, "PowerPC 750CX Revision Level Migration". |
| | | 40 | Updated Figure 19, "IBM Part Number Key." |
| 6/20/01 | 1.2 | 1 | Version Update. |
| | | 8 | 250K L2 cache line around removed. |
| | | 12 | Note added 1. |
| | | 14 | Table updated. 433MHz column removed. |
| | | 27 | Removed note from Table 11. |
| | | 29 | Called out AVDD in Table 13. |
| | | 30 | Table 14 updated for 500MHz max. |
| | | 38 | Added a bus timing note in section 7.9.3. |
| | | 40 | Updated part number decoder. Specifics removed, to be put in supplement. |
| | | 44 | Blank removed. |



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IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY
12533-6531

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