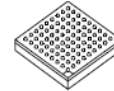


P1011

P1011 QorIQ Integrated Processor Hardware Specifications



The following list provides an overview of the feature set:

- A high-performance 32-bit core, built on Power Architecture® technology:
 - 36-bit physical addressing
 - Double-precision floating-point support
 - 32 Kbyte L1 instruction cache and 32 Kbyte L1 data cache for each core
 - 533 MHz to 800 MHz clock frequency
 - 256 Kbyte L2 cache with ECC. Also configurable as SRAM and stashing memory.
 - Three 10/100/1000 Mbps enhanced three-speed Ethernet controllers (eTSECs)
 - TCP/IP acceleration, quality of service, and classification capabilities
 - IEEE® 1588 support
 - Lossless flow control
 - MII, RMII, RGMII, SGMII
 - High-speed interfaces supporting various multiplexing options:
 - Four SerDes upto 2.5 GHz/lane multiplexed across controllers
 - Two PCI Express interfaces
 - Two SGMII interfaces
 - High-Speed USB controller (USB 2.0)
 - Host and device support
 - Enhanced host controller interface (EHCI)
 - ULPI interface to PHY
 - Enhanced secure digital host controller (SD/MMC)
 - Enhanced Serial peripheral interface (eSPI)
 - Integrated security engine
 - Protocol support includes ARC4, 3DES, AES, RSA/ECC, RNG, single-pass SSL/TLS
 - XOR acceleration
 - 32-bit DDR2/DDR3 SDRAM memory controller with ECC support
 - Programmable interrupt controller (PIC) compliant with OpenPIC standard
- One four-channel DMA controller
 - Two I²C controllers, DUART, timers
 - Enhanced local bus controller (eLBC)
 - TDM
 - 16 general-purpose I/O signals
 - Operating junction temperature (T_j) range: 0–125°C and –40°C to 125°C (industrial specification)
 - 31 × 31 mm 689-pin WB-TePBGA II (wire bond temperature-enhanced plastic BGA)

Table of Contents

| | | | | | |
|------|--|----|------|--|-----|
| 1 | Pin Assignments and Reset States | 4 | 2.13 | Enhanced Local Bus | 75 |
| 1.1 | Ball Layout Diagrams | 4 | 2.14 | Enhanced Secure Digital Host Controller (eSDHC) | 79 |
| 1.2 | Pinout Assignments | 9 | 2.15 | Programmable Interrupt Controller (PIC) Specifications | 81 |
| 2 | Electrical Characteristics | 33 | 2.16 | JTAG | 82 |
| 2.1 | Overall DC Electrical Characteristics | 33 | 2.17 | I2C | 84 |
| 2.2 | Power Sequencing | 37 | 2.18 | GPIO | 87 |
| 2.3 | Power Down Requirements | 37 | 2.19 | TDM | 89 |
| 2.4 | RESET Initialization | 37 | 2.20 | High-Speed Serial Interfaces (HSSI) | 91 |
| 2.5 | Power-on Ramp Rate | 38 | 2.21 | PCI Express | 97 |
| 2.6 | Power Characteristics | 39 | 3 | Thermal | 102 |
| 2.7 | Input Clocks | 41 | 3.1 | Thermal Characteristics | 102 |
| 2.8 | DDR2 and DDR3 SDRAM | 44 | 3.2 | Temperature Diode | 102 |
| 2.9 | eSPI | 53 | 4 | Package Information | 102 |
| 2.10 | DUART | 55 | 4.1 | Package Parameters for the P1011 WB-TePBGA II | 102 |
| 2.11 | Ethernet: Enhanced Three-Speed Ethernet (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII Electrical Characteristics | 56 | 4.2 | Ordering Information | 105 |
| 2.12 | USB | 72 | 5 | Product Documentation | 105 |
| | | | 6 | Revision History | 106 |

This figure shows the major functional units within the P1011.

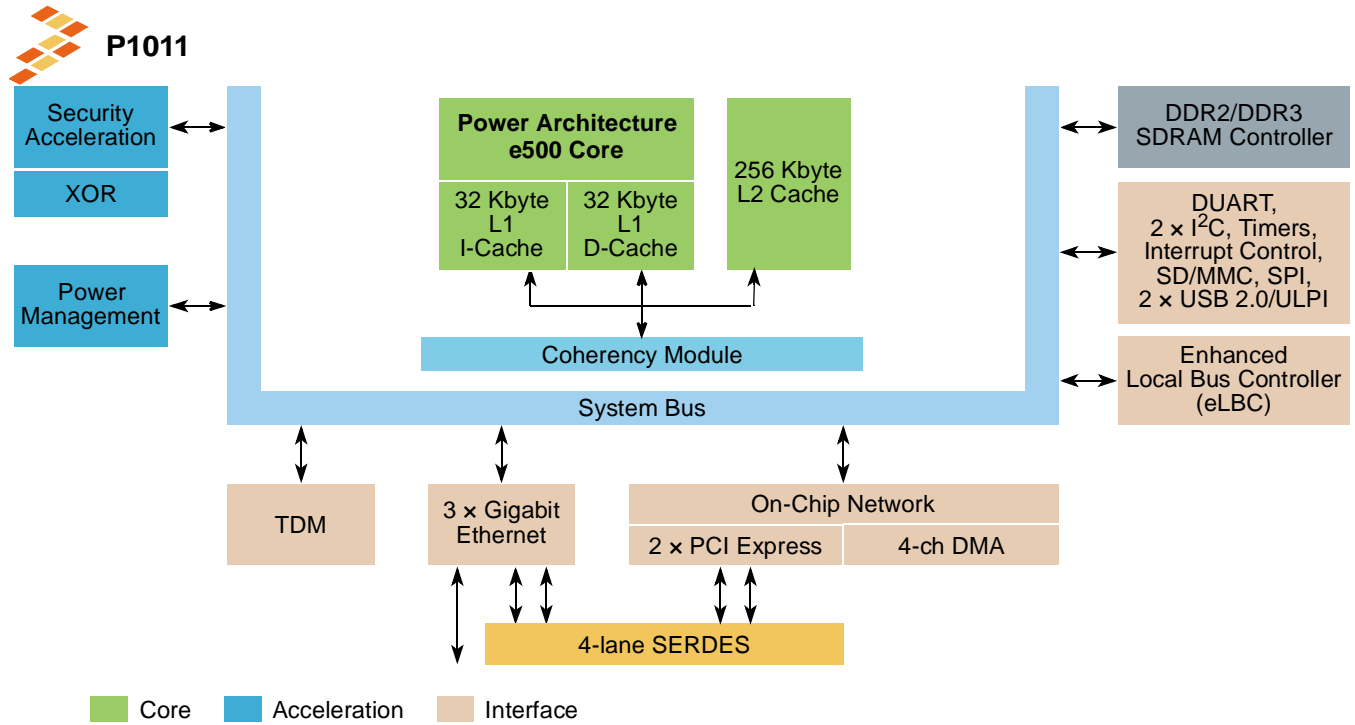


Figure 1. P1011 Block Diagram

1 Pin Assignments and Reset States

1.1 Ball Layout Diagrams

The following figures show the top view of the 689-pin BGA ball map diagram and detailed quadrant views.

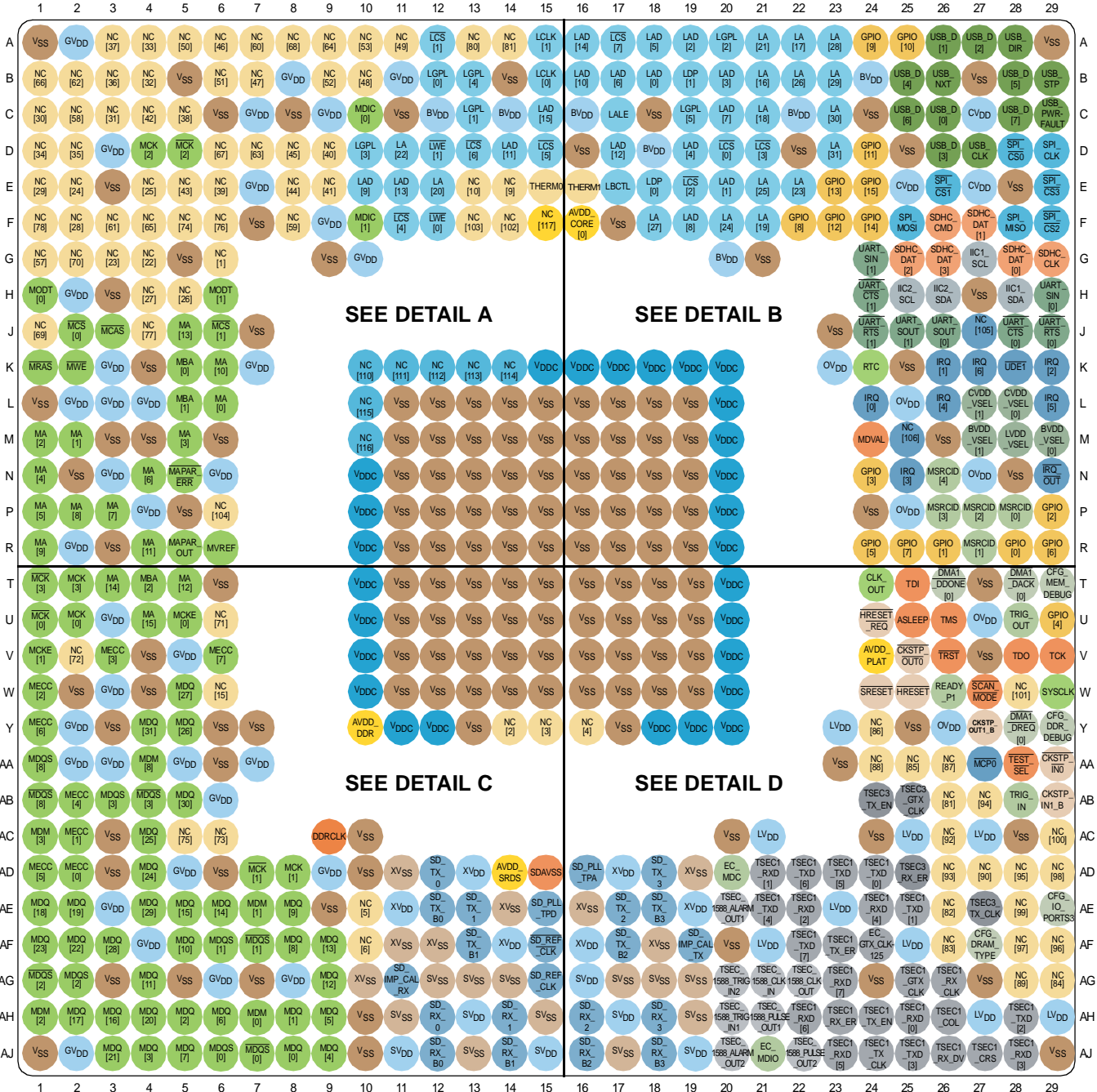
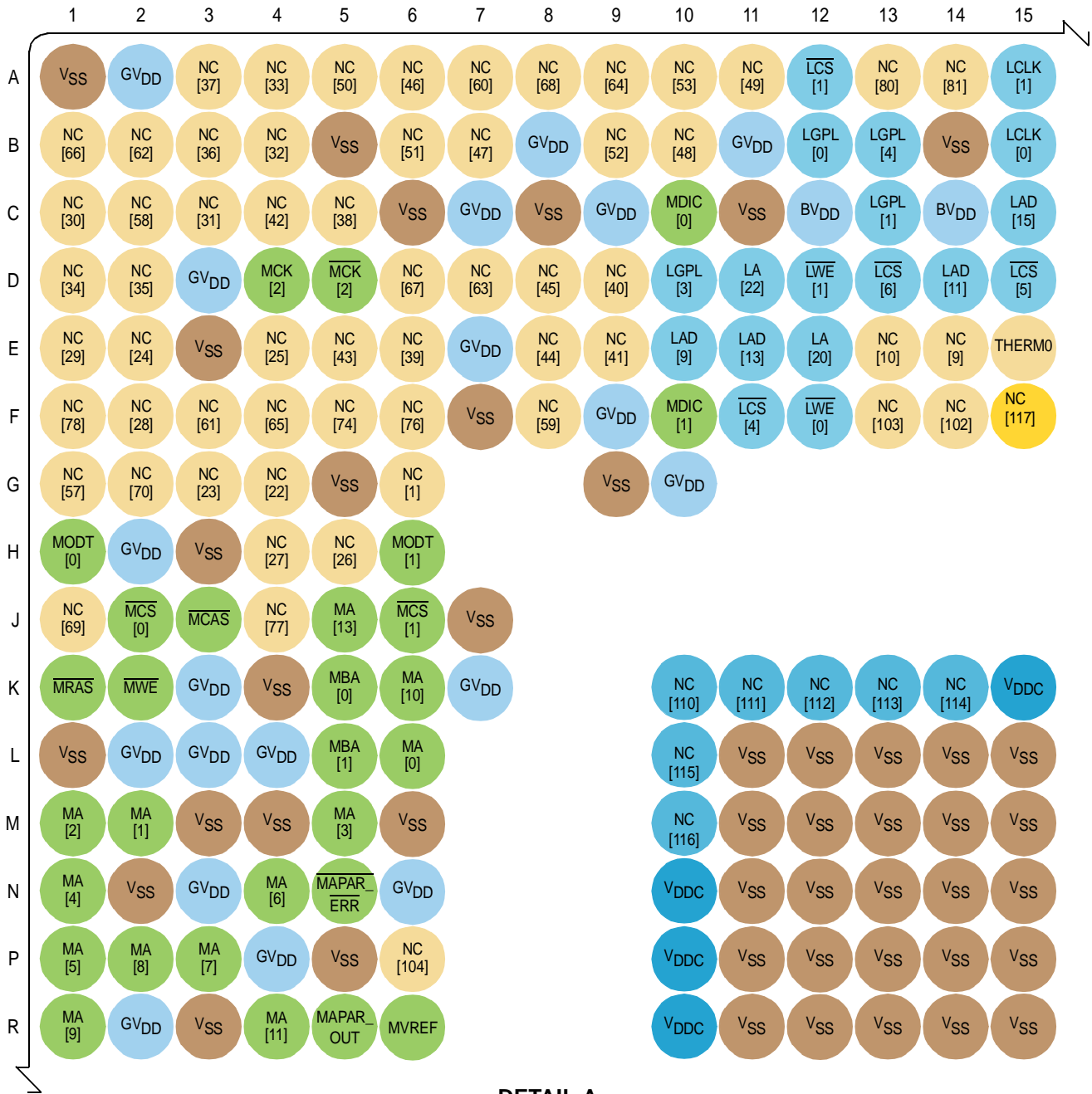


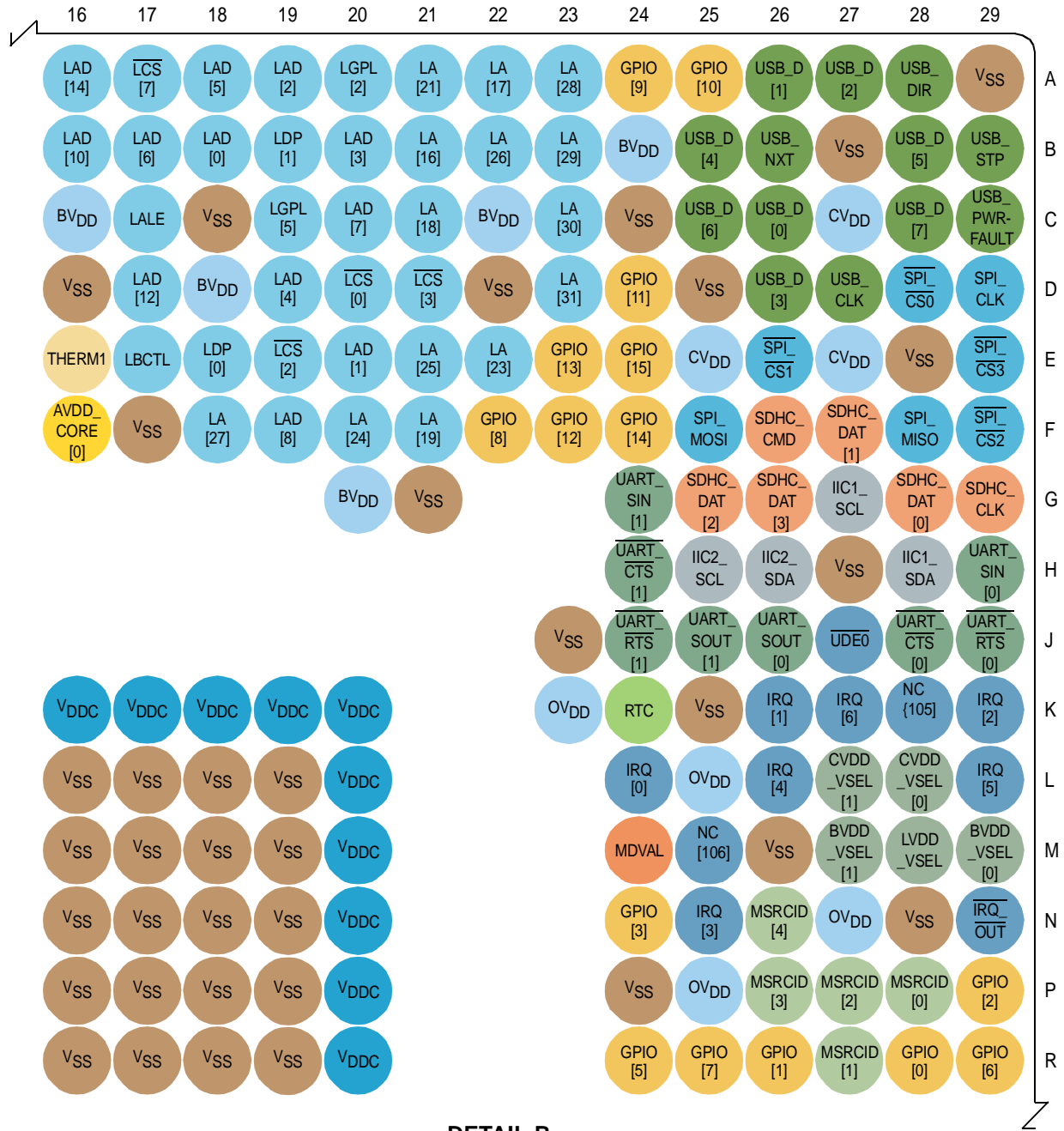
Figure 2. P1011 Top View Ball map



DETAIL A

Figure 3. P1011 Detail A Ball map

Pin Assignments and Reset States



DETAIL B

Figure 4. P1011 Detail B Ball map

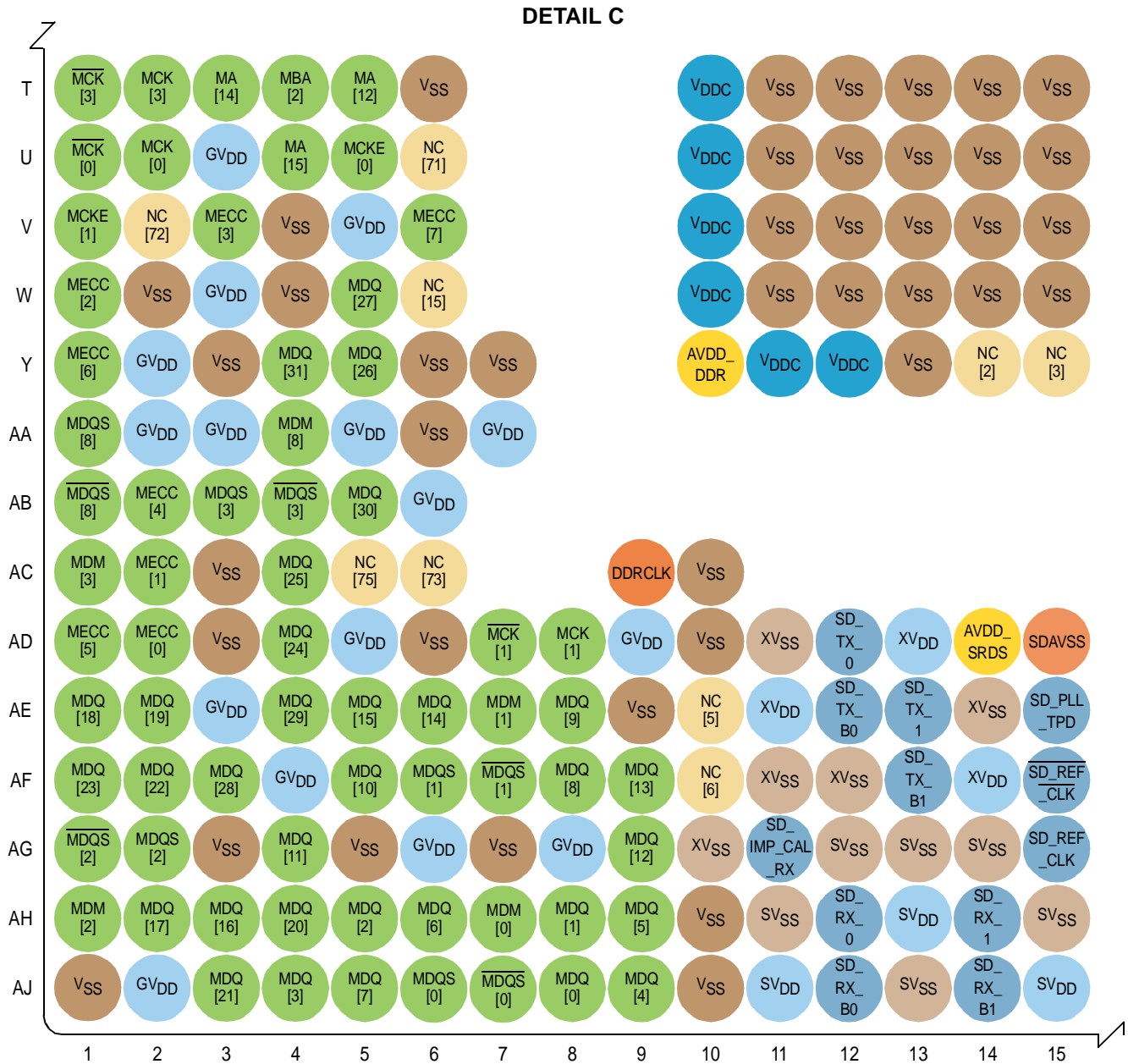


Figure 5. P1011 Detail C Ball map

DETAIL D

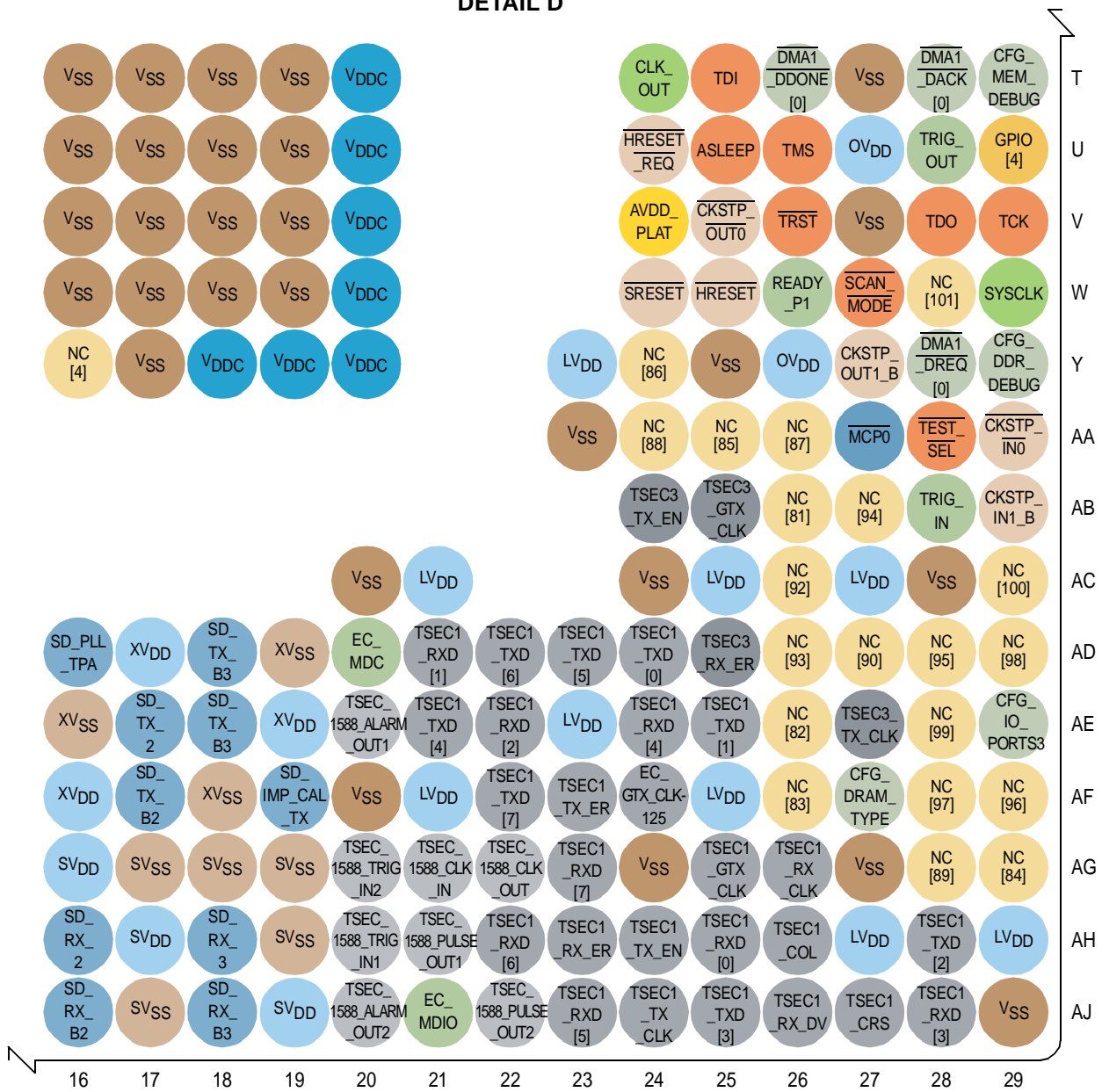


Figure 6. P1011 Detail D Ball map

1.2 Pinout Assignments

This table provides the pinout listing.

Table 1. P1011 Pinout Listing

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|-----------------------------------|--------------------|----------|------------------|------|
| DDR SDRAM Memory Interface | | | | |
| MDQ00 | AJ8 | I/O | GV _{DD} | — |
| MDQ01 | AH8 | I/O | GV _{DD} | — |
| MDQ02 | AH5 | I/O | GV _{DD} | — |
| MDQ03 | AJ4 | I/O | GV _{DD} | — |
| MDQ04 | AJ9 | I/O | GV _{DD} | — |
| MDQ05 | AH9 | I/O | GV _{DD} | — |
| MDQ06 | AH6 | I/O | GV _{DD} | — |
| MDQ07 | AJ5 | I/O | GV _{DD} | — |
| MDQ08 | AF8 | I/O | GV _{DD} | — |
| MDQ09 | AE8 | I/O | GV _{DD} | — |
| MDQ10 | AF5 | I/O | GV _{DD} | — |
| MDQ11 | AG4 | I/O | GV _{DD} | — |
| MDQ12 | AG9 | I/O | GV _{DD} | — |
| MDQ13 | AF9 | I/O | GV _{DD} | — |
| MDQ14 | AE6 | I/O | GV _{DD} | — |
| MDQ15 | AE5 | I/O | GV _{DD} | — |
| MDQ16 | AH3 | I/O | GV _{DD} | — |
| MDQ17 | AH2 | I/O | GV _{DD} | — |
| MDQ18 | AE1 | I/O | GV _{DD} | — |
| MDQ19 | AE2 | I/O | GV _{DD} | — |
| MDQ20 | AH4 | I/O | GV _{DD} | — |
| MDQ21 | AJ3 | I/O | GV _{DD} | — |
| MDQ22 | AF2 | I/O | GV _{DD} | — |
| MDQ23 | AF1 | I/O | GV _{DD} | — |
| MDQ24 | AD4 | I/O | GV _{DD} | — |
| MDQ25 | AC4 | I/O | GV _{DD} | — |
| MDQ26 | Y5 | I/O | GV _{DD} | — |
| MDQ27 | W5 | I/O | GV _{DD} | — |
| MDQ28 | AF3 | I/O | GV _{DD} | — |

Table 1. P1011 Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|--------|--------------------|----------|------------------|------|
| MDQ29 | AE4 | I/O | GV _{DD} | — |
| MDQ30 | AB5 | I/O | GV _{DD} | — |
| MDQ31 | Y4 | I/O | GV _{DD} | — |
| NC22 | G4 | NC | — | — |
| NC23 | G3 | NC | — | — |
| NC24 | E2 | NC | — | — |
| NC25 | E4 | NC | — | — |
| NC26 | H5 | NC | — | — |
| NC27 | H4 | NC | — | — |
| NC28 | F2 | NC | — | — |
| NC29 | E1 | NC | — | — |
| NC30 | C1 | NC | — | — |
| NC31 | C3 | NC | — | — |
| NC32 | B4 | NC | — | — |
| NC33 | A4 | NC | — | — |
| NC34 | D1 | NC | — | — |
| NC35 | D2 | NC | — | — |
| NC36 | B3 | NC | — | — |
| NC37 | A3 | NC | — | — |
| NC38 | C5 | NC | — | — |
| NC39 | E6 | NC | — | — |
| NC40 | D9 | NC | — | — |
| NC41 | E9 | NC | — | — |
| NC42 | C4 | NC | — | — |
| NC43 | E5 | NC | — | — |
| NC44 | E8 | NC | — | — |
| NC45 | D8 | NC | — | — |
| NC46 | A6 | NC | — | — |
| NC47 | B7 | NC | — | — |
| NC48 | B10 | NC | — | — |
| NC49 | A11 | NC | — | — |
| NC50 | A5 | NC | — | — |
| NC51 | B6 | NC | — | — |

Table 1. P1011 Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|-------------|--------------------|----------|------------------|------|
| NC52 | B9 | NC | — | — |
| NC53 | A10 | NC | — | — |
| MECC00 | AD2 | I/O | GV _{DD} | — |
| MECC01 | AC2 | I/O | GV _{DD} | — |
| MECC02 | W1 | I/O | GV _{DD} | — |
| MECC03 | V3 | I/O | GV _{DD} | — |
| MECC04 | AB2 | I/O | GV _{DD} | — |
| MECC05 | AD1 | I/O | GV _{DD} | — |
| MECC06 | Y1 | I/O | GV _{DD} | — |
| MECC07 | V6 | I/O | GV _{DD} | — |
| MAPAR_ERR_B | N5 | I | GV _{DD} | — |
| MAPAR_OUT | R5 | O | GV _{DD} | — |
| MDM00 | AH7 | O | GV _{DD} | — |
| MDM01 | AE7 | O | GV _{DD} | — |
| MDM02 | AH1 | O | GV _{DD} | — |
| MDM03 | AC1 | O | GV _{DD} | — |
| NC57 | G1 | NC | — | — |
| NC58 | C2 | NC | — | — |
| NC59 | F8 | NC | — | — |
| NC60 | A7 | NC | — | — |
| MDM08 | AA4 | O | GV _{DD} | — |
| MDQS00 | AJ6 | I/O | GV _{DD} | — |
| MDQS01 | AF6 | I/O | GV _{DD} | — |
| MDQS02 | AG2 | I/O | GV _{DD} | — |
| MDQS03 | AB3 | I/O | GV _{DD} | — |
| NC61 | F3 | NC | — | — |
| NC62 | B2 | NC | — | — |
| NC63 | D7 | NC | — | — |
| NC64 | A9 | NC | — | — |
| MDQS08 | AA1 | I/O | GV _{DD} | — |
| MDQS_B00 | AJ7 | I/O | GV _{DD} | — |
| MDQS_B01 | AF7 | I/O | GV _{DD} | — |
| MDQS_B02 | AG1 | I/O | GV _{DD} | — |

Table 1. P1011 Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|----------|--------------------|----------|------------------|------|
| MDQS_B03 | AB4 | I/O | GV _{DD} | — |
| NC65 | F4 | NC | — | — |
| NC66 | B1 | NC | — | — |
| NC67 | D6 | NC | — | — |
| NC68 | A8 | NC | — | — |
| MDQS_B08 | AB1 | I/O | GV _{DD} | — |
| MBA00 | K5 | O | GV _{DD} | — |
| MBA01 | L5 | O | GV _{DD} | — |
| MBA02 | T4 | O | GV _{DD} | — |
| MA00 | L6 | O | GV _{DD} | — |
| MA01 | M2 | O | GV _{DD} | — |
| MA02 | M1 | O | GV _{DD} | — |
| MA03 | M5 | O | GV _{DD} | — |
| MA04 | N1 | O | GV _{DD} | — |
| MA05 | P1 | O | GV _{DD} | — |
| MA06 | N4 | O | GV _{DD} | — |
| MA07 | P3 | O | GV _{DD} | — |
| MA08 | P2 | O | GV _{DD} | — |
| MA09 | R1 | O | GV _{DD} | — |
| MA10 | K6 | O | GV _{DD} | — |
| MA11 | R4 | O | GV _{DD} | — |
| MA12 | T5 | O | GV _{DD} | — |
| MA13 | J5 | O | GV _{DD} | — |
| MA14 | T3 | O | GV _{DD} | — |
| MA15 | U4 | O | GV _{DD} | — |
| MWE_B | K2 | O | GV _{DD} | — |
| MRAS_B | K1 | O | GV _{DD} | — |
| MCAS_B | J3 | O | GV _{DD} | — |
| MCS_B00 | J2 | O | GV _{DD} | — |
| MCS_B01 | J6 | O | GV _{DD} | — |
| NC69 | J1 | NC | — | — |
| NC70 | G2 | NC | — | — |
| MCKE00 | U5 | O | GV _{DD} | 8 |

Table 1. P1011 Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---------------|--------------------|----------|------------------------|------|
| MCKE01 | V1 | O | GV _{DD} | 8 |
| NC71 | U6 | NC | — | — |
| NC72 | V2 | NC | — | — |
| MCK00 | U2 | O | GV _{DD} | — |
| MCK01 | AD8 | O | GV _{DD} | — |
| MCK02 | D4 | O | GV _{DD} | — |
| MCK03 | T2 | O | GV _{DD} | — |
| NC73 | AC6 | NC | — | — |
| NC74 | F5 | NC | — | — |
| MCK_B00 | U1 | O | GV _{DD} | — |
| MCK_B01 | AD7 | O | GV _{DD} | — |
| MCK_B02 | D5 | O | GV _{DD} | — |
| MCK_B03 | T1 | O | GV _{DD} | — |
| NC75 | AC5 | NC | — | — |
| NC76 | F6 | NC | — | — |
| MODT00 | H1 | O | GV _{DD} | — |
| MODT01 | H6 | O | GV _{DD} | — |
| NC77 | J4 | NC | — | — |
| NC78 | F1 | NC | — | — |
| MDIC00 | C10 | I/O | GV _{DD} | 14 |
| MDIC01 | F10 | I/O | GV _{DD} | 14 |
| SerDes | | | | |
| SD_TX_3 | AD18 | O | XV _{DD} _SRDS | — |
| SD_TX_2 | AE17 | O | XV _{DD} _SRDS | — |
| SD_TX_1 | AE13 | O | XV _{DD} _SRDS | — |
| SD_TX_0 | AD12 | O | XV _{DD} _SRDS | — |
| SD_TX_B3 | AE18 | O | XV _{DD} _SRDS | — |
| SD_TX_B2 | AF17 | O | XV _{DD} _SRDS | — |
| SD_TX_B1 | AF13 | O | XV _{DD} _SRDS | — |
| SD_TX_B0 | AE12 | O | XV _{DD} _SRDS | — |
| SD_RX_3 | AH18 | I | SV _{DD} _SRDS | — |
| SD_RX_2 | AH16 | I | SV _{DD} _SRDS | — |

Table 1. P1011 Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|--|--------------------|----------|------------------------|-------|
| SD_RX_1 | AH14 | I | SV _{DD} _SRDS | — |
| SD_RX_0 | AH12 | I | SV _{DD} _SRDS | — |
| SD_RX_B3 | AJ18 | I | SV _{DD} _SRDS | — |
| SD_RX_B2 | AJ16 | I | SV _{DD} _SRDS | — |
| SD_RX_B1 | AJ14 | I | SV _{DD} _SRDS | — |
| SD_RX_B0 | AJ12 | I | SV _{DD} _SRDS | — |
| SD_REF_CLK | AG15 | I | SV _{DD} _SRDS | — |
| SD_REF_CLK_B | AF15 | I | SV _{DD} _SRDS | — |
| SD_PLL_TPD | AE15 | O | XV _{DD} _SRDS | 10 |
| SD_IMP_CAL_RX | AG11 | I | XV _{DD} _SRDS | 23 |
| SD_IMP_CAL_TX | AF19 | I | XV _{DD} _SRDS | 23 |
| SD_PLL_TPA | AD16 | O | XV _{DD} _SRDS | 10 |
| Enhanced Local Bus Controller Interface | | | | |
| LAD00/USB2_D07 | B18 | I/O | BV _{DD} | 4, 19 |
| LAD01/USB2_D06 | E20 | I/O | BV _{DD} | 4, 19 |
| LAD02/USB2_D05 | A19 | I/O | BV _{DD} | 4, 19 |
| LAD03/USB2_D04 | B20 | I/O | BV _{DD} | 4, 19 |
| LAD04/USB2_D03 | D19 | I/O | BV _{DD} | 4, 19 |
| LAD05/USB2_D02 | A18 | I/O | BV _{DD} | 4, 19 |
| LAD06/USB2_D01 | B17 | I/O | BV _{DD} | 4, 19 |
| LAD07/USB2_D00 | C20 | I/O | BV _{DD} | 4, 19 |
| LAD08/USB2_NXT | F19 | I/O | BV _{DD} | 4, 19 |
| LAD09/USB2_DIR | E10 | I/O | BV _{DD} | 4, 19 |
| LAD10/USB2_STP | B16 | I/O | BV _{DD} | 4, 19 |
| LAD11/USB2_PWRFAULT | D14 | I/O | BV _{DD} | 4, 19 |
| LAD12/USB2_CLK | D17 | I/O | BV _{DD} | 4, 19 |
| LAD13/USB2_PCTL0 | E11 | I/O | BV _{DD} | 4, 19 |
| LAD14/USB2_PCTL1 | A16 | I/O | BV _{DD} | 4, 19 |
| LAD15 | C15 | I/O | BV _{DD} | 4, 19 |
| LDP00 | E18 | I/O | BV _{DD} | 7 |
| LDP01 | B19 | I/O | BV _{DD} | 7 |
| LA16 | B21 | I/O | BV _{DD} | 6 |

Table 1. P1011 Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---------|--------------------|----------|------------------|-------|
| LA17 | A22 | I/O | BV _{DD} | 6, 13 |
| LA18 | C21 | I/O | BV _{DD} | 4, 6 |
| LA19 | F21 | I/O | BV _{DD} | 4, 6 |
| LA20 | E12 | I/O | BV _{DD} | 4, 6 |
| LA21 | A21 | I/O | BV _{DD} | 4, 6 |
| LA22 | D11 | I/O | BV _{DD} | 4, 6 |
| LA23 | E22 | I/O | BV _{DD} | 4, 6 |
| LA24 | F20 | I/O | BV _{DD} | 4, 6 |
| LA25 | E21 | I/O | BV _{DD} | 4, 6 |
| LA26 | B22 | I/O | BV _{DD} | 4, 6 |
| LA27 | F18 | I/O | BV _{DD} | 6, 20 |
| LA28 | A23 | I/O | BV _{DD} | 6, 13 |
| LA29 | B23 | I/O | BV _{DD} | — |
| LA30 | C23 | I/O | BV _{DD} | — |
| LA31 | D23 | I/O | BV _{DD} | — |
| LCS_B00 | D20 | O | BV _{DD} | 7 |
| LCS_B01 | A12 | O | BV _{DD} | 7 |
| LCS_B02 | E19 | O | BV _{DD} | 7 |
| LCS_B03 | D21 | O | BV _{DD} | 7 |
| LCS_B04 | F11 | I/O | BV _{DD} | 7 |
| LCS_B05 | D15 | I/O | BV _{DD} | 7 |
| LCS_B06 | D13 | O | BV _{DD} | 7 |
| LCS_B07 | A17 | O | BV _{DD} | 7 |
| LWE_B00 | F12 | O | BV _{DD} | 6 |
| LWE_B01 | D12 | I/O | BV _{DD} | 5 |
| LBCTL | E17 | I/O | BV _{DD} | 5 |
| LALE | C17 | O | BV _{DD} | 5 |
| LGPL0 | B12 | I/O | BV _{DD} | |
| LGPL1 | C13 | I/O | BV _{DD} | |
| LGPL2 | A20 | O | BV _{DD} | 5 |
| LGPL3 | D10 | I/O | BV _{DD} | 4 |
| LGPL4 | B13 | I/O | BV _{DD} | 24 |
| LGPL5 | C19 | I/O | BV _{DD} | 4 |

Table 1. P1011 Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|--|--------------------|----------|------------------|------|
| LCLK00 | B15 | I/O | BV _{DD} | — |
| LCLK01 | A15 | I/O | BV _{DD} | — |
| NC80 | A13 | NC | — | — |
| NC81 | A14 | NC | — | — |
| DMA | | | | |
| DMA1_DREQ_B00 | Y28 | I | OV _{DD} | — |
| NC101 | W28 | NC | — | — |
| DMA1_DACK_B00 | T28 | O | OV _{DD} | 25 |
| CFG_MEM_DEBUG | T29 | I/O | OV _{DD} | — |
| DMA1_DDONE_B00 | T26 | O | OV _{DD} | 13 |
| CFG_DDR_DEBUG | Y29 | I/O | OV _{DD} | — |
| Programmable Interrupt Controller | | | | |
| UDE0_B | J27 | I | OV _{DD} | 2 |
| NC105 | K28 | NC | — | — |
| MCP0_B | AA27 | I | OV _{DD} | 2 |
| NC106 | M25 | NC | — | — |
| IRQ00 | L24 | I | OV _{DD} | — |
| IRQ01 | K26 | I | OV _{DD} | — |
| IRQ02 | K29 | I | OV _{DD} | — |
| IRQ03 | N25 | I | OV _{DD} | — |
| IRQ04 | L26 | I | OV _{DD} | — |
| IRQ05 | L29 | I | OV _{DD} | — |
| IRQ06 / TDM_RX_CLK | K27 | I | OV _{DD} | — |
| IRQ_OUT_B | N29 | O | OV _{DD} | 2, 3 |
| Voltage Select | | | | |
| LVDD_VSEL | M28 | I | OV _{DD} | 18 |
| BVDD_VSEL0 | M29 | I | OV _{DD} | 18 |
| BVDD_VSEL1 | M27 | I | OV _{DD} | 18 |
| CVDD_VSEL0 | L28 | I | OV _{DD} | 18 |
| CVDD_VSEL1 | L27 | I | OV _{DD} | 18 |
| 1588 | | | | |
| TSEC_1588_CLK_IN | AG21 | I | LV _{DD} | — |

Table 1. P1011 Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---|--------------------|----------|------------------|------|
| TSEC_1588_TRIG_IN1 | AH20 | I | LV _{DD} | — |
| TSEC_1588_TRIG_IN2 | AG20 | I | LV _{DD} | — |
| TSEC_1588_ALARM_OUT1 | AE20 | O | LV _{DD} | 4, 6 |
| TSEC_1588_ALARM_OUT2 | AJ20 | O | LV _{DD} | 4, 6 |
| TSEC_1588_CLK_OUT | AG22 | O | LV _{DD} | 4, 6 |
| TSEC_1588_PULSE_OUT1 | AH21 | O | LV _{DD} | 4, 6 |
| TSEC_1588_PULSE_OUT2 | AJ22 | O | LV _{DD} | 4, 6 |
| Ethernet Management Interface | | | | |
| EC_MDC | AD20 | O | LV _{DD} | 4, 6 |
| EC_MDIO | AJ21 | I/O | LV _{DD} | — |
| Gigabit Ethernet Reference Clock | | | | |
| EC_GTX_CLK125 | AF24 | I | LV _{DD} | 16 |
| Enhanced Three Speed Ethernet Controller 1 | | | | |
| TSEC1_TXD07/TSEC3_TXD03 | AF22 | O | LV _{DD} | 4, 6 |
| TSEC1_TXD06/TSEC3_TXD02 | AD22 | O | LV _{DD} | 4, 6 |
| TSEC1_TXD05/TSEC3_TXD01 | AD23 | O | LV _{DD} | 4, 6 |
| TSEC1_TXD04/TSEC3_TXD00 | AE21 | O | LV _{DD} | 4, 6 |
| TSEC1_TXD03 | AJ25 | O | LV _{DD} | 4, 6 |
| TSEC1_TXD02 | AH28 | O | LV _{DD} | 4, 6 |
| TSEC1_TXD01 | AE25 | O | LV _{DD} | 4, 6 |
| TSEC1_TXD00 | AD24 | O | LV _{DD} | 4, 6 |
| TSEC1_TX_EN | AH24 | O | LV _{DD} | 22 |
| TSEC1_TX_ER | AF23 | O | LV _{DD} | 4, 6 |
| TSEC1_TX_CLK/ TSEC1_GTX_CLK125 | AJ24 | I | LV _{DD} | — |
| TSEC1_GTX_CLK | AG25 | O | LV _{DD} | — |
| TSEC1_CRS/TSEC3_RX_DV | AJ27 | I/O | LV _{DD} | — |
| TSEC1_COL/TSEC3_RX_CLK | AH26 | I | LV _{DD} | — |
| TSEC1_RXD07/TSEC3_RXD03 | AG23 | I | LV _{DD} | — |
| TSEC1_RXD06/TSEC3_RXD02 | AH22 | I | LV _{DD} | — |
| TSEC1_RXD05/TSEC3_RXD01 | AJ23 | I | LV _{DD} | — |
| TSEC1_RXD04/TSEC3_RXD00 | AE24 | I | LV _{DD} | — |

Table 1. P1011 Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|--|--------------------|----------|------------------|--------------------|
| TSEC1_RXD03 | AJ28 | I | LV _{DD} | — |
| TSEC1_RXD02 | AE22 | I | LV _{DD} | — |
| TSEC1_RXD01 | AD21 | I | LV _{DD} | — |
| TSEC1_RXD00 | AH25 | I | LV _{DD} | — |
| TSEC1_RX_DV | AJ26 | I | LV _{DD} | — |
| TSEC1_RX_ER | AH23 | I | LV _{DD} | — |
| TSEC1_RX_CLK | AG26 | I | LV _{DD} | — |
| Three Speed Ethernet Controller 3 | | | | |
| NC82 | AE26 | NC | — | — |
| NC83 | AF26 | NC | — | — |
| TSEC3_TX_EN | AB24 | O | LV _{DD} | 22 |
| TSEC3_GTX_CLK | AB25 | O | LV _{DD} | — |
| NC84 | AG29 | NC | — | — |
| NC85 | AA25 | NC | — | — |
| CFG_DRAM_TYPE | AF27 | I | LV _{DD} | — |
| NC86 | Y24 | NC | — | — |
| NC87 | AA26 | NC | — | — |
| CFG_IO_PORTS3 | AE29 | I | LV _{DD} | — |
| NC88 | AA24 | NC | — | — |
| NC89 | AG28 | NC | — | — |
| TSEC3_RX_ER | AD25 | I/O | LV _{DD} | — |
| TSEC3_TX_CLK | AE27 | I | LV _{DD} | — |
| NC90 | AD27 | NC | — | — |
| NC91 | AB26 | NC | — | — |
| NC92 | AC26 | NC | — | — |
| NC93 | AD26 | NC | — | — |
| NC94 | AB27 | NC | — | — |
| NC95 | AD28 | NC | — | — |
| NC96 | AF29 | NC | — | — |
| NC97 | AF28 | NC | — | — |
| NC98 | AD29 | NC | — | — |
| NC99 | AE28 | NC | — | — |

Table 1. P1011 Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|-----------------------|--------------------|----------|------------------|-------|
| NC100 | AC29 | NC | — | — |
| DUART | | | | |
| UART_SOUT00 | J26 | O | OV _{DD} | 17 |
| UART_SOUT01 | J25 | I/O | OV _{DD} | |
| UART_SIN00 | H29 | I | OV _{DD} | — |
| UART_SIN01 | G24 | I/O | OV _{DD} | — |
| UART_CTS_B00 | J28 | I | OV _{DD} | — |
| UART_CTS_B01 | H24 | I/O | OV _{DD} | — |
| UART_RTS_B00 | J29 | O | OV _{DD} | 5 |
| UART_RTS_B01 | J24 | O | OV _{DD} | 5 |
| I2C | | | | |
| IIC1 | H28 | I/O | OV _{DD} | 3, 12 |
| IIC1_SCL | G27 | I/O | OV _{DD} | 3, 12 |
| IIC2_SDA | H26 | I/O | OV _{DD} | 3, 12 |
| IIC2_SCL | H25 | I/O | OV _{DD} | 3, 12 |
| eSDHC | | | | |
| SDHC_DATA00 | G28 | I/O | CV _{DD} | — |
| SDHC_DATA01 | F27 | I/O | CV _{DD} | — |
| SDHC_DATA02 | G25 | I/O | CV _{DD} | — |
| SDHC_DATA03 | G26 | I/O | CV _{DD} | — |
| SDHC_CMD | F26 | I/O | CV _{DD} | — |
| SDHC_CLK | G29 | O | CV _{DD} | — |
| SPI | | | | |
| SPI_MISO | F28 | I | CV _{DD} | — |
| SPI_MOSI | F25 | I/O | CV _{DD} | — |
| SPI_CS0_B/SDHC_DATA04 | D28 | I/O | CV _{DD} | — |
| SPI_CS1_B/SDHC_DATA05 | E26 | I/O | CV _{DD} | — |
| SPI_CS2_B/SDHC_DATA06 | F29 | I/O | CV _{DD} | — |
| SPI_CS3_B/SDHC_DATA07 | E29 | I/O | CV _{DD} | — |
| SPI_CLK | D29 | O | CV _{DD} | — |
| USB | | | | |
| USB_NXT | B26 | I | CV _{DD} | — |

Table 1. P1011 Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|-------------------------------------|--------------------|----------|------------------|------|
| USB_DIR | A28 | I | CV _{DD} | — |
| USB_STP | B29 | O | CV _{DD} | 25 |
| USB_PWRFAULT | C29 | I | CV _{DD} | — |
| USB_CLK | D27 | I | CV _{DD} | — |
| USB_D07 | C28 | I/O | CV _{DD} | — |
| USB_D06 | C25 | I/O | CV _{DD} | — |
| USB_D05 | B28 | I/O | CV _{DD} | — |
| USB_D04 | B25 | I/O | CV _{DD} | — |
| USB_D03 | D26 | I/O | CV _{DD} | — |
| USB_D02 | A27 | I/O | CV _{DD} | — |
| USB_D01 | A26 | I/O | CV _{DD} | — |
| USB_D00 | C26 | I/O | CV _{DD} | — |
| General-Purpose Input/Output | | | | |
| GPIO00/IRQ07/TDM_TX_DATA | R28 | I/O | OV _{DD} | — |
| GPIO01/IRQ08/TDM_TFS | R26 | I/O | OV _{DD} | — |
| GPIO02/IRQ09/TDM_TX_CLK | P29 | I/O | OV _{DD} | — |
| GPIO03/IRQ10/TDM_RFS | N24 | I/O | OV _{DD} | — |
| GPIO04/IRQ11/TDM_RX_DATA | U29 | I/O | OV _{DD} | — |
| GPIO05 | R24 | I/O | OV _{DD} | — |
| GPIO06 | R29 | I/O | OV _{DD} | — |
| GPIO07 | R25 | I/O | OV _{DD} | — |
| GPIO08/SDHC_CD | F22 | I/O | BV _{DD} | — |
| GPIO09/SDHC_WP | A24 | I/O | BV _{DD} | — |
| GPIO10/USB_PCTL0 | A25 | I/O | BV _{DD} | — |
| GPIO11/USB_PCTL1 | D24 | I/O | BV _{DD} | — |
| GPIO12 | F23 | I/O | BV _{DD} | — |
| GPIO13 | E23 | I/O | BV _{DD} | — |
| GPIO14 | F24 | I/O | BV _{DD} | — |
| GPIO15 | E24 | I/O | BV _{DD} | — |
| System Control | | | | |
| HRESET_B | W25 | I | OV _{DD} | — |
| HRESET_REQ_B | U24 | O | OV _{DD} | 13 |

Table 1. P1011 Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|--|--------------------|----------|------------------|-------|
| SRESET_B | W24 | I | OV _{DD} | — |
| CKSTP_IN0_B | AA29 | I | OV _{DD} | 2 |
| CKSTP_IN1_B | AB29 | I | OV _{DD} | 2 |
| CKSTP_OUT0_B | V25 | O | OV _{DD} | 2, 3 |
| CKSTP_OUT1_B | Y27 | O | OV _{DD} | 2, 3 |
| Debug | | | | |
| TRIG_IN | AB28 | I | OV _{DD} | — |
| TRIG_OUT | U28 | O | OV _{DD} | 6, 13 |
| READY_P1 | W26 | O | OV _{DD} | 6 |
| MSRCID00/LB_MSRCID00/ PLL_PER_OUT00 | P28 | I/O | OV _{DD} | — |
| MSRCID01/LB_MSRCID01/ PLL_PER_OUT01 | R27 | I/O | OV _{DD} | 13 |
| MSRCID02/LB_MSRCID02/ PLL_PER_OUT02 | P27 | I/O | OV _{DD} | 13 |
| MSRCID03/LB_MSRCID03/ PLL_PER_OUT03 | P26 | I/O | OV _{DD} | 13 |
| MSRCID04/LB_MSRCID04/ PLL_UP_DN | N26 | I/O | OV _{DD} | 17 |
| MDVAL/LB_MDVAL/ PLL_PER_VALID | M24 | I/O | OV _{DD} | 13 |
| Clocks | | | | |
| CLK_OUT | T24 | O | OV _{DD} | 8 |
| RTC | K24 | I | OV _{DD} | — |
| DDRCLK | AC9 | I | OV _{DD} | 15 |
| SYSCLK | W29 | I | OV _{DD} | — |
| DFT | | | | |
| SCAN_MODE_B | W27 | I | OV _{DD} | 13 |
| TEST_SEL_B | AA28 | I | OV _{DD} | 25 |
| JTAG | | | | |
| TCK | V29 | I | OV _{DD} | — |
| TDI | T25 | I | OV _{DD} | 9 |
| TDO | V28 | O | OV _{DD} | 8 |
| TMS | U26 | I | OV _{DD} | 9 |

Table 1. P1011 Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|---------------------------------|--------------------|------------------------|------------------|--------|
| TRST_B | V26 | I | OV _{DD} | 9 |
| Power Management | | | | |
| ASLEEP | U25 | O | OV _{DD} | 13 |
| NC1 | G6 | NC | — | — |
| NC2 | Y14 | NC | — | — |
| NC3 | Y15 | NC | — | — |
| NC4 | Y16 | NC | — | — |
| NC5 | AE10 | NC | — | — |
| NC6 | AF10 | NC | — | — |
| NC9 | E14 | NC | — | — |
| NC10 | E13 | NC | — | — |
| NC15 | W6 | NC | — | — |
| Power and Ground Signals | | | | |
| GND | AH10 | — | — | — |
| GND | AJ10 | — | — | — |
| GND | AD10 | — | — | — |
| THERM1 | E16 | Internal Diode Anode | — | 26 |
| THERM0 | E15 | Internal Diode Cathode | — | 26 |
| AGND_SRDS | AD15 | — | — | — |
| AV _{DD} _CORE0 | F16 | — | — | 11, 21 |
| NC117 | F15 | NC | — | — |
| AV _{DD} _DDR | Y10 | — | — | 11 |
| NC102 | F14 | NC | — | — |
| AV _{DD} _PLAT | V24 | — | — | 11 |
| AV _{DD} _SRDS | AD14 | — | — | 11 |
| BV _{DD} | B24 | — | — | — |
| BV _{DD} | C12 | — | — | — |
| BV _{DD} | C14 | — | — | — |
| BV _{DD} | C16 | — | — | — |
| BV _{DD} | C22 | — | — | — |
| BV _{DD} | D18 | — | — | — |

Table 1. P1011 Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|------------------|--------------------|----------|--------------|------|
| BV _{DD} | G20 | — | — | — |
| CV _{DD} | C27 | — | — | — |
| CV _{DD} | E25 | — | — | — |
| CV _{DD} | E27 | — | — | — |
| GV _{DD} | A2 | — | — | — |
| GV _{DD} | B8 | — | — | — |
| GV _{DD} | B11 | — | — | — |
| GV _{DD} | C7 | — | — | — |
| GV _{DD} | C9 | — | — | — |
| GV _{DD} | D3 | — | — | — |
| GV _{DD} | E7 | — | — | — |
| GV _{DD} | F9 | — | — | — |
| GV _{DD} | G10 | — | — | — |
| GV _{DD} | H2 | — | — | — |
| GV _{DD} | K3 | — | — | — |
| GV _{DD} | K7 | — | — | — |
| GV _{DD} | L2 | — | — | — |
| GV _{DD} | L3 | — | — | — |
| GV _{DD} | L4 | — | — | — |
| GV _{DD} | N3 | — | — | — |
| GV _{DD} | N6 | — | — | — |
| GV _{DD} | P4 | — | — | — |
| GV _{DD} | R2 | — | — | — |
| GV _{DD} | U3 | — | — | — |
| GV _{DD} | V5 | — | — | — |
| GV _{DD} | W3 | — | — | — |
| GV _{DD} | Y2 | — | — | — |
| GV _{DD} | AA2 | — | — | — |
| GV _{DD} | AA3 | — | — | — |
| GV _{DD} | AA5 | — | — | — |
| GV _{DD} | AA7 | — | — | — |
| GV _{DD} | AB6 | — | — | — |
| GV _{DD} | AD5 | — | — | — |

Table 1. P1011 Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|-----------------------|--------------------|----------|--------------|------|
| GV _{DD} | AD9 | — | — | — |
| GV _{DD} | AE3 | — | — | — |
| GV _{DD} | AF4 | — | — | — |
| GV _{DD} | AG6 | — | — | — |
| GV _{DD} | AG8 | — | — | — |
| GV _{DD} | AJ2 | — | — | — |
| LV _{DD} | Y23 | — | — | — |
| LV _{DD} | AC21 | — | — | — |
| LV _{DD} | AC25 | — | — | — |
| LV _{DD} | AC27 | — | — | — |
| LV _{DD} | AE23 | — | — | — |
| LV _{DD} | AF21 | — | — | — |
| LV _{DD} | AF25 | — | — | — |
| LV _{DD} | AH27 | — | — | — |
| LV _{DD} | AH29 | — | — | — |
| SV _{DD_SRDS} | AG16 | — | — | — |
| SV _{DD_SRDS} | AH13 | — | — | — |
| SV _{DD_SRDS} | AH17 | — | — | — |
| SV _{DD_SRDS} | AJ11 | — | — | — |
| SV _{DD_SRDS} | AJ15 | — | — | — |
| SV _{DD_SRDS} | AJ19 | — | — | — |
| SGND_SRDS | AG12 | — | — | — |
| SGND_SRDS | AG13 | — | — | — |
| SGND_SRDS | AG14 | — | — | — |
| SGND_SRDS | AG17 | — | — | — |
| SGND_SRDS | AG18 | — | — | — |
| SGND_SRDS | AG19 | — | — | — |
| SGND_SRDS | AH11 | — | — | — |
| SGND_SRDS | AH15 | — | — | — |
| SGND_SRDS | AH19 | — | — | — |
| SGND_SRDS | AJ13 | — | — | — |
| SGND_SRDS | AJ17 | — | — | — |
| XV _{DD_SRDS} | AD13 | — | — | — |

Table 1. P1011 Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|------------------------|--------------------|----------|--------------|------|
| XV _{DD} _SRDS | AD17 | — | — | — |
| XV _{DD} _SRDS | AE11 | — | — | — |
| XV _{DD} _SRDS | AE19 | — | — | — |
| XV _{DD} _SRDS | AF14 | — | — | — |
| XV _{DD} _SRDS | AF16 | — | — | — |
| XGND_SRDS | AD11 | — | — | — |
| XGND_SRDS | AD19 | — | — | — |
| XGND_SRDS | AE14 | — | — | — |
| XGND_SRDS | AE16 | — | — | — |
| XGND_SRDS | AF11 | — | — | — |
| XGND_SRDS | AF12 | — | — | — |
| XGND_SRDS | AF18 | — | — | — |
| XGND_SRDS | AG10 | — | — | — |
| MVREF | R6 | — | — | — |
| OV _{DD} | K23 | — | — | — |
| OV _{DD} | L25 | — | — | — |
| OV _{DD} | N27 | — | — | — |
| OV _{DD} | P25 | — | — | — |
| OV _{DD} | U27 | — | — | — |
| OV _{DD} | Y26 | — | — | — |
| NC103 | F13 | NC | — | — |
| NC104 | P6 | NC | — | — |
| NC110 | K10 | NC | — | — |
| NC111 | K11 | NC | — | — |
| NC112 | K12 | NC | — | — |
| NC113 | K13 | NC | — | — |
| NC114 | K14 | NC | — | — |
| NC115 | L10 | NC | — | — |
| NC116 | M10 | NC | — | — |
| V _{DDC} | K15 | — | — | — |
| V _{DDC} | K17 | — | — | — |
| V _{DDC} | K19 | — | — | — |
| V _{DDC} | K16 | — | — | — |

Table 1. P1011 Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|------------------|--------------------|----------|--------------|------|
| V _{DDC} | L20 | — | — | — |
| V _{DDC} | K18 | — | — | — |
| V _{DDC} | K20 | — | — | — |
| V _{DDC} | N10 | — | — | — |
| V _{DDC} | N20 | — | — | — |
| V _{DDC} | M20 | — | — | — |
| V _{DDC} | R10 | — | — | — |
| V _{DDC} | R20 | — | — | — |
| V _{DDC} | P10 | — | — | — |
| V _{DDC} | P20 | — | — | — |
| V _{DDC} | U10 | — | — | — |
| V _{DDC} | U20 | — | — | — |
| V _{DDC} | T10 | — | — | — |
| V _{DDC} | T20 | — | — | — |
| V _{DDC} | W10 | — | — | — |
| V _{DDC} | V10 | — | — | — |
| V _{DDC} | V20 | — | — | — |
| V _{DDC} | W20 | — | — | — |
| V _{DDC} | Y11 | — | — | — |
| V _{DDC} | Y19 | — | — | — |
| GND | A1 | — | — | — |
| GND | A29 | — | — | — |
| GND | B5 | — | — | — |
| GND | B14 | — | — | — |
| GND | B27 | — | — | — |
| GND | C6 | — | — | — |
| GND | C8 | — | — | — |
| GND | C11 | — | — | — |
| GND | C18 | — | — | — |
| GND | C24 | — | — | — |
| GND | D16 | — | — | — |
| GND | D22 | — | — | — |
| GND | D25 | — | — | — |

Table 1. P1011 Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|--------|--------------------|----------|--------------|------|
| GND | E3 | — | — | — |
| GND | E28 | — | — | — |
| GND | F7 | — | — | — |
| GND | G5 | — | — | — |
| GND | G9 | — | — | — |
| GND | G21 | — | — | — |
| GND | H3 | — | — | — |
| GND | H27 | — | — | — |
| GND | J7 | — | — | — |
| GND | J23 | — | — | — |
| GND | K4 | — | — | — |
| GND | F17 | — | — | — |
| GND | L12 | — | — | — |
| GND | L14 | — | — | — |
| GND | L16 | — | — | — |
| GND | L18 | — | — | — |
| GND | M11 | — | — | — |
| GND | K25 | — | — | — |
| GND | L1 | — | — | — |
| GND | L11 | — | — | — |
| GND | L13 | — | — | — |
| GND | L15 | — | — | — |
| GND | L17 | — | — | — |
| GND | L19 | — | — | — |
| GND | M3 | — | — | — |
| GND | M4 | — | — | — |
| GND | M6 | — | — | — |
| GND | M19 | — | — | — |
| GND | M12 | — | — | — |
| GND | M13 | — | — | — |
| GND | M14 | — | — | — |
| GND | M15 | — | — | — |
| GND | M16 | — | — | — |

Table 1. P1011 Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|--------|--------------------|----------|--------------|------|
| GND | M17 | — | — | — |
| GND | M18 | — | — | — |
| GND | P11 | — | — | — |
| GND | M26 | — | — | — |
| GND | N2 | — | — | — |
| GND | N11 | — | — | — |
| GND | N12 | — | — | — |
| GND | N13 | — | — | — |
| GND | N14 | — | — | — |
| GND | N15 | — | — | — |
| GND | N16 | — | — | — |
| GND | N17 | — | — | — |
| GND | N18 | — | — | — |
| GND | N19 | — | — | — |
| GND | N28 | — | — | — |
| GND | P5 | — | — | — |
| GND | P19 | — | — | — |
| GND | P12 | — | — | — |
| GND | P13 | — | — | — |
| GND | P14 | — | — | — |
| GND | P15 | — | — | — |
| GND | P16 | — | — | — |
| GND | P17 | — | — | — |
| GND | P18 | — | — | — |
| GND | T11 | — | — | — |
| GND | P24 | — | — | — |
| GND | R3 | — | — | — |
| GND | R11 | — | — | — |
| GND | R12 | — | — | — |
| GND | R13 | — | — | — |
| GND | R14 | — | — | — |
| GND | R15 | — | — | — |
| GND | R16 | — | — | — |

Table 1. P1011 Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|--------|--------------------|----------|--------------|------|
| GND | R17 | — | — | — |
| GND | R18 | — | — | — |
| GND | R19 | — | — | — |
| GND | T6 | — | — | — |
| GND | T19 | — | — | — |
| GND | T12 | — | — | — |
| GND | T13 | — | — | — |
| GND | T14 | — | — | — |
| GND | T15 | — | — | — |
| GND | T16 | — | — | — |
| GND | T17 | — | — | — |
| GND | T18 | — | — | — |
| GND | V11 | — | — | — |
| GND | T27 | — | — | — |
| GND | U11 | — | — | — |
| GND | U12 | — | — | — |
| GND | U13 | — | — | — |
| GND | U14 | — | — | — |
| GND | U15 | — | — | — |
| GND | U16 | — | — | — |
| GND | U17 | — | — | — |
| GND | U18 | — | — | — |
| GND | U19 | — | — | — |
| GND | V4 | — | — | — |
| GND | V19 | — | — | — |
| GND | V12 | — | — | — |
| GND | V13 | — | — | — |
| GND | V14 | — | — | — |
| GND | V15 | — | — | — |
| GND | V16 | — | — | — |
| GND | V17 | — | — | — |
| GND | V18 | — | — | — |
| GND | W12 | — | — | — |

Table 1. P1011 Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|------------------|--------------------|----------|--------------|------|
| GND | V27 | — | — | — |
| GND | W2 | — | — | — |
| GND | W4 | — | — | — |
| GND | W11 | — | — | — |
| GND | W13 | — | — | — |
| GND | W14 | — | — | — |
| GND | W15 | — | — | — |
| GND | W16 | — | — | — |
| GND | W17 | — | — | — |
| GND | W19 | — | — | — |
| GND | Y3 | — | — | — |
| GND | Y6 | — | — | — |
| GND | Y7 | — | — | — |
| GND | W18 | — | — | — |
| V _{DDC} | Y12 | — | — | — |
| GND | Y13 | — | — | — |
| GND | Y17 | — | — | — |
| V _{DDC} | Y18 | — | — | — |
| V _{DDC} | Y20 | — | — | — |
| GND | Y25 | — | — | — |
| GND | AA6 | — | — | — |
| GND | AA23 | — | — | — |
| GND | AC3 | — | — | — |
| GND | AC10 | — | — | — |
| GND | AC20 | — | — | — |
| GND | AC24 | — | — | — |
| GND | AC28 | — | — | — |
| GND | AD3 | — | — | — |
| GND | AD6 | — | — | — |
| GND | AE9 | — | — | — |
| GND | AF20 | — | — | — |
| GND | AG3 | — | — | — |
| GND | AG5 | — | — | — |

Table 1. P1011 Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|--------|--------------------|----------|--------------|------|
| GND | AG7 | — | — | — |
| GND | AG24 | — | — | — |
| GND | AG27 | — | — | — |
| GND | AJ1 | — | — | — |
| GND | AJ29 | — | — | — |

Note:

- All multiplexed signals are listed only once and do not re-occur.
- Recommend that a weak pull-up resistor (2–10 K Ω) be placed on this pin to OVDD.
- This pin is an open drain signal.
- This pin is a reset configuration pin. It has a weak internal pull-up, P-FET, which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-k Ω pull-down resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, a pull-up or active driver is needed.
- The value of LALE, LGPL2, and LBCTL at reset sets the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-k Ω pull-up or pull-down resistors. See *P1020 QorIQ Integrated Processor Reference Manual* for clock ratio settings.
- Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin is described as an I/O for boundary scan.
- If this pin is configured for local bus controller usage, it is recommended that a weak pull-up resistor (2–10 K Ω) be placed on this pin to BVDD, ensuring that there is no random chip select assertion due to possible noise or other factors.
- This output is actively driven during reset rather than being three-stated during reset.
- These JTAG pins have weak internal pull-up P-FETs that are always enabled.
- Do not connect.
- Independent supplies derived from board VDD.
- Recommend that a pull-up resistor (~1 k Ω) be placed on this pin to OVDD.
- These pins must NOT be pulled down by a resistor or the component they are connected to during power-on reset: LA28, LA17, HRESET_REQ, MSRCID[1:3], MDVAL, ASLEEP, DMA1_DDONE_B00, SCAN_MODE_B, TRIG_OUT.
- For DDR2 MDIC[0] is grounded through an 18.2- Ω (full-strength mode) or 36.4- Ω (half-strength mode) precision 1% resistor and Dn_MDIC[1] is connected to GVDD through an 18.2- Ω (full-strength mode) or 36.4- Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR IOs. The calibration resistor value for DDR3 should be 20- Ω (full-strength mode) or 40- Ω (half-strength mode).

Table 1. P1011 Pinout Listing (continued)

| Signal | Package Pin Number | Pin Type | Power Supply | Note |
|--------|--------------------|----------|--------------|------|
|--------|--------------------|----------|--------------|------|

15. DDRCLK input is only required when the P1011 DDR controller is running in asynchronous mode. When the DDR controller is configured to run in synchronous mode via POR setting `cfg_ddr_pll[0:2] = 111`, the DDRCLK input is not required. It is recommended that users tie it off to GND when DDR controller is running in synchronous mode. See the “Clock Signals” section and the “DDR Complex Clock PLL Ratio” table in the “DDR PLL Ratio” section of the *P1020QorIQ Integrated Host Processor Family Reference Manual*, for a more detailed description of DDR controller operation in asynchronous and synchronous modes.
16. EC_GTX_CLK125 is a 125-MHz input clock shared among all eTSEC ports in the following modes: RGMII. If none of the eTSEC ports is operating in these modes, the EC_GTX_CLK125 input can be tied off to GND.
17. These POR configuration inputs may be used in the future to control functionality. It is advised that boards are built with the ability to pull-down these pins. LA[20:22], UART_SOUT[0], and MSRCID[4] are reserved for future reset configuration.
18. Incorrect settings can lead to irreversible device damage.
19. The value of LAD[0:15] during reset sets the upper 16 bits of the GPPORCR.
20. The value of LA27 during reset is used to determine CPU boot configuration. See the “CPU Boot POR Configuration,” section in the applicable device reference manual.
21. It must be the same as V_{DD_Core} .
22. When eTSEC1 and eTSEC3 are used as parallel interfaces, pins TSEC1_TX_EN and TSEC3_TX_EN requires an external 4.7-k Ω pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven. However, because of the pull-down resistor on TSEC3_TX_EN cause the eSDHC card-detect (`cfg_sdhc_cd_pol_sel`) to be inverted, the inversion should be overridden from the SDHCDCR [CD_INV] debug control register.
23. SD_IMP_CAL_RX should be grounded through an 200- Ω precision 1% resistor and SD_IMP_CAL_TX is grounded through an 100- Ω precision 1% resistor.
24. For systems which boot from Local Bus (GPCM)-controlled NOR flash or (FCM)-controlled NAND flash, a pull-up on LGPL4 is required.
25. Refer to AN4259 for the correct settings.
26. These pins may be connected to a temperature diode monitoring device such as the On Semiconductor, NCT1008™. If a temperature diode monitoring device is not connected, these pins may be connected to test point or left as a no connect.

2 Electrical Characteristics

This section provides the AC and DC electrical specifications. The processor is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings¹

| Characteristic | Symbol | Max Value | Unit | Note |
|---|--|--|------|------|
| Core 0 and platform supply voltage | V_{DDC} | -0.3 to 1.05 | V | — |
| PLL supply voltage | AV_{DD_CORE0} AV_{DD_DDR} AV_{DD_PLAT} AV_{DD_SRDS} | -0.3 to 1.05 | V | 8 |
| Core power supply for SerDes transceivers | SV_{DD_SRDS} | -0.3 to 1.05 | V | — |
| Pad power supply for SerDes transceivers | XV_{DD_SRDS} | -0.3 to 1.05 | V | — |
| DDR2/3 DRAM I/O voltage | GV_{DD} | -0.3 to 1.98 | V | — |
| Three-speed Ethernet I/O, MII management voltage (eTSEC) | LV_{DD} | -0.3 to 3.63 -0.3 to 2.75 | V | 1, 4 |
| DUART, system control and power management, I ² C, GPIOx 8, and JTAG I/O voltage | OV_{DD} | -0.3 to 3.63 | V | — |
| USB, eSPI, eSDHC | CV_{DD} | -0.3 to 3.63 -0.3 to 2.75 -0.3 to 1.98 | V | — |
| Enhanced local bus I/O voltage and GPIOx8 voltage | BV_{DD} | -0.3 to 3.63 -0.3 to 2.75 -0.3 to 1.98 | V | — |

Table 2. Absolute Maximum Ratings¹ (continued)

| Characteristic | | Symbol | Max Value | Unit | Note |
|---------------------------|--|------------|-------------------------------|------|------|
| Input voltage | DDR2/DDR3 DRAM signals | MV_{IN} | -0.3 to ($GV_{DD} + 0.3$) | V | 2, 7 |
| | DDR2/DDR3 DRAM reference | MV_{REF} | -0.3 to ($GV_{DD}/2 + 0.3$) | V | — |
| | Three-speed Ethernet signals | LV_{IN} | -0.3 to ($LV_{DD} + 0.3$) | V | 3, 7 |
| | Enhanced local bus signals | BV_{IN} | -0.3 to ($BV_{DD} + 0.3$) | — | 5 |
| | DUART, SYSCLK, system control and power management, I ² C, clocking, I/O voltage select, and JTAG I/O voltage | OV_{IN} | -0.3 to ($OV_{DD} + 0.3$) | V | 6, 7 |
| | USB, eSPI, eSDHC | CV_{IN} | -0.3 to ($CV_{DD} + 0.3$) | V | 4 |
| | SerDes signals | XV_{IN} | -0.3 to ($XV_{DD} + 0.3$) | V | — |
| Storage temperature range | | T_{STG} | -55 to 150 | °C | — |

Notes:

- Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution: LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution: CV_{IN} must not exceed CV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution: BV_{IN} must not exceed BV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- (C,X,B,G,L,O) V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 7.
- AV_{DD} is measured at the input to the filter (as shown in AN4259) and not at the pin of the device.

2.1.2 Recommended Operating Conditions

This table provides the recommended operating conditions for this device. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

| Characteristic | Symbol | Recommended Value | Unit | Notes |
|--|--|-------------------|------|-------|
| Core 0 and platform supply voltage | V_{DDC} | 1.0 ± 50 mV | V | 1 |
| PLL supply voltage | AV_{DD_CORE0} AV_{DD_DDR} AV_{DD_PLAT} AV_{DD_SRDS} | 1.0 ± 50 mV | V | — |
| Core power supply for SerDes transceivers | SV_{DD_SRDS} | 1.0 ± 50 mV | V | — |
| Pad power supply for SerDes transceivers and PCI Express | XV_{DD_SRDS} | 1.0 ± 50 mV | V | — |
| DDR2 DRAM I/O voltage | GV_{DD} | 1.8 V ± 90 mV | V | — |
| DDR3 DRAM I/O voltage | GV_{DD} | 1.5 V ± 75 mV | — | — |

Table 3. Recommended Operating Conditions (continued)

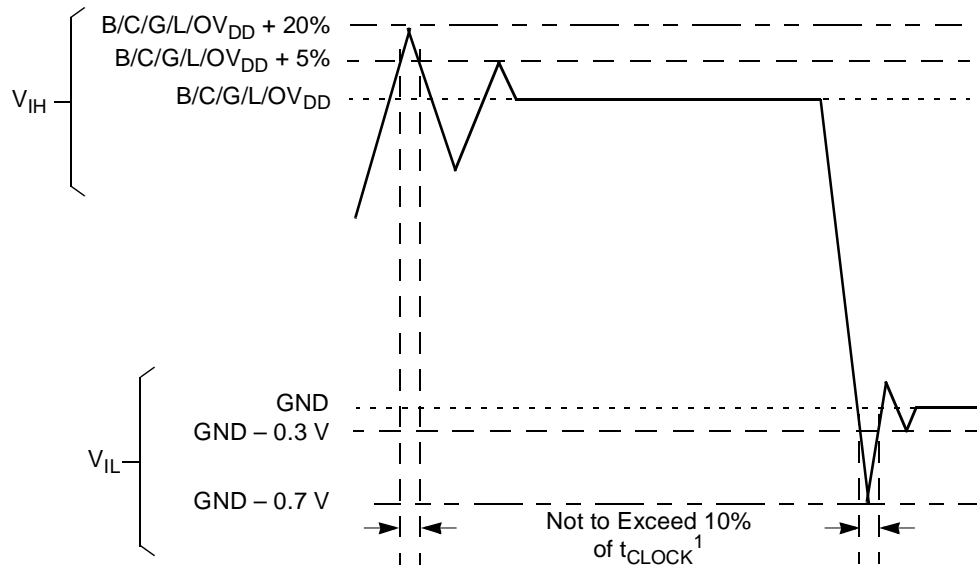
| Characteristic | | Symbol | Recommended Value | Unit | Notes |
|--|--|------------|---|------|-------|
| Three-speed Ethernet I/O voltage (eTSEC) | | LV_{DD} | 3.3 V \pm 165 mV 2.5 V \pm 125 mV | V | — |
| DUART, system control and power management, I ² C, GPIOx8, and JTAG I/O voltage | | OV_{DD} | 3.3 V \pm 165 mV | V | — |
| Enhanced local bus I/O and GPIOx8 voltage | | BV_{DD} | 3.3 V \pm 165 mV 2.5 V \pm 125 mV 1.8 V \pm 90 mV | V | — |
| USB, eSPI, eSDHC | | CV_{DD} | 3.3 V \pm 165 mV 2.5 V \pm 125 mV 1.8 V \pm 90 mV | V | — |
| Input voltage | DDR2/3 DRAM signals | MV_{IN} | GND to GV_{DD} | V | — |
| | DDR2/3 DRAM reference | MV_{REF} | GND to $GV_{DD}/2$ | V | — |
| | Three-speed Ethernet signals | LV_{IN} | GND to LV_{DD} | V | — |
| | Enhanced local bus signals | BV_{IN} | GND to BV_{DD} | V | — |
| | DUART, SYSCLK, system control and power management, I ² C, and JTAG signals | OV_{IN} | GND to OV_{DD} | V | — |
| | USB, eSPI, eSDHC | CV_{IN} | GND to CV_{DD} | V | — |
| Junction temperature range | | TA/TJ | 0 to 125 Commercial –40 to 125 Industrial | °C | 3 |

Notes:

1. **Caution:** Until V_{DD} reaches its recommended operating voltage, V_{DD} may exceed L/C/B/G/ OV_{DD} by up to 0.7 V. If 0.7 V is exceeded, extra current will be drawn by the device.
2. **Caution:** Until V_{DD} reaches its recommended operating voltage, if L/C/B/G/ OV_{DD} exceeds V_{DD} , extra current may be drawn by the device.
3. Min temp is specified with T_A ; Max temp is specified with T_J .

Electrical Characteristics

This figure shows the undershoot and overshoot voltages at the interfaces of the device.



Note:

1. t_{CLOCK} refers to the clock period associated with the respective interface:
 For I²C and JTAG, t_{CLOCK} references SYSCLK.
 For DDR, t_{CLOCK} references MCK.
 For eTSEC, t_{CLOCK} references EC_GTX_CLK125.
 For eLBC, t_{CLOCK} references LCLK.

Figure 7. Overshoot/Undershoot Voltage for BV_{DD}/CV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}

The core voltage must always be provided at nominal 1.0 V (see [Table 3](#) for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in [Table 3](#). The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The SDRAM interface uses a differential receiver referenced the externally supplied MV_{REF} signal (nominally set to GV_{DD}/2). The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

2.1.3 Output Driver Characteristics

This table provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 4. Output Drive Capability

| Driver Type | Output Impedance (Ω) | Supply Voltage | Notes |
|---|--|--|-------|
| Enhanced local bus interface, GPIO[0:7] | 45 45 45 | BV _{DD} = 3.3 V BV _{DD} = 2.5 V BV _{DD} = 1.8 V | — |
| DDR2 signal (programmable) | 18 (full-strength mode) 36 (half-strength mode) | GV _{DD} = 1.8 V | 11 |
| DDR 3 signal (programmable) | 20 (full-strength mode) 40 (half-strength mode) | GV _{DD} = 1.5 V | 1 |

Table 4. Output Drive Capability (continued)

| Driver Type | Output Impedance (Ω) | Supply Voltage | Notes |
|-----------------------------|-------------------------------|--|-------|
| TSEC signals | 45 | $LV_{DD} = 2.5/3.3\text{ V}$ | — |
| DUART, system control, JTAG | 45 | $OV_{DD} = 3.3\text{ V}$ | — |
| I ² C | 45 | $OV_{DD} = 3.3\text{ V}$ | — |
| USB, SPI, eSDHC | 45 | $CV_{DD} = 3.3\text{ V}$ $CV_{DD} = 2.5\text{ V}$ $CV_{DD} = 1.8\text{ V}$ | — |

Note:

- The drive strength of the DDR2/3 interface in half-strength mode is at $T_j = 105^\circ\text{C}$ and at GV_{DD} (min)

2.2 Power Sequencing

The processor requires that its power rails be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

- V_{DD} , V_{DDC} , AV_{DD} , BV_{DD} , LV_{DD} , CV_{DD} , OV_{DD} , SV_{DD_SRDS} and, XV_{DD_SRDS}
- GV_{DD}

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

To guarantee MCKE low during power-up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, the sequencing for GV_{DD} is not required.

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

2.3 Power Down Requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

2.4 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements. This table provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Table 5. RESET Initialization Timing Specifications

| Parameter/Condition | Min | Max | Unit | Note |
|---|-----|-----|---------------|------|
| Required assertion time of $\overline{\text{HRESET}}$ | 25 | — | μs | 1, 2 |
| Minimum assertion time of $\overline{\text{TRESET}}$ simultaneous to HRESET assertion | 25 | — | ns | 3 |
| Maximum rise/fall time of $\overline{\text{HRESET}}$ | — | 1 | SYSCLK | — |
| Minimum assertion time for $\overline{\text{SRESET}}$ | 3 | — | SYSCLKs | 4 |

Table 5. RESET Initialization Timing Specifications (continued)

| Parameter/Condition | Min | Max | Unit | Note |
|---|-----|-----|---------|------|
| Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$ | 4 | — | SYSCLKs | 4 |
| Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$ | 2 | — | SYSCLKs | 4 |
| Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$ | — | 5 | SYSCLKs | 4 |

Notes:

1. There may be some extra current leakage when driving signals high during this time.
2. Reset assertion timing requirements for DDR3 DRAMs may differ.
3. TRST is an asynchronous level sensitive signal. For guidance on how this requirement can be met, refer to the JTAG signal termination guidelines in AN4259.
4. SYSCLK is the primary clock input for the processor.

This table provides the PLL lock times.

Table 6. PLL Lock Times

| Parameter/Condition | Min | Max | Unit | Notes |
|---------------------|-----|-----|---------------|-------|
| PLL lock times | — | 100 | μs | — |

2.5 Power-on Ramp Rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid falsely triggering the ESD circuitry. This table provides the power supply ramp rate specifications.

Table 7. Power Supply Ramp Rate

| Parameter | Min | Max | Unit | Notes |
|---|-----|-------|------|-------|
| Required ramp rate for all voltage supplies (including OVDD/CVDD/GVDD/BVDD/SVDD/LVDD, All VDD supplies, MVREF and all AVDD supplies.) | — | 36000 | V/s | 1, 2 |

Note:

1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range (see [Table 3](#)).

2.6 Power Characteristics

The core power dissipation for the core complex bus (CCB) versus the core frequency for this family of QorIQ devices is shown in this table.

Table 8. Core Power Dissipation

| Core Frequency (MHz) | Platform Frequency (MHz) | V _{DD} (V) | Power Mode | Junction Temperature (°C) | Power (W) | Notes |
|----------------------|--------------------------|---------------------|------------|---------------------------|-----------|------------|
| 533 | 266 | 1 | Typical | 65 | 1.37 | 1, 2, 3 |
| | | | | Thermal | 105 | 2.19 |
| | | | 125 | | 2.42 | 1, 4, 5 |
| | | | Maximum | 105 | 2.22 | 1, 5, 6, 7 |
| | | | | 125 | 2.45 | 1, 5, 6, 7 |
| | | | 667 | 333 | 1 | Typical |
| Thermal | 105 | 2.29 | | | | |
| | 125 | 2.51 | | | | 1, 4, 5 |
| Maximum | 105 | 2.33 | | | | 1, 5, 6, 7 |
| | 125 | 2.55 | | | | 1, 5, 6, 7 |
| 800 | 400 | 1 | | | | Typical |
| | | | Thermal | 105 | 2.38 | |
| | | | | 125 | 2.61 | 1, 4, 5 |
| | | | Maximum | 105 | 2.43 | 1, 5, 6, 7 |
| | | | | 125 | 2.65 | 1, 5, 6, 7 |

Note:

1. Combined power of VDD, VDDC, and AVDD_n with DDR controller/s and all SerDes banks active. Does not include I/O power.
2. Typical power assumes Dhrystone running with activity factor of 80% (on all cores) and executing DMA on the platform with 90% activity factor.
3. Typical power based on nominal processed device.
4. Thermal power assumes Dhrystone running with activity factor of 80% (on all cores) and executing DMA on the platform at 90% activity factor.
5. Thermal and maximum power are based on worst case processed device.
6. Maximum power assumes Dhrystone running with activity factor at 100% (on all cores) and executing DMA on the platform at 100% activity factor.
7. Maximum power provided for power supply design sizing.

2.6.1 I/O DC Power Supply Recommendation

This table provides estimated I/O power numbers for each block: DDR, PCIe, eLBC, eTSEC, SGMII, eSDHC, USB, eSPI, DUART, I²C, and GPIO.

Table 9. I/O Power Supply Estimated Values

| Interface | Parameter | Symbol | Typical | Unit | Notes |
|----------------------|-------------------|----------------------------|---------|------|---------|
| DDR3 75% utilization | 600 MHz data rate | GV _{DD} (1.5 V) | 0.76 | W | 1, 2 |
| | 667 MHz data rate | GV _{DD} (1.5 V) | 0.82 | W | 1, 2 |
| DDR3 40% utilization | 600 MHz data rate | GV _{DD} (1.5 V) | 0.57 | W | 1, 2 |
| | 667 MHz data rate | GV _{DD} (1.5 V) | 0.63 | W | 1, 2 |
| PCI Express | x1, 2.5 G-baud | X/SV _{DD} (1.0 V) | 0.11 | W | 1 |
| | x2, 2.5 G-baud | X/SV _{DD} (1.0 V) | 0.15 | W | 1 |
| | x4, 2.5 G-baud | X/SV _{DD} (1.0 V) | 0.229 | W | 1 |
| SGMII | x1, 1.25G-baud | X/SV _{DD} (1.0 V) | 0.096 | W | 1 |
| eLBC | 16-bit, 83MHz | BV _{DD} (1.8 V) | 0.017 | W | 1, 3 |
| | | BV _{DD} (2.5 V) | 0.03 | W | 1, 3 |
| | | BV _{DD} (3.3 V) | 0.047 | W | 1, 3 |
| eTSEC | RGMII | LV _{DD} (2.5 V) | 0.075 | W | 1, 3, 4 |
| | | LV _{DD} (3.3 V) | 0.124 | W | 1, 3, 4 |
| eSDHC | — | CV _{DD} (1.8 V) | 0.005 | W | 1, 3 |
| | | CV _{DD} (2.5 V) | 0.009 | W | 1, 3 |
| | | CV _{DD} (3.3 V) | 0.014 | W | 1, 3 |
| USB (per port) | — | CV _{DD} (1.8 V) | 0.004 | W | 1, 3 |
| | | CV _{DD} (2.5 V) | 0.008 | W | 1, 3 |
| | | CV _{DD} (3.3 V) | 0.012 | W | 1, 3 |
| eSPI | — | CV _{DD} (1.8 V) | 0.004 | W | 1, 3 |
| | | CV _{DD} (2.5 V) | 0.006 | W | 1, 3 |
| | | CV _{DD} (3.3 V) | 0.01 | W | 1, 3 |
| I ² C | — | OV _{DD} (3.3 V) | 0.002 | W | 1, 3 |
| DUART | — | OV _{DD} (3.3 V) | 0.006 | W | 1, 3 |
| IEEE1588 | — | LV _{DD} (2.5 V) | 0.004 | W | 1, 3 |
| | | LV _{DD} (3.3 V) | 0.007 | W | 1, 3 |
| GPIO [0:7] | x8 | OV _{DD} (3.3 V) | 0.004 | W | 1, 3, 5 |

Table 9. I/O Power Supply Estimated Values (continued)

| Interface | Parameter | Symbol | Typical | Unit | Notes |
|-------------|-----------|-------------------|---------|------|---------|
| GPIO [8:15] | x8 | BV_{DD} (1.8 V) | 0.002 | W | 1, 3, 5 |
| | | BV_{DD} (2.5 V) | 0.003 | W | 1, 3, 5 |
| | | BV_{DD} (3.3 V) | 0.005 | W | 1, 3, 5 |

Notes:

1. The typical values are estimates based on simulations 65 C junction temperature.
2. DDR power numbers are based on 2 rank DIMM.
3. Assuming 15 pF total capacitance load per pin.
4. The current values are per each eTSEC used.
5. GPIO x8 support on OVDD and x8 on BVDD rail supply.

2.7 Input Clocks

This section discusses the system clock timing, SYSCLK and spread spectrum sources, real time clock timing, eTSEC Gigabit reference clock timing, DDR clock timing, and other input clocks.

2.7.1 System Clock Timing

This table provides the system clock (SYSCLK) DC specifications.

Table 10. SYSCLK DC Electrical Characteristics

At recommended operating conditions with $OV_{DD} = 3.3 \text{ V} \pm 165 \text{ mV}$

| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
|---|----------|-----|---------|----------|---------------|-------|
| Input high voltage | V_{IH} | 2.0 | — | | V | 1 |
| Input low voltage | V_{IL} | — | — | 0.8 | V | 1 |
| Input capacitance | C_{IN} | — | 7 | 15 | pf | — |
| Input current ($V_{IN} = 0 \text{ V}$ or $V_{IN} = V_{DD}$) | I_{IN} | — | — | ± 50 | μA | 2 |

Note:

1. The max V_{IH} , and min V_{IL} values can be found in Table 3.
2. The symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 3.

This table provides the system clock (SYSCLK) AC timing specifications.

Table 11. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 3) with $OV_{DD} = 3.3 \text{ V} \pm 165 \text{ mV}$

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|--|------------------------------------|-----|---------|-----------|------|-------|
| SYSCLK frequency | f_{SYSCLK} | 64 | — | 100 | MHz | 1 |
| SYSCLK cycle time | t_{SYSCLK} | 10 | — | 15 | ns | — |
| SYSCLK duty cycle | $t_{\text{KHK}}/t_{\text{SYSCLK}}$ | 40 | — | 60 | % | 2 |
| SYSCLK slew rate | — | 1 | — | 4 | V/ns | 3 |
| SYSCLK peak period jitter | — | — | — | ± 150 | ps | — |
| SYSCLK jitter phase noise at -56dBc | — | — | — | 500 | KHz | 4 |

Table 11. SYSCLK AC Timing Specifications (continued)At recommended operating conditions (see Table 3) with $OV_{DD} = 3.3\text{ V} \pm 165\text{ mV}$

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|--|-----------------|-----|---------|-----|------|-------|
| AC Input Swing Limits at 3.3 V OV_{DD} | ΔV_{AC} | 1.9 | — | — | V | — |

Notes:

- Caution:** The CCB_clk to SYSCLK ratio and e500 core to CCB_clk ratio settings must be chosen such that the resulting SYSCLK frequency, e500 core frequency, and CCB_clk frequency do not exceed their respective maximum or minimum operating frequencies. Refer to for ratio settings.
- Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.
- Slew rate as measured from $\pm 0.3 \Delta V_{AC}$ at center of peak to peak voltage at clock input.
- Phase noise is calculated as FFT of TIE jitter.

2.7.2 SYSCLK and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 12 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the processor's input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the P1011 is compatible with spread spectrum sources if the recommendations listed in this table are observed.

Table 12. Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 3.

| Parameter | Min | Max | Unit | Notes |
|----------------------|-----|-----|------|-------|
| Frequency modulation | — | 60 | kHz | — |
| Frequency spread | — | 1.0 | % | 1, 2 |

Note:

- SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 11.
- Maximum spread spectrum frequency may not result in exceeding any maximum operating frequency of the device.

CAUTION

The processor's minimum and maximum SYSCLK, DDRCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e500 core/DDR memory frequency should avoid violating the stated limits by using down-spreading only.

2.7.3 Real Time Clock Timing

The real time clock timing (RTC) input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than $2 \times$ the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

2.7.4 eTSEC Gigabit Reference Clock Timing

This table lists the eTSEC gigabit reference clock DC electrical characteristics.

Table 13. eTSEC Gigabit Reference Clock DC Electrical Characteristics

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|----------|-----|----------|---------|-------|
| High-level input voltage | V_{IH} | 2 | — | V | 1 |
| Low-level input voltage | V_{IL} | — | 0.8 | V | 1 |
| Input current ($V_{IN} = 0$ V or $V_{IN} = V_{DD}$) | I_{IN} | — | ± 40 | μ A | 2 |

Note:

- The max V_{IH} , and min V_{IL} values can be found in Table 3.
- The symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 3.

This table provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications.

Table 14. EC_GTX_CLK125 AC Timing Specifications

At recommended operating conditions with $LV_{DD} = 2.5 \pm 0.125$ mV/ 3.3 V ± 165 mV

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|---|-----------------------|-----|---------|-------------|------|-------|
| EC_GTX_CLK125 frequency | t_{G125} | — | 125 | — | MHz | — |
| EC_GTX_CLK125 cycle time | t_{G125} | — | 8 | — | ns | — |
| EC_GTX_CLK rise and fall time $LV_{DD} = 2.5$ V $LV_{DD} = 3.3$ V | t_{G125R}/t_{G125F} | — | — | 0.75 1.0 | ns | 1 |
| EC_GTX_CLK125 duty cycle 1000Base-T for RGMII | t_{G125H}/t_{G125} | 47 | — | 53 | % | 2 |
| EC_GTX_CLK125 jitter | — | — | — | ± 150 | ps | 2 |

Notes:

- Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for $LV_{DD} = 2.5$ V and from 0.6 and 2.7 V for $LV_{DD} = 3.3$ V.
- EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 2.11.3.2, "RGMII AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.

2.7.5 DDR Clock Timing

This table provides the system clock (DDRCLK) DC specifications.

Table 15. DDRCLK DC Electrical Characteristics

At recommended operating conditions with $OV_{DD} = 3.3$ V ± 165 mV

| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
|---|----------|------|---------|-----------------|---------|-------|
| Input high voltage | V_{IH} | 2.0 | — | $OV_{DD} + 0.3$ | V | 1 |
| Input low voltage | V_{IL} | -0.3 | — | 0.8 | V | 1 |
| Input capacitance | C_{IN} | — | 7 | 15 | pf | — |
| Input current ($V_{IN} = 0$ V or $V_{IN} = V_{DD}$) | I_{IN} | — | — | ± 50 | μ A | 2 |

Note:

- The symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 2 and Table 3.

Electrical Characteristics

This table provides the DDR clock (DDRCLK) AC timing specification.

Table 16. DDRCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} of 3.3 V \pm 5%.

| Parameter/Condition | Symbol | Min | Typical | Max | Unit | Notes |
|--|----------------------|-------|---------|-----------|------|-------|
| DDRCLK frequency | f_{DDRCLK} | 66.66 | — | 166.7 | MHz | 1, 2 |
| DDRCLK cycle time | t_{DDRCLK} | 6 | — | 15 | ns | 1, 2 |
| DDRCLK duty cycle | t_{KHK}/t_{DDRCLK} | 40 | — | 60 | % | 2 |
| DDRCLK slew rate | — | 1 | — | 4 | V/ns | 3 |
| DDRCLK peak period jitter | — | — | — | ± 150 | ps | — |
| DDRCLK jitter phase noise at -56 dBc | — | — | — | 500 | KHz | 4 |
| AC Input Swing Limits at 3.3 V OV_{DD} | ΔV_{AC} | 1.9 | — | — | V | — |

Notes:

- Caution:** The DDR complex clock to DDRCLK ratio settings must be chosen such that the resulting DDR complex clock frequency does not exceed the maximum or minimum operating frequencies. Refer to *P1020 QorIQ Integrated Processor Reference Manual* for ratio settings.
- Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.
- Slew rate as measured from $\pm 0.3 \Delta V_{AC}$ at center of peak to peak voltage at clock input.
- Phase noise is calculated as FFT of TIE jitter.

2.7.6 Other Input Clocks

A description of the overall clocking of this device is available in the *QorIQ P1020 Integrated Host Processor Family Reference Manual* in the form of a clock subsystem block diagram. For information on the input clocks of other functional blocks of the platform, such as SerDes and eTSEC, see the specific section of this document.

2.8 DDR2 and DDR3 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface. Note that the required $GV_{DD}(\text{typ})$ voltage is 1.8 V or 1.5 V when interfacing to DDR2 or DDR3 SDRAM respectively.

2.8.1 DDR SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR SDRAM component(s) when interfacing to DDR2 SDRAM.

Table 17. DDR2 SDRAM Interface DC Electrical Characteristics

At recommended operating condition with $GV_{DD} = 1.8$ V1

| Parameter | Symbol | Min | Max | Unit | Notes |
|-----------------------|------------|-----------------------|-----------------------|------|---------|
| I/O reference voltage | MV_{REF} | $0.49 \times GV_{DD}$ | $0.51 \times GV_{DD}$ | V | 2, 3, 4 |
| Input high voltage | V_{IH} | $MV_{REF} + 0.125$ | — | V | 5 |
| Input low voltage | V_{IL} | — | $MV_{REF} - 0.125$ | V | 5 |

Table 17. DDR2 SDRAM Interface DC Electrical Characteristics (continued)At recommended operating condition with $GV_{DD} = 1.8\text{ V}$

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|----------|-------|-----|---------------|-------|
| Output high current ($V_{OUT} = 1.37\text{ V}$) | I_{OH} | -13.4 | — | mA | 6 |
| Output low current ($V_{OUT} = 0.330\text{ V}$) | I_{OL} | 13.4 | — | mA | 6 |
| I/O leakage current | I_{OZ} | -50 | 50 | μA | 7 |

Notes:

- GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
- MV_{REF} is expected to be equal to $0.5 \times GV_{DD}$ and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 2\%$ of the DC value.
- V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MV_{REF} with a min value of $MV_{REF} - 0.04$ and a max value of $MV_{REF} + 0.04$. V_{TT} should track variations in the DC level of MV_{REF} .
- The voltage regulator for MV_{REF} must be able to supply up to 1500 μA .
- Input capacitance load for DQ, DQS, and \overline{DQS} are available in the IBIS models.
- Refer to the IBIS model for the complete output IV curve characteristics.
- Output leakage is measured with all outputs disabled, $0\text{ V} \leq V_{OUT} \leq GV_{DD}$.

Electrical Characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Table 18. DDR3 SDRAM Interface DC Electrical Characteristics

At recommended operating condition with $GV_{DD} = 1.5\text{ V}^1$

| Parameter | Symbol | Min | Max | Unit | Note |
|-----------------------|------------|-----------------------|-----------------------|---------------|---------|
| I/O reference voltage | MV_{REF} | $0.49 \times GV_{DD}$ | $0.51 \times GV_{DD}$ | V | 2, 3, 4 |
| Input high voltage | V_{IH} | $MV_{REF} + 0.100$ | GV_{DD} | V | 5 |
| Input low voltage | V_{IL} | GND | $MV_{REF} - 0.100$ | V | 5 |
| I/O leakage current | I_{OZ} | -50 | 50 | μA | 6 |

Notes:

- GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
- MV_{REFn} is expected to be equal to $0.5 \times GV_{DD}$ and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REFn} may not exceed the MV_{REFn} DC level by more than $\pm 1\%$ of GV_{DD} (i.e. $\pm 15\text{ mV}$).
- V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MV_{REFn} with a min value of $MV_{REFn} - 0.04$ and a max value of $MV_{REFn} + 0.04$. V_{TT} should track variations in the DC level of MV_{REFn} .
- The voltage regulator for MV_{REFn} must meet the specifications stated in Table 20.
- Input capacitance load for DQ, DQS, and \overline{DQS} are available in the IBIS models.
- Output leakage is measured with all outputs disabled, $0\text{ V} \leq V_{OUT} \leq GV_{DD}$.

This table provides the DDR controller interface capacitance for DDR2 and DDR3.

Table 19. DDR2 DDR3 SDRAM Capacitance

At recommended operating conditions with GV_{DD} of $1.8\text{ V} \pm 5\%$ for DDR2 or $1.5\text{ V} \pm 5\%$ for DDR3

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|-----------|-----|-----|------|-------|
| Input/output capacitance: DQ, DQS, \overline{DQS} | C_{IO} | 6 | 8 | pF | 1, 2 |
| Delta input/output capacitance: DQ, DQS, \overline{DQS} | C_{DIO} | — | 0.5 | pF | 1, 2 |

Note:

- This parameter is sampled. $GV_{DD} = 1.8\text{ V} \pm 0.1\text{ V}$ (for DDR2), $f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.
- This parameter is sampled. $GV_{DD} = 1.5\text{ V} \pm 0.075\text{ V}$ (for DDR3), $f = 1\text{ MHz}$, $T_A = 25^\circ\text{C}$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.175 V.

This table provides the current draw characteristics for MV_{REF} .

Table 20. Current Draw Characteristics for MV_{REF}

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Max | Unit | Notes |
|--|------------|-----|------|---------------|-------|
| Current draw for DDR2 SDRAM for MV_{REF} | MV_{REF} | — | 1500 | μA | — |
| Current draw for DDR3 SDRAM for MV_{REF} | MV_{REF} | — | 1250 | μA | — |

2.8.2 DDR2 and DDR3 SDRAM Interface AC Timing Specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports both DDR2 and DDR3 memories. Note that the required $GV_{DD}(\text{typ})$ voltage is 1.8 V or 1.5 V when interfacing to DDR2 or DDR3 SDRAM respectively.

2.8.2.1 DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR2 SDRAM.

Table 21. DDR2 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.8 V \pm 5%

| Parameter | | Symbol | Min | Max | Unit | Notes |
|-----------------------|--------------------------|------------|-------------------|-------------------|------|-------|
| AC input low voltage | \geq 667 MHz data rate | V_{ILAC} | — | $MV_{REF} - 0.20$ | V | — |
| | \leq 533 MHz data rate | | — | $MV_{REF} - 0.25$ | | |
| AC input high voltage | \geq 667 MHz data rate | V_{IHAC} | $MV_{REF} + 0.20$ | — | V | — |
| | \leq 533 MHz data rate | | $MV_{REF} + 0.25$ | — | | |

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

Table 22. DDR3 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.5 V \pm 5%

| Parameter | Symbol | Min | Max | Unit | Notes |
|-----------------------|------------|--------------------|--------------------|------|-------|
| AC input low voltage | V_{ILAC} | — | $MV_{REF} - 0.175$ | V | — |
| AC input high voltage | V_{IHAC} | $MV_{REF} + 0.175$ | — | V | — |

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR2 and DDR3 SDRAM.

Table 23. DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.8 V \pm 5% for DDR2 or 1.5 V \pm 5% for DDR3

| Parameter | Symbol | Min | Max | Unit | Notes |
|-----------------------------------|--------------|------|-----|------|-------|
| Controller Skew for MDQS—MDQ/MECC | t_{CISKEW} | — | — | ps | 1 |
| 667 MHz data rate | | –390 | 390 | | |
| 533 MHz data rate | | –450 | 450 | | |
| 400 MHz data rate | | –515 | 515 | | |

Electrical Characteristics

Table 23. DDR2 and DDR3 SDRAM Interface Input AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of 1.8 V \pm 5% for DDR2 or 1.5 V \pm 5% for DDR3

| Parameter | Symbol | Min | Max | Unit | Notes |
|----------------------------------|--------------|------|-----|------|-------|
| Tolerated Skew for MDQS—MDQ/MECC | t_{DISKEW} | — | — | ps | 3 |
| 667 MHz data rate | | -360 | 360 | | |
| 533 MHz data rate | | -488 | 488 | | |
| 400 MHz data rate | | -733 | 733 | | |

Note:

- t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
- DDR3 only.
- The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW} . This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - \text{abs}(t_{CISKEW}))$ where T is the clock period and $\text{abs}(t_{CISKEW})$ is the absolute value of t_{CISKEW} .

This figure shows the DDR2 and DDR3 SDRAM interface input timing diagram.

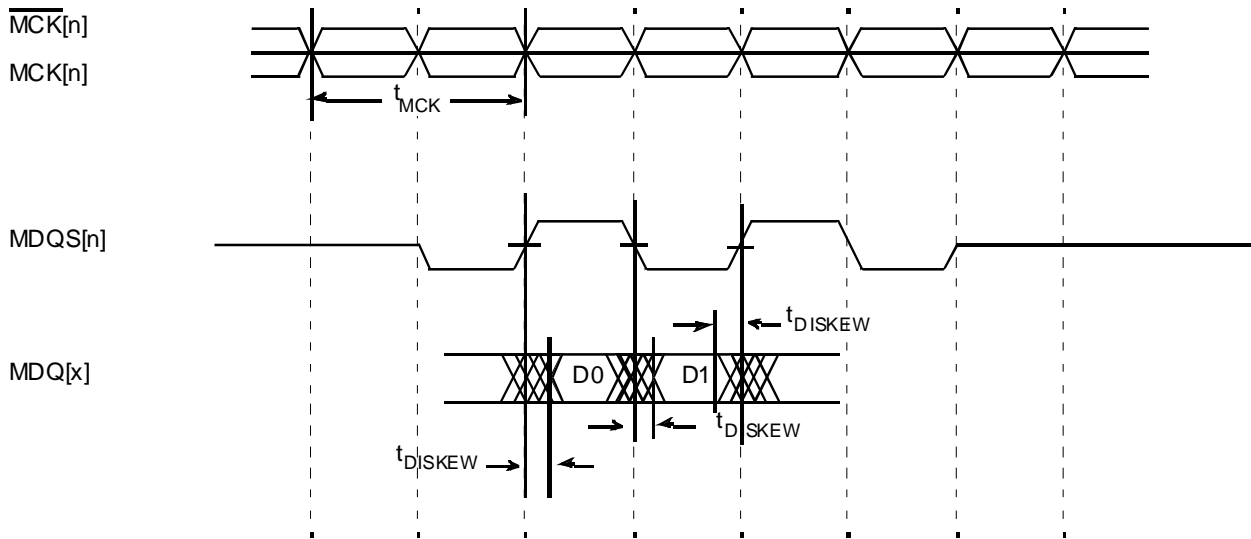


Figure 8. DDR2 and DDR3 SDRAM Interface Input Timing Diagram

2.8.2.2 DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

This table contains the output AC timing targets for the DDR2 and DDR3 SDRAM interface.

Table 24. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.8 V \pm 5% for DDR2 or 1.5 V \pm 5% for DDR3

| Parameter | Symbol ¹ | Min | Max | Unit | Notes |
|-------------------|---------------------|-----|-----|------|-------|
| MCK[n] cycle time | t_{MCK} | 3 | 5 | ns | 2 |

Table 24. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications (continued)At recommended operating conditions with GV_{DD} of 1.8 V \pm 5% for DDR2 or 1.5 V \pm 5% for DDR3

| Parameter | Symbol ¹ | Min | Max | Unit | Notes |
|--|---------------------|--------------------------|------------------|------|-------|
| ADDR/CMD output setup with respect to MCK 667 MHz data rate 533 MHz data rate 400 MHz data rate | t_{DDKHAS} | — .950 1.33 1.8 | — — — — | ns | 3 |
| ADDR/CMD output hold with respect to MCK 667 MHz data rate 533 MHz data rate 400 MHz data rate | t_{DDKHAX} | — .950 1.33 1.8 | — — — — | ns | 3 |
| MCS[n] output setup with respect to MCK 667 MHz data rate 533 MHz data rate 400 MHz data rate | t_{DDKHCS} | — .950 1.33 1.8 | — — — — | ns | 3 |
| MCS[n] output hold with respect to MCK 667 MHz data rate 533 MHz data rate 400 MHz data rate | $t_{DDKH CX}$ | — .950 1.33 1.8 | — — — — | ns | 3 |
| MCK to MDQS Skew \leq 667 MHz data rate | t_{DDKMHM} | — -0.6 | — 0.6 | ns | 4 |

Electrical Characteristics

Table 24. DDR2 and DDR3 SDRAM Interface Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of $1.8\text{ V} \pm 5\%$ for DDR2 or $1.5\text{ V} \pm 5\%$ for DDR3

| Parameter | Symbol ¹ | Min | Max | Unit | Notes |
|--|--------------------------------|----------------------|----------------------|------|-------|
| MDQ/MECC/MDM output setup with respect to MDQS | t_{DDKHDS} , t_{DDKLDS} | — | — | ps | 5 |
| 667 MHz data rate | | 325 | — | | |
| 533 MHz data rate | | 388 | — | | |
| 400 MHz data rate | | 550 | — | | |
| MDQ/MECC/MDM output hold with respect to MDQS | t_{DDKHDX} , t_{DDKLDX} | — | — | ps | 5 |
| 667 MHz data rate | | 325 | — | | |
| 533 MHz data rate | | 388 | — | | |
| 400 MHz data rate | | 550 | — | | |
| MDQS preamble | t_{DDKHMP} | $0.9 \times t_{MCK}$ | — | ns | — |
| MDQS postamble | t_{DDKHME} | $0.4 \times t_{MCK}$ | $0.6 \times t_{MCK}$ | ns | — |

Note:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state}) (\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
- All MCK/MCK and MCDQS/MCDQS referenced measurements are made from the crossing of the two signals.
- ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MECC/MDM/MDQS.
- Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *P1020 QorIQ Integrated Processor Reference Manual* for a description and explanation of the timing modifications enabled by use of these bits.
- Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.

NOTE

For the ADDR/CMD setup and hold specifications in [Table 24](#), it is assumed that the clock control register is set to adjust the memory clocks by $\frac{1}{2}$ applied cycle.

This figure shows the DDR2 and DDR3 SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKMHM}).

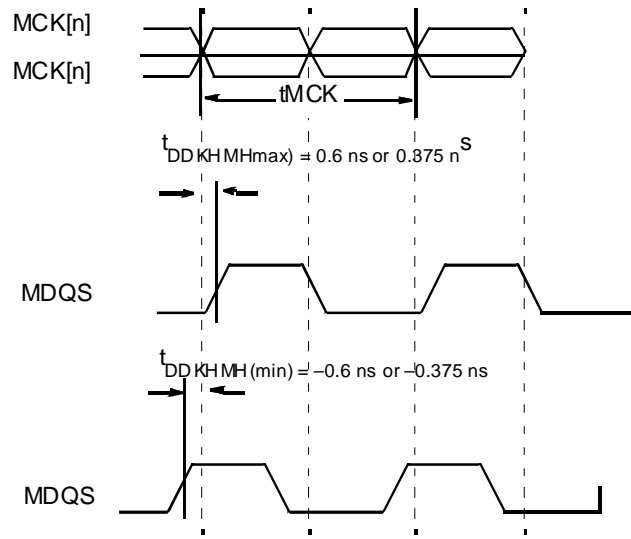


Figure 9. t_{DDKMHM} Timing Diagram

This figure shows the DDR2 and DDR3 SDRAM output timing diagram.

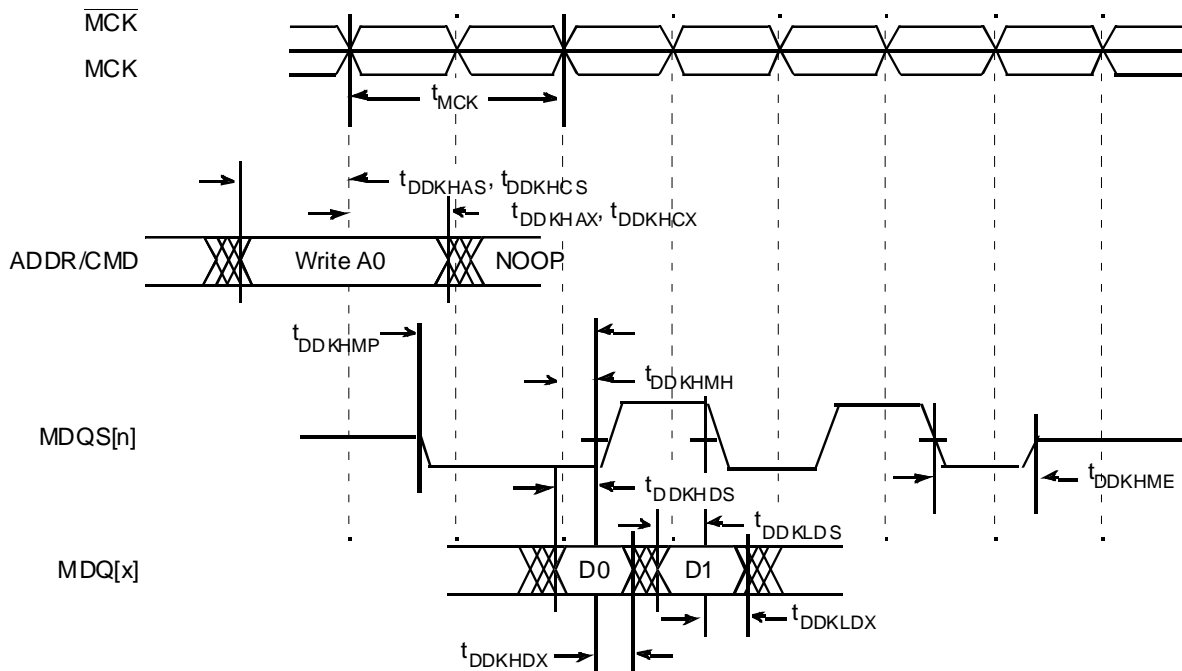


Figure 10. DDR2 and DDR3 Output Timing Diagram

Electrical Characteristics

This figure provides the AC test load for the DDR2 and DDR3 controller bus.

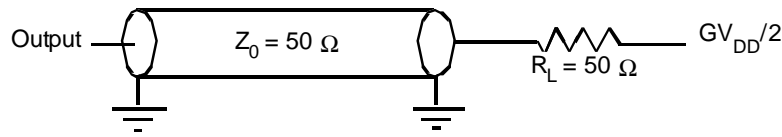


Figure 11. DDR2 and DDR3 Controller Bus AC Test Load

2.8.2.3 DDR2 and DDR3 SDRAM Differential Timing Specifications

This section describes the DC and AC differential timing specifications for the DDR2 and DDR3 SDRAM controller interface.

This figure shows the differential timing specification.

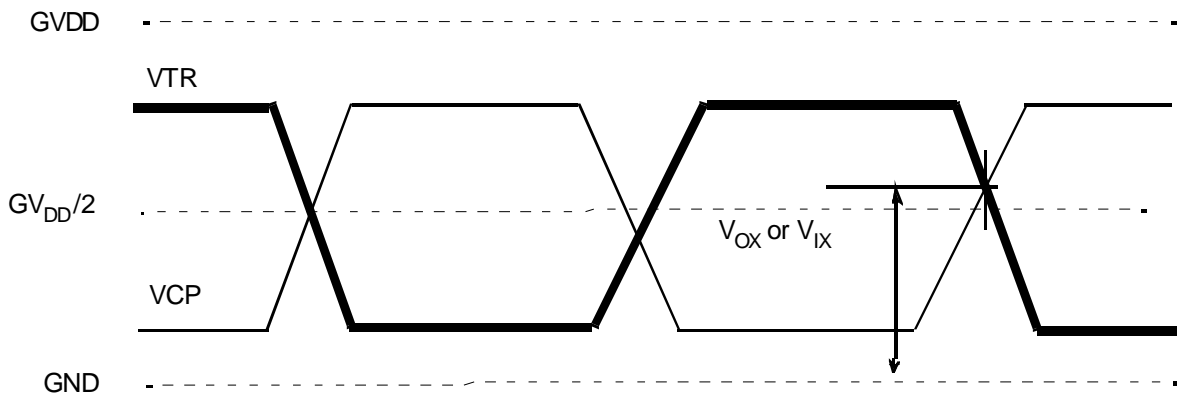


Figure 12. DDR2 and DDR3 SDRAM Differential Timing Specifications

NOTE

VTR specifies the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as $\overline{\text{MCK}}$ or $\overline{\text{MDQS}}$).

This table provides the DDR2 differential specifications for the differential signals MDQS/ $\overline{\text{MDQS}}$ and MCK/ $\overline{\text{MCK}}$.

Table 25. DDR2 SDRAM Differential Electrical Characteristics

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|------------|------------------------------|------------------------------|------|-------|
| Input AC Differential Crosspoint Voltage | V_{IXAC} | $0.5 \times GV_{DD} - 0.175$ | $0.5 \times GV_{DD} + 0.175$ | V | — |
| Output AC Differential Crosspoint Voltage | V_{OXAC} | $0.5 \times GV_{DD} - 0.125$ | $0.5 \times GV_{DD} + 0.125$ | V | — |

This table provides the DDR3 differential specifications for the differential signals MDQS/ $\overline{\text{MDQS}}$ and MCK/ $\overline{\text{MCK}}$.

Table 26. DDR3 SDRAM Differential Electrical Characteristics

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|------------|------------------------------|------------------------------|------|-------|
| Input AC Differential Crosspoint Voltage | V_{IXAC} | $0.5 \times GV_{DD} - 0.150$ | $0.5 \times GV_{DD} + 0.150$ | V | — |
| Output AC Differential Crosspoint Voltage | V_{OXAC} | $0.5 \times GV_{DD} - 0.115$ | $0.5 \times GV_{DD} + 0.115$ | V | — |

2.9 eSPI

This section describes the DC and AC electrical specifications for the SPI interface.

2.9.1 eSPI DC Electrical Characteristics

This table provides the DC electrical characteristics for eSPI interface at $CV_{DD} = 3.3$ V.

Table 27. SPI DC Electrical Characteristics (3.3V)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Note |
|---|----------|-----|----------|---------------|------|
| Input high voltage | V_{IH} | 2.0 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.8 | V | 1 |
| Input current ($0\text{ V} \leq V_{IN} \leq CV_{DD}$) | I_{IN} | — | ± 50 | μA | 2 |
| Output high voltage ($I_{OH} = -6.0\text{ mA}$) | V_{OH} | 2.4 | — | V | — |
| Output low voltage ($I_{OL} = 6.0\text{ mA}$) | V_{OL} | — | 0.5 | V | — |
| Output low voltage ($I_{OL} = 3.2\text{ mA}$) | V_{OL} | — | 0.4 | V | — |

Note:

- Note that the min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in [Table 3](#).
- Note that the symbol V_{IN} , in this case, represents the CV_{IN} symbol referenced in [Section 2.1.2, "Recommended Operating Conditions."](#)

This table provides the DC electrical characteristics for the eSPI interface operating at $CV_{DD} = 2.5$ V.

Table 28. SPI DC Electrical Characteristics (2.5 V)

| Parameter | Symbol | Min | Max | Unit | Note |
|--|----------|-----|----------|---------------|------|
| High-level input voltage | V_{IH} | 1.7 | — | V | 1 |
| Low-level input voltage | V_{IL} | — | 0.7 | V | 1 |
| Input current ($V_{IN} = 0\text{ V}$ or $V_{IN} = CV_{DD}$) | I_{IN} | — | ± 40 | μA | 2 |
| High-level output voltage ($CV_{DD} = \text{min}$, $I_{OH} = -1\text{ mA}$) | V_{OH} | 2.0 | — | V | — |
| Low-level output voltage ($CV_{DD} = \text{min}$, $I_{OL} = 1\text{ mA}$) | V_{OL} | — | 0.4 | V | — |

Note:

- The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in [Table 3](#).
- The symbol V_{IN} , in this case, represents the CV_{IN} symbol referenced in [Section 2.1.2, "Recommended Operating Conditions."](#)

This table provides the DC electrical characteristics for the eSPI interface operating at $CV_{DD} = 1.8$ V.

Table 29. SPI DC Electrical Characteristics (1.8 V)

| Parameter | Symbol | Min | Max | Unit | Note |
|--------------------------|----------|------|-----|------|------|
| High-level input voltage | V_{IH} | 1.25 | — | V | 1 |
| Low-level input voltage | V_{IL} | — | 0.6 | V | 1 |

Electrical Characteristics

Table 29. SPI DC Electrical Characteristics (1.8 V) (continued)

| Parameter | Symbol | Min | Max | Unit | Note |
|--|----------|------|----------|---------------|------|
| Input current ($V_{IN} = 0\text{ V}$ or $V_{IN} = CV_{DD}$) | I_{IN} | — | ± 40 | μA | 2 |
| High-level output voltage ($CV_{DD} = \text{min}$, $I_{OH} = -0.5\text{ mA}$) | V_{OH} | 1.35 | — | V | — |
| Low-level output voltage ($CV_{DD} = \text{min}$, $I_{OL} = 0.5\text{ mA}$) | V_{OL} | — | 0.4 | V | — |

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN} , in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

2.9.2 eSPI AC Timing Specifications

This table provides the SPI input and output AC timing specifications.

Table 30. SPI AC Timing Specifications¹

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Max | Unit | Note |
|--|---------------|---|---|------|------|
| SPI outputs—Master data (internal clock) hold time | t_{NIKH0X} | $0.5+(t_{PLAT}$ FOR M_CLK *SPMODE [HO _ADJ]) | — | ns | 2, 3 |
| SPI outputs—Master data (internal clock) delay | t_{NIKH0V} | — | $5.5+(t_{PLAT}$ FORM _CLK *SPMODE [HO_ ADJ]) | ns | 2, 3 |
| SPI_CS outputs—Master data (internal clock) hold time | $t_{NIKH0X2}$ | 0 | — | ns | 2 |
| SPI_CS outputs—Master data (internal clock) delay | $t_{NIKH0V2}$ | — | 6.0 | ns | 2 |
| SPI inputs—Master data (internal clock) input setup time | t_{NIIVKH} | 5 | — | ns | — |
| SPI inputs—Master data (internal clock) input hold time | t_{NIIXKH} | 0 | — | ns | — |

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state}) (\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{NIKH0V} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
3. See the *P1020 QorIQ Integrated Processor Reference Manual* for detail about the register SPMODE

This figure provides the AC test load for the SPI.

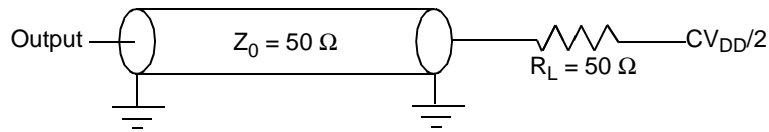


Figure 13. SPI AC Test Load

This figure represents the AC timing from Table 30 in master mode (internal clock). Note that although the specifications are generally refer to the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge. Also, note that the clock edge is selectable on SPI.

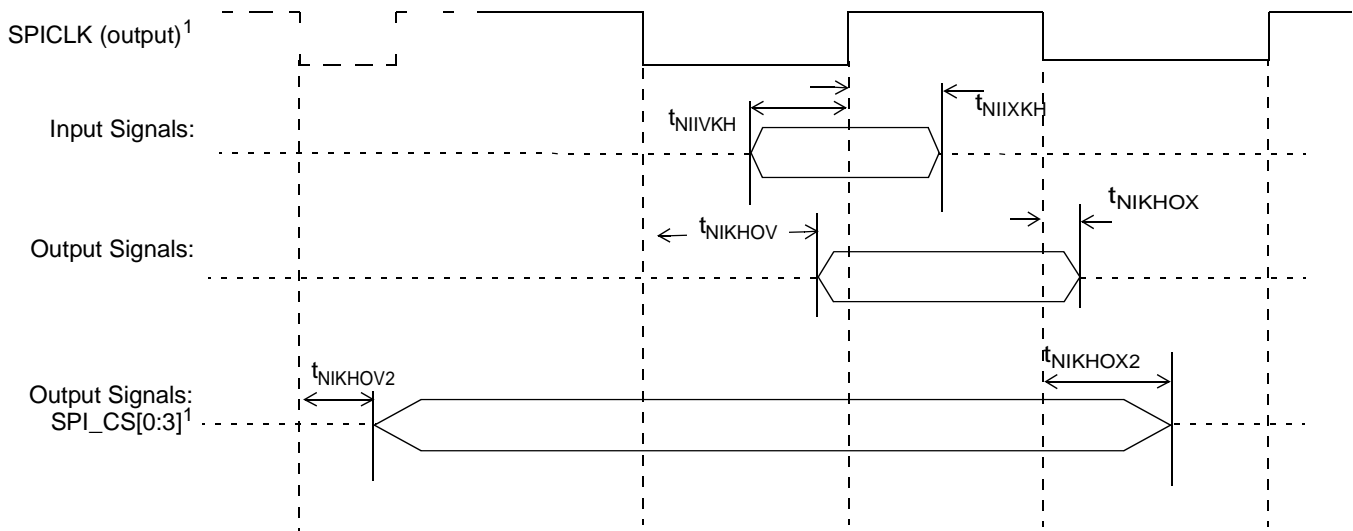


Figure 14. SPI AC Timing in Master Mode (Internal Clock) Diagram

2.10 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

2.10.1 DUART DC Electrical Characteristics

This table provides the DC electrical characteristics for the DUART interface.

Table 31. DUART DC Electrical Characteristics

For recommended operating conditions, see Table 3

| Parameter | Symbol | Min | Max | Unit | Notes |
|--|----------|-----|----------|---------------|-------|
| Input high voltage | V_{IH} | 2 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.8 | V | 1 |
| Input current ($OV_{IN} = 0\text{ V}$ or $OV_{IN} = OV_{DD}$) | I_{IN} | — | ± 50 | μA | 2 |
| Output high voltage ($OV_{DD} = mn$, $I_{OH} = -2\text{ mA}$) | V_{OH} | 2.4 | — | V | — |

Electrical Characteristics

Table 31. DUART DC Electrical Characteristics

For recommended operating conditions, see [Table 3](#)

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|----------|-----|-----|------|-------|
| Output low voltage ($OV_{DD} = \text{min}$, $I_{OL} = 2 \text{ mA}$) | V_{OL} | — | 0.4 | V | — |

Note:

- Note that the min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in [Figure 3](#).
- Note that the symbol OV_{IN} represents the input voltage of the supply. It is referenced in [Figure 3](#).

2.10.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 32. DUART AC Timing Specifications

| Parameter | Value | Unit | Notes |
|-------------------|---------------------|------|-------|
| Minimum baud rate | CCB clock/1,048,576 | baud | 1 |
| Maximum baud rate | CCB clock/16 | baud | 2 |
| Oversample rate | 16 | — | 3 |

Notes:

- CCB clock refers to the platform clock.
- Actual attainable baud rate will be limited by the latency of interrupt processing.
- The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

2.11 Ethernet: Enhanced Three-Speed Ethernet (eTSEC) (10/100/1000 Mbps)—MII/RMII/RGMII/SGMII Electrical Characteristics

This section provides the AC and DC electrical characteristics for enhanced three-speed Ethernet 10/100/1000 controller and MII management.

2.11.1 MII Interface Electrical Specifications

This section provides AC and DC electrical characteristics of MII interface for eTSEC.

2.11.1.1 MII and RMII DC Electrical Characteristics

All MII drivers and receivers comply with the DC parametric attributes specified in this table.

Table 33. MII and RMII DC Electrical Characteristics

At recommended operating conditions with $LV_{DD} = 3.3\text{ V}$

| Parameter | Symbol | Min | Max | Unit | Notes |
|--|----------|-----|-----|---------------|-------|
| Input high voltage | V_{IH} | 2.0 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.8 | V | — |
| Input high current ($V_{IN} = LV_{DD}$) | I_{IH} | — | 50 | μA | 2 |
| Input low current ($V_{IN} = \text{GND}$) | I_{IL} | -50 | — | μA | 2 |
| Output high voltage ($LV_{DD} = \text{min}$, $I_{OH} = -4.0\text{ mA}$) | V_{OH} | 2.4 | — | V | — |
| Output low voltage ($LV_{DD} = \text{min}$, $I_{OL} = 4.0\text{ mA}$) | V_{OL} | — | 0.4 | V | — |

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in [Table 3](#).
2. The symbol V_{IN} , in this case, represents the LV_{IN} symbols referenced in [Table 2](#) and [Table 3](#).

2.11.1.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

2.11.1.2.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

Table 34. MII Transmit AC Timing Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|--------------------|--------|-----|--------|------|
| TX_CLK clock period 10 Mbps | t_{MTX} | 399.96 | 400 | 400.04 | ns |
| TX_CLK clock period 100 Mbps | t_{MTX} | 39.996 | 40 | 40.004 | ns |
| TX_CLK duty cycle | t_{MTXH}/t_{MTX} | 35 | — | 65 | % |
| TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay | t_{MTKHDX} | 1 | 5 | 15 | ns |
| TX_CLK data clock rise (20%–80%) | t_{MTXR} | 1.0 | — | 4.0 | ns |
| TX_CLK data clock fall (80%–20%) | t_{MTXF} | 1.0 | — | 4.0 | ns |

This figure shows the MII transmit AC timing diagram.

Electrical Characteristics

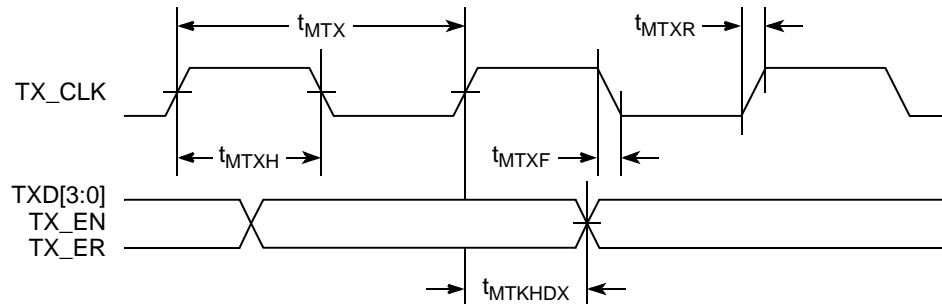


Figure 15. MII Transmit AC Timing Diagram

2.11.1.2.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

Table 35. MII Receive AC Timing Specifications

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|--------------------|--------|-----|--------|------|
| RX_CLK clock period 10 Mbps | t_{MRX} | 399.96 | 400 | 400.04 | ns |
| RX_CLK clock period 100 Mbps | t_{MRX} | 39.996 | 40 | 40.004 | ns |
| RX_CLK duty cycle | t_{MRXH}/t_{MRX} | 35 | — | 65 | % |
| RXD[3:0], RX_DV, RX_ER setup time to RX_CLK | t_{MRDVKH} | 10.0 | — | — | ns |
| RXD[3:0], RX_DV, RX_ER hold time to RX_CLK | t_{MRDXKH} | 10.0 | — | — | ns |
| RX_CLK clock rise (20%–80%) | t_{MRXR} | 1.0 | — | 4.0 | ns |
| RX_CLK clock fall time (80%–20%) | t_{MRXF} | 1.0 | — | 4.0 | ns |

Note: The frequency of RX_CLK should not exceed the frequency of TX_CLK by more than 300 ppm.

This figure provides the AC test load for eTSEC.

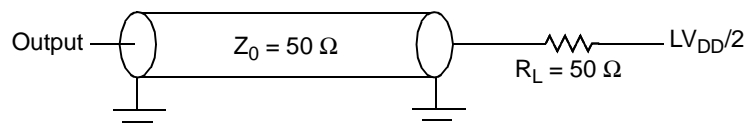


Figure 16. eTSEC AC Test Load

This figure shows the MII receive AC timing diagram.

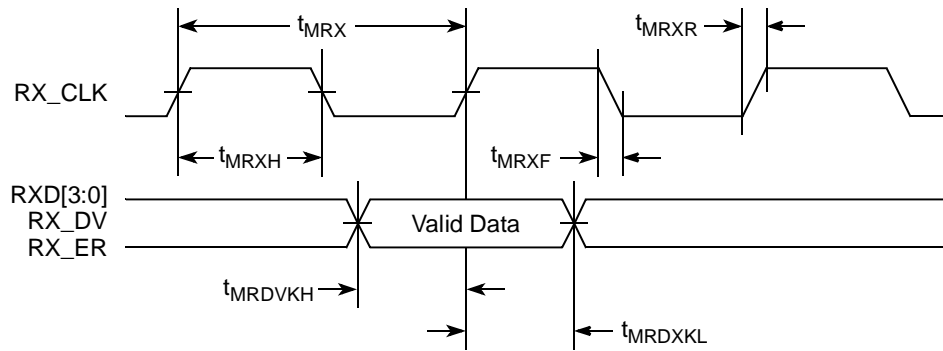


Figure 17. MII Receive AC Timing Diagram

2.11.2 RMII AC Timing Specifications

In RMII mode, the reference clock should be fed to TSEC_n_TX_CLK. This section describes the RMII transmit and receive AC timing specifications.

This table lists the RMII transmit AC timing specifications.

Table 36. RMII Transmit AC Timing Specifications

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|-------------|-----|------|------|------|
| TSEC _n _TX_CLK clock period | t_{RMT} | — | 20.0 | — | ns |
| TSEC _n _TX_CLK duty cycle | t_{RMTH} | 35 | — | 65 | % |
| TSEC _n _TX_CLK peak-to-peak jitter | t_{RMTJ} | — | — | 250 | ps |
| Rise time TSEC _n _TX_CLK (20%–80%) | t_{RMTR} | 1.0 | — | 5.0 | ns |
| Fall time TSEC _n _TX_CLK (80%–20%) | t_{RMTF} | 1.0 | — | 5.0 | ns |
| TSEC _n _TX_CLK to RMII data TXD[1:0], TX_EN delay | t_{RMTDX} | 2.0 | — | 10.0 | ns |

This figure shows the RMII transmit AC timing diagram.

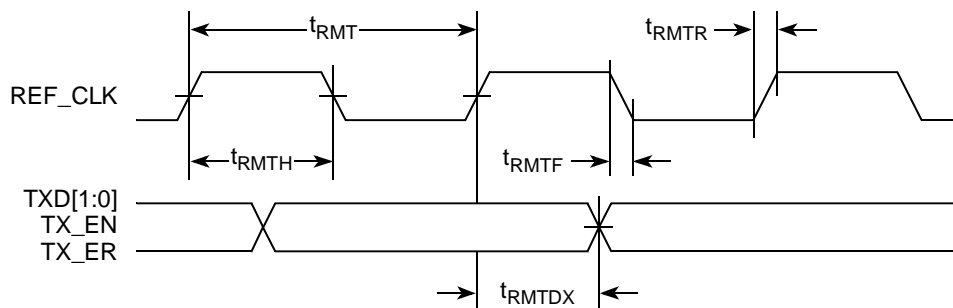


Figure 18. RMII Transmit AC Timing Diagram

Electrical Characteristics

This table lists the RMI receive AC timing specifications.

Table 37. RMI Receive AC Timing Specifications

For recommended operating conditions, see [Table 3](#)

| Parameter | Symbol | Min | Typ | Max | Unit |
|--|-------------|-----|------|-----|------|
| TSEcn_TX_CLK clock period | t_{RMR} | — | 20.0 | — | ns |
| TSEcn_TX_CLK duty cycle | t_{RMRH} | 35 | — | 65 | % |
| TSEcn_TX_CLK peak-to-peak jitter | t_{RMRJ} | — | — | 250 | ps |
| Rise time TSEcn_TX_CLK (20%–80%) | t_{RMRR} | 1.0 | — | 5.0 | ns |
| Fall time TSEcn_TX_CLK (80%–20%) | t_{RMRF} | 1.0 | — | 5.0 | ns |
| RXD[1:0], CRS_DV, RX_ER setup time to TSEcn_TX_CLK rising edge | t_{RMRDV} | 4.0 | — | — | ns |
| RXD[1:0], CRS_DV, RX_ER hold time to TSEcn_TX_CLK rising edge | t_{RMRDX} | 2.0 | — | — | ns |

This figure provides the AC test load for eTSEC.

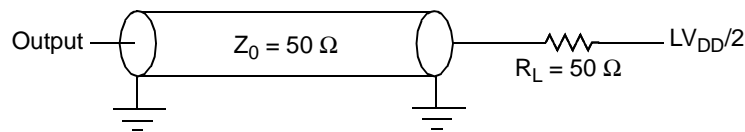


Figure 19. eTSEC AC Test Load

This figure shows the RMI receive AC timing diagram.

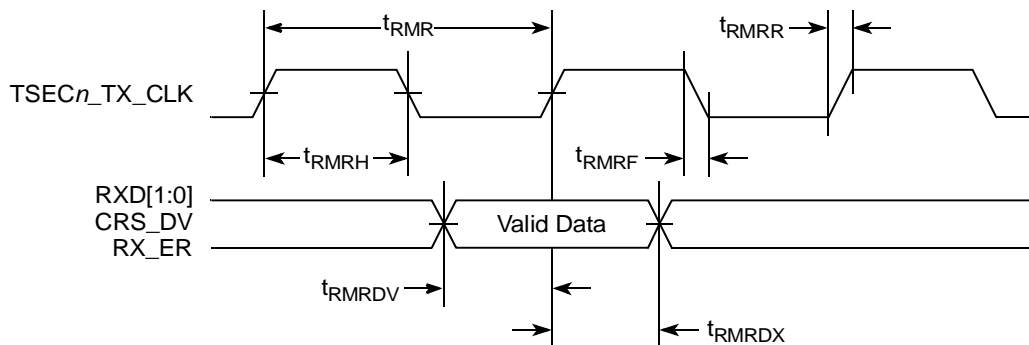


Figure 20. RMI Receive AC Timing Diagram

2.11.3 RGMII Interface Electrical Specifications

This section provides AC and DC electrical characteristics of RGMII interface for eTSEC.

2.11.3.1 RGMII DC Electrical Characteristics

This table shows the RGMII DC electrical characteristics when operating from a 2.5 V supply.

Table 38. RGMII DC Electrical Characteristics (2.5V)

At recommended operating conditions with $LV_{DD} = 2.5\text{ V}$

| Parameter | Symbol | Min | Max | Unit | Notes |
|--|----------|--------------------|-----------------|---------------|-------|
| Input high voltage | V_{IH} | 1.70 | — | V | — |
| Input low voltage | V_{IL} | — | 0.70 | V | — |
| Input high current ($V_{IN} = LV_{DD}$) | I_{IH} | — | 50 | μA | — |
| Input low current ($V_{IN} = \text{GND}$) | I_{IL} | -50 | — | μA | 2 |
| Output high voltage ($LV_{DD} = \text{min}$, $I_{OH} = -1.0\text{ mA}$) | V_{OH} | 2.00 | $LV_{DD} + 0.3$ | V | — |
| Output low voltage ($LV_{DD} = \text{min}$, $I_{OL} = 1.0\text{ mA}$) | V_{OL} | $\text{GND} - 0.3$ | 0.40 | V | — |

Note:

- Note that the min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in [Table 3](#).
- The symbol V_{IN} , in this case, represents the LV_{IN} symbols referenced in [Table 3](#).

2.11.3.2 RGMII AC Timing Specifications

This table presents the RGMII AC timing specifications.

Table 39. RGMII AC Timing Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol ¹ | Min | Typ | Max | Unit | Notes |
|--|---------------------|------|-----|-----|------|-------|
| Data to clock output skew (at transmitter) | t_{SKRGT_TX} | -500 | 0 | 500 | ps | 5 |
| Data to clock input skew (at receiver) | t_{SKRGT_RX} | 1.0 | — | 2.6 | ns | 2 |
| Clock period duration | t_{RGT} | 7.2 | 8.0 | 8.8 | ns | 3 |
| Duty cycle for 10BASE-T and 100BASE-TX | t_{RGTH}/t_{RGT} | 40 | 50 | 60 | % | 3, 4 |

Electrical Characteristics

Table 39. RGMII AC Timing Specifications (continued)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol ¹ | Min | Typ | Max | Unit | Notes |
|------------------------|---------------------|-----|-----|------|------|-------|
| Duty cycle for Gigabit | t_{RGTH}/t_{RGT} | 45 | 50 | 55 | % | — |
| Rise time (20%–80%) | t_{RGTR} | — | — | 0.75 | ns | — |
| Fall time (20%–80%) | t_{RGTF} | — | — | 0.75 | ns | — |

Notes:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. For example, the subscript of t_{RGT} represents the RGMII receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their chip. If so, additional PCB delay is probably not needed.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. The frequency of RX_CLK should not exceed the frequency of GTX_CLK125 by more than 300 ppm.

This figure shows the RGMII AC timing and multiplexing diagrams.

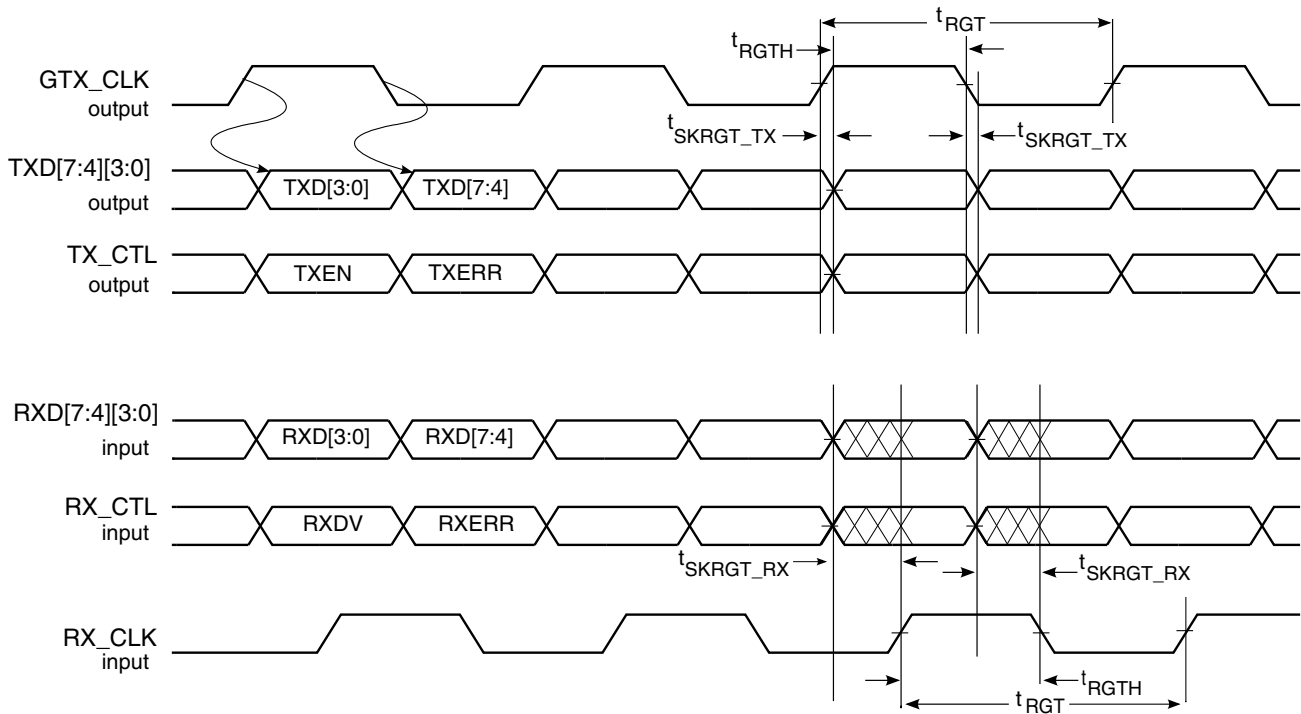


Figure 21. RGMII AC Timing and Multiplexing Diagrams

2.11.4 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-Coupled serial link from the dedicated SerDes interface of P1011 as shown in [Figure 23](#), where C_{TX} is the external (on board) AC-Coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to SGND_SRDS. The reference circuit of the SerDes transmitter and receiver is shown in [Figure 52](#).

2.11.4.1 SGMII DC Electrical Characteristics

This section discusses the electrical characteristics for the SGMII interface.

2.11.4.1.1 DC Requirements for SGMII SD_REF_CLK and SD_REF_CLK

The characteristics and DC requirements of the separate SerDes reference clock are described in [Section 2.20.2.2, “DC Level Requirement for SerDes Reference Clocks.”](#)

2.11.4.1.2 SGMII Transmit DC Timing Specifications

This table describe the SGMII SerDes transmitter AC-Coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs ($SDn_TX[n]$ and $\overline{SDn_TX}[n]$) as shown in [Figure 23](#).

Table 40. SGMII DC Transmitter Electrical Characteristics

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|--|------------|--|-----|--|------|-----------------------------|
| Output high voltage | V_{OH} | — | — | $XV_{DD_SRDS2-Typ}/2 + V_{OD} _{-max}/2$ | mV | 1 |
| Output low voltage | V_{OL} | $XV_{DD_SRDS2-Typ}/2 - V_{OD} _{-max}/2$ | — | — | mV | 1 |
| Output differential voltage ^{2, 3, 4} (XV_{DD-Typ} at 1.0V) | $ V_{OD} $ | 304 | 475 | 689 | mV | Equalization setting: 1.0x |
| | | 279 | 436 | 632 | | Equalization setting: 1.09x |
| | | 254 | 396 | 574 | | Equalization setting: 1.2x |
| | | 229 | 357 | 518 | | Equalization setting: 1.33x |
| | | 202 | 316 | 459 | | Equalization setting: 1.5x |
| | | 178 | 277 | 402 | | Equalization setting: 1.71x |
| | | 152 | 237 | 344 | | Equalization setting: 2.0x |
| Output impedance (single-ended) | R_O | 40 | 50 | 60 | Ω | — |

Note:

- This will not align to DC-coupled SGMII.
- $|V_{OD}| = |V_{SD2_TXn} - V_{\overline{SD2_TXn}}|$. $|V_{OD}|$ is also referred as output differential peak voltage. $V_{TX-DIFFp-p} = 2 * |V_{OD}|$.
- The $|V_{OD}|$ value shown in the table assumes the following transmit equalization setting in the XMITEQAB (for SerDes lanes A & B) or XMITEQEF (for SerDes lanes E & E) bit field of the SerDes 2 control register:
 - The MSbit (bit 0) of the above bit field is set to zero (selecting the full $V_{DD-DIFF-p-p}$ amplitude - power up default);
 - The LSbits (bit [1:3]) of the above bit field is set based on the equalization setting shown in table.
- The $|V_{OD}|$ value shown in the Typ column is based on the condition of $XV_{DD_SRDS2-Typ}=1.0$ V, no common mode offset variation, SerDes transmitter is terminated with 100-Ω differential load between $SD_TX[n]$ and $\overline{SD_TX}[n]$.

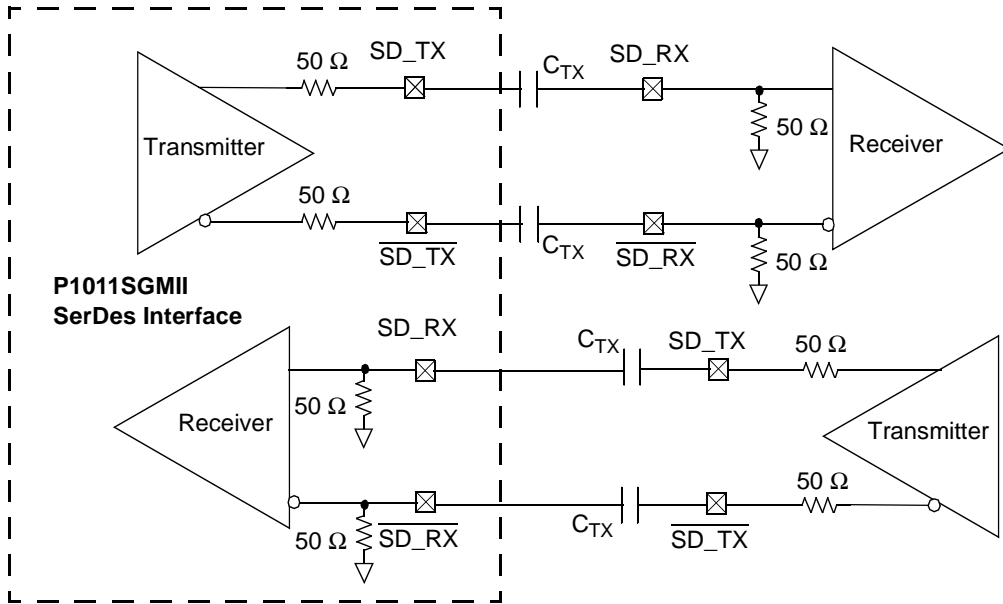


Figure 22. 4-Wire AC-Coupled SGMII Serial Link Connection Example

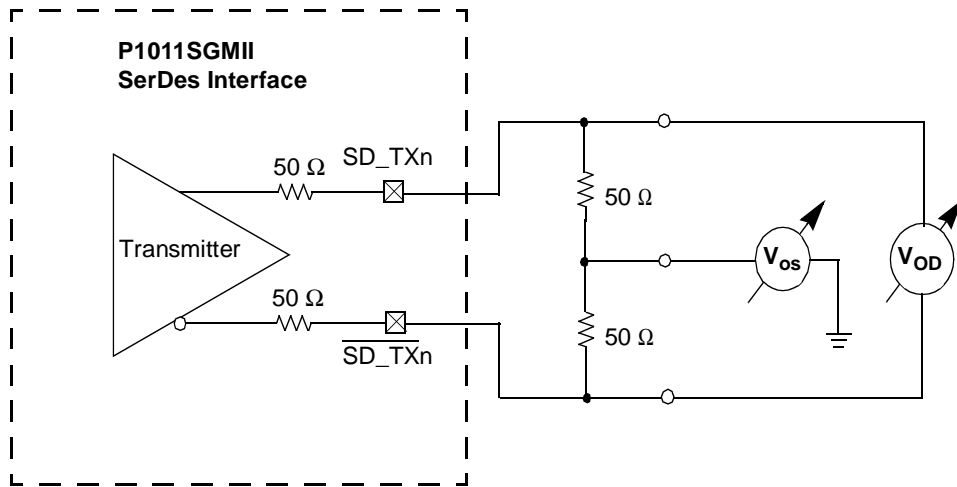


Figure 23. SGMII Transmitter DC Measurement Circuit

2.11.4.1.3 SGMII DC Receiver Timing Specification

This table lists the SGMII DC receiver electrical characteristics. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 41. SGMII DC Receiver Electrical Characteristics⁵

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit | Notes | |
|---------------------------------------|----------------|-------------------|-----|-----|----------|-------|------|
| DC Input voltage range | — | N/A | | | — | 1 | |
| Input differential voltage | LSTS = 001 | $V_{RX_DIFFp-p}$ | 100 | — | 1200 | mV | 2, 4 |
| | LSTS = 100 | | 175 | — | | | |
| Loss of signal threshold | LSTS = 001 | VLOS | 30 | — | 100 | mV | 3, 4 |
| | LSTS = 100 | | 65 | — | 175 | | |
| Receiver differential input impedance | Z_{RX_DIFF} | 80 | — | 120 | Ω | — | |

Note:

1. Input must be externally AC-coupled.
2. $V_{RX_DIFFp-p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in PCI Express. Refer to the PCI Express Differential Receiver (RX) Input Specifications section for further explanation.
4. The LSTS shown in the table refers to the EIC2[0:2] or EIC3[0:2] bit field of the GUTS_SRDSR4 register, depending on the SerDes lane usage

2.11.4.2 SGMII AC Timing Specifications

This section describes the AC timing specifications for the SGMII interface.

2.11.4.2.1 AC Requirements for SGMII $\overline{SD_REF_CLK}$ and $\overline{SD_REF_CLK}$

Note that the SGMII clock requirements for $\overline{SD_REF_CLK}$ and $\overline{SD_REF_CLK}$ are intended to be used within the clocking guidelines specified by [Section 2.20.2.3](#), “AC Requirements for SerDes Reference Clocks.”

2.11.4.2.2 SGMII Transmit AC Timing Specifications

This table provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 42. SGMII Transmit AC Timing Specifications

At recommended operating conditions with $XV_{DD_SRDS} = 1.0\text{ V} \pm 50\text{ mV}$

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|----------------------|--------|--------|-----|--------|--------|-------|
| Deterministic Jitter | JD | — | — | 0.17 | UI p-p | — |
| Total Jitter | JT | — | — | 0.35 | UI p-p | — |
| Unit Interval | UI | 799.92 | 800 | 800.08 | ps | — |

Electrical Characteristics

Table 42. SGMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with $XV_{DD_SRDS} = 1.0\text{ V} \pm 50\text{ mV}$

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|-----------------------|----------|-----|-----|-----|------|-------|
| AC coupling capacitor | C_{TX} | 10 | — | 200 | nF | 3 |

Notes:

- Each UI is $800\text{ ps} \pm 100\text{ ppm}$.
- See Figure 25 for single frequency sinusoidal jitter limits.
- The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.

2.11.4.2.3 SGMII AC Measurement details

Transmitter and receiver AC characteristics are measured at the transmitter outputs ($SD_TX[n]$ and $\overline{SD_TX}[n]$) or at the receiver inputs ($SD_RX[n]$ and $\overline{SD_RX}[n]$) as depicted in this figure, respectively.

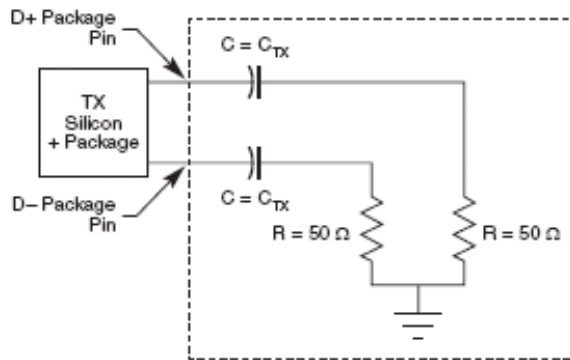


Figure 24. SGMII AC Test/Measurement Load

2.11.4.2.4 SGMII Receiver AC Timing Specifications

This table provides the SGMII receive AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 43. SGMII Receive AC Timing Specifications

At recommended operating conditions with $XV_{DD_SRDS2} = 1.0\text{ V} \pm 50\text{ mV}$

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|--|--------|--------|-----|------------|--------|-------|
| Deterministic Jitter Tolerance | JD | 0.37 | — | — | UI p-p | 1, 2 |
| Combined Deterministic and Random Jitter Tolerance | JDR | 0.55 | — | — | UI p-p | 1, 2 |
| Total Jitter Tolerance | JT | 0.65 | — | — | UI p-p | 1, 2 |
| Bit Error Ratio | BER | — | — | 10^{-12} | | — |
| Unit Interval | UI | 799.92 | 800 | 800.08 | ps | 3 |

Notes:

- Measured at receiver.
- Refer to RapidIO™ 1×/4× LP Serial Physical Layer Specification for interpretation of jitter specifications.
- Each UI is $800\text{ ps} \pm 100\text{ ppm}$.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of this figure.

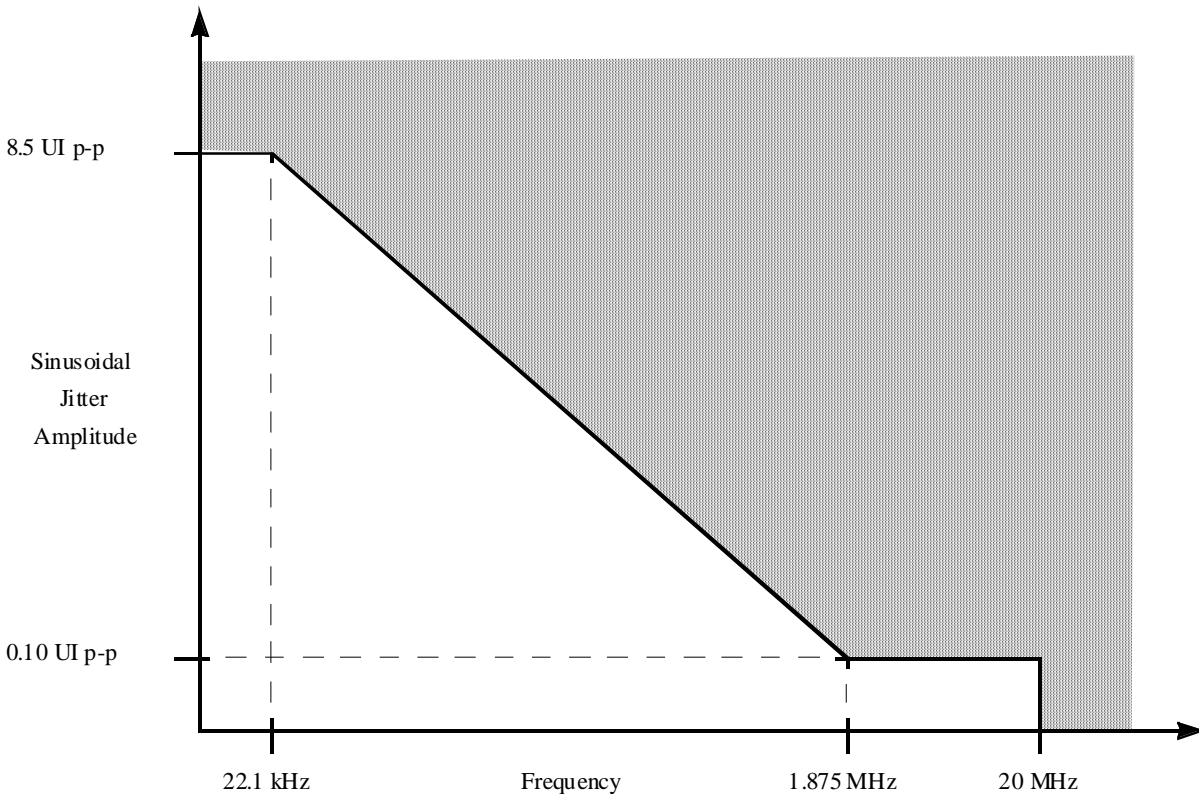


Figure 25. Single Frequency Sinusoidal Jitter Limits

2.11.5 MII Management

2.11.5.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V and 2.5 V. The DC electrical characteristics for MDIO and MDC are provided in the following tables.

Table 44. MII Management DC Electrical Characteristics

At recommended operating conditions with $LV_{DD} = 3.3\text{ V}$

| Parameter | Symbol | Min | Max | Unit | Notes |
|--|----------|-----|-----------------|---------------|-------|
| Input high voltage | V_{IH} | 2.0 | — | V | — |
| Input low voltage | V_{IL} | — | 0.90 | V | — |
| Input high current ($LV_{DD} = \text{Max}$, $V_{IN} = 2.1\text{ V}$) | I_{IH} | — | 50 | μA | 1 |
| Input low current ($LV_{DD} = \text{Max}$, $V_{IN} = 0.5\text{ V}$) | I_{IL} | -50 | — | μA | 1 |
| Output high voltage ($LV_{DD} = \text{Min}$, $I_{OH} = -1.0\text{ mA}$) | V_{OH} | 2.4 | $LV_{DD} + 0.3$ | V | — |

Electrical Characteristics

Table 44. MII Management DC Electrical Characteristics (continued)

At recommended operating conditions with $LV_{DD} = 3.3\text{ V}$

| Parameter | Symbol | Min | Max | Unit | Notes |
|--|----------|-----|-----|------|-------|
| Output low voltage ($LV_{DD} = \text{Min}$, $I_{OL} = 1.0\text{ mA}$) | V_{OL} | GND | 0.4 | V | — |

Note:

- Note that the symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in [Table 2](#) and [Table 3](#).

Table 45. MII Management DC Electrical Characteristics

At recommended operating conditions with $LV_{DD} = 2.5\text{ V}$

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|----------|--------------------|-----------------|---------------|-------|
| Input high voltage | V_{IH} | 1.70 | $LV_{DD} + 0.3$ | V | — |
| Input low voltage | V_{IL} | -0.3 | 0.70 | V | — |
| Input high current ($V_{IN} = LV_{DD}$) | I_{IH} | — | 50 | μA | 1, 2 |
| Input low current ($V_{IN} = \text{GND}$) | I_{IL} | -50 | — | μA | — |
| Output high voltage ($LV_{DD} = \text{Min}$, $I_{OH} = -1.0\text{ mA}$) | V_{OH} | 2.00 | $LV_{DD} + 0.3$ | V | — |
| Output low voltage ($LV_{DD} = \text{Min}$, $I_{OL} = 1.0\text{ mA}$) | V_{OL} | $\text{GND} - 0.3$ | 0.40 | V | — |

Notes:

- EC1_MDC and EC1_MDIO operate on LV_{DD} .
- Note that the symbol V_{IN} , in this case, represents the LV_{IN} and TV_{IN} symbols referenced in [Table 3](#).

2.11.5.1.1 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 46. MII Management AC Timing Specifications

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|----------------------------|--------------|-------------------------------|-----|-------------------------------|------|-------|
| MDC frequency | f_{MDC} | — | 2.5 | — | MHz | 2 |
| MDC period | t_{MDC} | — | 400 | — | ns | — |
| MDC clock pulse width high | t_{MDCH} | 32 | — | — | ns | — |
| MDC to MDIO delay | t_{MDKHDX} | $(16 \cdot t_{plb_clk}) - 3$ | — | $(16 \cdot t_{plb_clk}) + 3$ | ns | 3, 4 |
| MDIO to MDC setup time | t_{MDDVKH} | 5 | — | — | ns | — |

Table 46. MII Management AC Timing Specifications (continued)

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|-----------------------|--------------|-----|-----|-----|------|-------|
| MDIO to MDC hold time | t_{MDDXKH} | 0 | — | — | ns | — |

Notes:

- The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
- This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ± 3 ns. For example, with a platform clock of 333 MHz, the min/max delay is 48 ns ± 3 ns. Similarly, if the platform clock is 400 MHz, the min/max delay is 40 ns ± 3 ns.
- t_{plb_clk} is the platform (CCB) clock.

This figure shows the MII management interface timing diagram.

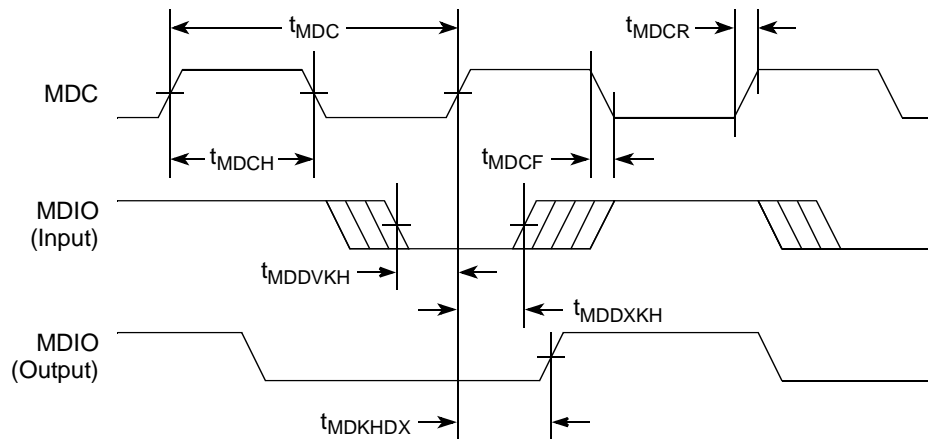


Figure 26. MII Management Interface Timing Diagram

2.11.6 eTSEC IEEE Std 1588™ Timing Specifications

2.11.6.1 eTSEC IEEE Std 1588 DC Electrical Characteristics

This table shows eTSEC IEEE Std 1588 DC electrical characteristics when operating at $V_{DD} = 3.3$ V supply.

Table 47. eTSEC IEEE 1588 DC Electrical Characteristics ($V_{DD} = 3.3$ V)

For recommended operating conditions with $V_{DD} = 3.3$ V.

| Parameter | Symbol | Min | Max | Unit | Notes |
|--|----------|-----|-----|---------------|-------|
| Input high voltage | V_{IH} | 2.0 | — | V | 2 |
| Input low voltage | V_{IL} | — | 0.9 | V | 2 |
| Input high current ($V_{DD} = \text{Max}$, $V_{IN} = 2.1$ V) | I_{IH} | — | 50 | μA | 1 |

Electrical Characteristics

Table 47. eTSEC IEEE 1588 DC Electrical Characteristics (LV_{DD} = 3.3 V) (continued)

For recommended operating conditions with LV_{DD} = 3.3 V.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|-----------------|-----|-----|------|-------|
| Input low current (LV _{DD} = Max, V _{IN} = 0.5 V) | I _{IL} | -50 | — | μA | 1 |
| Output high voltage (LV _{DD} = Min, I _{OH} = -1.0 mA) | V _{OH} | 2.4 | — | V | — |
| Output low voltage (LV _{DD} = Min, I _{OL} = 1.0 mA) | V _{OL} | — | 0.4 | V | — |

Note:

- Note that the symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in [Table 2](#) and [Table 3](#).
- The min V_{IL} and max V_{IH} values are based on the respective LV_{IN} values found in [Table 3](#).

This table shows the IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 2.5 V supply.

Table 48. eTSEC IEEE 1588 DC Electrical Characteristics (LV_{DD} = 2.5 V)

For recommended operating conditions with LV_{DD} = 2.5 V

| Parameter | Symbol | Min | Max | Unit | Notes |
|--|-----------------|------|------|------|-------|
| Input high voltage | V _{IH} | 1.70 | — | V | — |
| Input low voltage | V _{IL} | — | 0.70 | V | — |
| Input current (LV _{IN} = 0 V or LV _{IN} = LV _{DD}) | I _{IH} | — | ±50 | μA | 2 |
| Output high voltage (LV _{DD} = min, I _{OH} = -1.0 mA) | V _{OH} | 2.00 | — | V | — |
| Output low voltage (LV _{DD} = min, I _{OL} = 1.0 mA) | V _{OL} | — | 0.40 | V | — |

Note:

- The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in [Table 3](#).
- The symbol V_{IN}, in this case, represents the LV_{IN} symbols referenced in [Table 2](#) and [Table 3](#).

2.11.6.2 eTSEC IEEE 1588 AC Specifications

This table provides the IEEE 1588 AC timing specifications.

Table 49. eTSEC IEEE 1588 AC Timing Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|------------------------------------|---|---------------------------|-----|-------------------------|------|------|
| TSEC_1588_CLK clock period | t _{T1588CLK} | 5 | — | T _{RX_CLK} × 7 | ns | 1, 3 |
| TSEC_1588_CLK duty cycle | t _{T1588CLKH} / t _{T1588CLK} | 40 | 50 | 60 | % | — |
| TSEC_1588_CLK peak-to-peak jitter | t _{T1588CLKINJ} | — | — | 250 | ps | — |
| Rise time eTSEC_1588_CLK (20%–80%) | t _{T1588CLKINR} | 1.0 | — | 2.0 | ns | — |
| Fall time eTSEC_1588_CLK (80%–20%) | t _{T1588CLKINF} | 1.0 | — | 2.0 | ns | — |
| TSEC_1588_CLK_OUT clock period | t _{T1588CLKOUT} | 2 × t _{T1588CLK} | — | — | ns | — |
| TSEC_1588_CLK_OUT duty cycle | t _{T1588CLKOTH} / t _{T1588CLKOUT} | 30 | 50 | 70 | % | — |
| TSEC_1588_PULSE_OUT | t _{T1588OV} | 0.5 | — | 3.0 | ns | — |

Table 49. eTSEC IEEE 1588 AC Timing Specifications (continued)

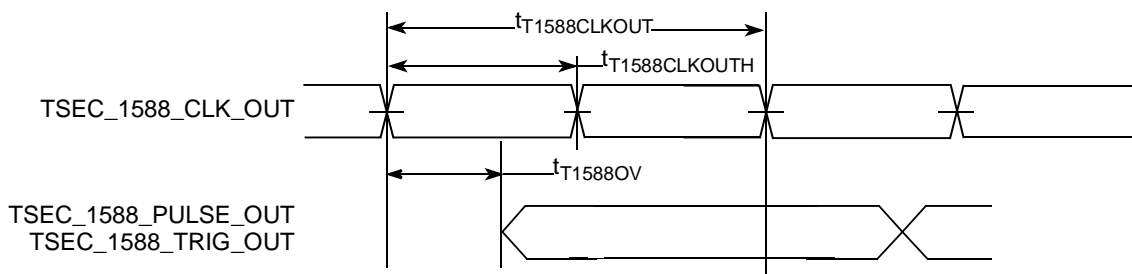
For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|-------------------------------|------------------|------------------------------|-----|-----|------|------|
| TSEC_1588_TRIG_IN pulse width | $t_{T1588TRIGH}$ | $2 \times t_{T1588CLK_MAX}$ | — | — | ns | 2 |

Note:

1. T_{RX_CLK} is the max clock period of eTSEC receiving clock selected by TMR_CTRL[CKSEL]. See the *P1020 QorIQ Integrated Processor Reference Manual* for a description of TMR_CTRL registers.
2. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the *P1020 QorIQ Integrated Processor Reference Manual* for a description of TMR_CTRL registers.
3. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK} , but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ will be 2800, 280, and 56 ns respectively.

This figure shows the data and command output AC timing diagram.



Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is non inverting. Otherwise, it is counted starting at the falling edge.

Figure 27. eTSEC IEEE 1588 Output AC Timing

This figure shows the data and command input AC timing diagram.

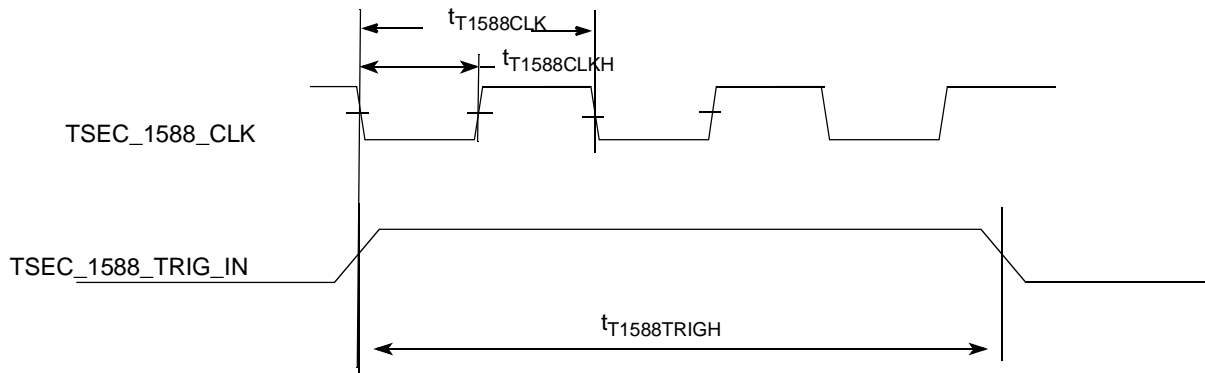


Figure 28. eTSEC IEEE 1588 Input AC Timing

2.12 USB

This section provides the AC and DC electrical specifications for the USB and USB2 interfaces of the P1011. USB2 is muxed with eLBC interface while USB is not muxed except USB_PCTL0 and USB_PCTL1 Both the interfaces USB and USB2 will be referred as USB in this section as they share the same AC and DC characteristics.

2.12.1 USB DC Electrical Characteristics

The following tables provides the DC electrical characteristics for the USB interface.

Table 50. USB DC Electrical Characteristics (CV_{DD} = 3.3 V)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|-----------------|-----|-----|------|-------|
| Input high voltage | V _{IH} | 2 | — | V | 1 |
| Input low voltage | V _{IL} | — | 0.8 | V | 1 |
| Input current (CV _{IN} = 0V or CV _{IN} = CV _{DD}) | I _{IN} | — | ±50 | μA | 2 |
| Output High voltage (CV _{DD} = min, I _{OH} = -2 mA) | V _{OH} | 2.8 | — | V | — |
| Output Low voltage (CV _{DD} = min, I _{OL} = 2 mA) | V _{OL} | — | 0.3 | V | — |

Note:

- Note that the min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in [Table 3](#).
- Note that the symbol CV_{IN} represents the input voltage of the supply. It is referenced in [Table 3](#).

Table 51. USB DC Electrical Characteristics (CV_{DD} = 2.5 V)

| Parameter | Symbol | Min | Max | Unit | Notes |
|--|-----------------|-----|-----|------|-------|
| High-level input voltage ¹ | V _{IH} | 1.7 | — | V | 1 |
| Low-level input voltage | V _{IL} | — | 0.7 | V | 1 |
| Input current (V _{IN} = 0 V or V _{IN} = CV _{DD}) | I _{IN} | — | ±40 | μA | 2 |
| High-level output voltage (CV _{DD} = min, I _{OH} = -1 mA) | V _{OH} | 2.0 | — | V | 3 |
| Low-level output voltage (CV _{DD} = min, I _{OL} = 1mA) | V _{OL} | — | 0.4 | V | — |

Notes:

- The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in [Table 3](#).
- The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in [Section 2.1.2, "Recommended Operating Conditions."](#)
- Not applicable for open drain signals.

Table 52. USB DC Electrical Characteristics ($CV_{DD} = 1.8V$)

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|----------|------|----------|---------|-------|
| High-level input voltage ¹ | V_{IH} | 1.25 | — | V | 1 |
| Low-level input voltage | V_{IL} | — | 0.6 | V | 1 |
| Input current ($V_{IN} = 0 V$ or $V_{IN} = CV_{DD}$) | I_{IN} | — | ± 40 | μA | 2 |
| High-level output voltage ($CV_{DD} = \text{min}$, $I_{OH} = -0.5 \text{ mA}$) | V_{OH} | 1.35 | — | V | 3 |
| Low-level output voltage ($CV_{DD} = \text{min}$, $I_{OL} = 0.5 \text{ mA}$) | V_{OL} | — | 0.4 | V | — |

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN} , in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."
3. Not applicable for open drain signals.

2.12.2 USB AC Electrical Specifications

This table describes the general timing parameters of the USB interface.

Table 53. USB General Timing Parameters

For recommended operating conditions, see Table 3

| Parameter | Symbol | Min | Max | Unit | Notes |
|--|--------------|-----|-----|------|------------|
| USB clock cycle time | t_{USCK} | 15 | — | ns | 2, 3, 4, 5 |
| Input setup to USB clock—all inputs | t_{USIVKH} | 4 | — | ns | 2, 3, 4, 5 |
| input hold to USB clock—all inputs | t_{USIXKH} | 1 | — | ns | 2, 3, 4, 5 |
| USB clock to output valid—all outputs | t_{USKHOV} | — | 7 | ns | 2, 3, 4, 5 |
| Output hold from USB clock—all outputs | t_{USKHGX} | 2 | — | ns | 2, 3, 4, 5 |

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(\text{First two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{First two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHGX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H) with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from $CV_{DD}/2$ of the rising edge of the USB clock to $0.4 \times CV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.
6. When switching the data pins from outputs to inputs using the $USBn_DIR$ pin, the output timings will be violated on that cycle because the output buffers are tristated asynchronously. This should not be a problem, because the PHY should not be functionally looking at these signals on that cycle as per ULPI specifications.

Electrical Characteristics

These figures provide the AC test load and signals for the USB, respectively.

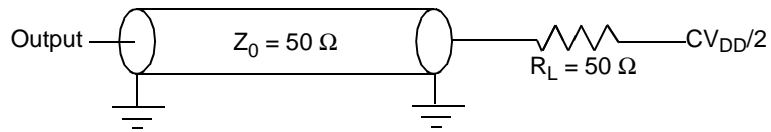


Figure 29. USB AC Test Load

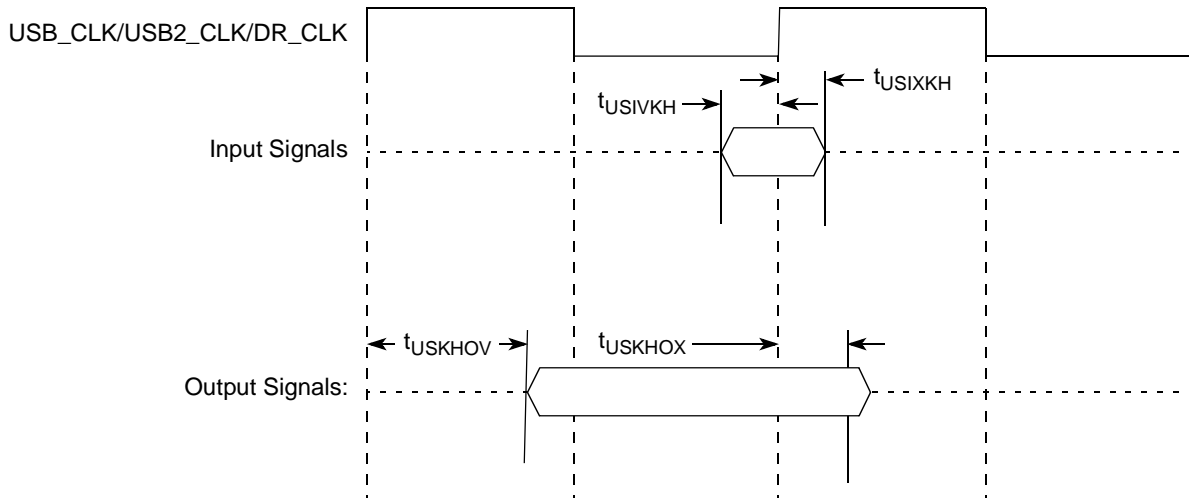


Figure 30. USB Signals

This table provides the USB clock input (USB_CLK_IN) AC timing specifications.

Table 54. USB_CLK_IN AC Timing Specifications

| Parameter | Conditions | Symbol | Min | Typ | Max | Unit |
|--|---|---------------------------|-------|-----|-------|------|
| Frequency range | Steady state | $f_{\text{USB_CLK_IN}}$ | 59.97 | 60 | 60.03 | MHz |
| Clock frequency tolerance | — | $t_{\text{CLK_TOL}}$ | -0.05 | 0 | 0.05 | % |
| Reference clock duty cycle | Measured at 1.6 V | $t_{\text{CLK_DUTY}}$ | 40 | 50 | 60 | % |
| Total input jitter/time interval error | Peak-to-peak value measured with a second order high-pass filter of 500 kHz bandwidth | $t_{\text{CLK_PJ}}$ | — | — | 200 | ps |

2.13 Enhanced Local Bus

This section describes the DC and AC electrical specifications for the enhanced local bus interface.

2.13.1 Enhanced Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the enhanced local bus interface operating at $BV_{DD} = 3.3$ V DC.

Table 55. Enhanced Local Bus DC Electrical Characteristics (3.3 V DC)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit |
|--|----------|-----|----------|---------|
| Input high voltage | V_{IH} | 2 | — | V |
| Input low voltage | V_{IL} | — | 0.8 | V |
| Input current ($V_{IN} = 0$ V or $V_{IN} = BV_{DD}$) | I_{IN} | — | ± 50 | μ A |
| Output high voltage ($BV_{DD} = \text{min}$, $I_{OH} = -2$ mA) | V_{OH} | 2.4 | — | V |
| Output low voltage ($BV_{DD} = \text{min}$, $I_{OL} = 2$ mA) | V_{OL} | — | 0.4 | V |

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in [Table 3](#).
2. The symbol V_{IN} , in this case, represents the BV_{IN} symbol referenced in [Section 2.1.2, "Recommended Operating Conditions."](#)

This table provides the DC electrical characteristics for the enhanced local bus interface when operating at $BV_{DD} = 2.5$ V DC.

Table 56. Enhanced Local Bus DC Electrical Characteristics (2.5 V DC)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit |
|--|----------|-----|----------|---------|
| Input high voltage | V_{IH} | 1.7 | — | V |
| Input low voltage | V_{IL} | — | 0.7 | V |
| Input current ($V_{IN} = 0$ V or $V_{IN} = BV_{DD}$) | I_{IN} | — | ± 50 | μ A |
| Output high voltage ($BV_{DD} = \text{min}$, $I_{OH} = -1$ mA) | V_{OH} | 2.0 | — | V |
| Output low voltage ($BV_{DD} = \text{min}$, $I_{OL} = 1$ mA) | V_{OL} | — | 0.4 | V |

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in [Table 3](#).
2. The symbol V_{IN} , in this case, represents the BV_{IN} symbol referenced in [Section 2.1.2, "Recommended Operating Conditions."](#)

Electrical Characteristics

This table provides the DC electrical characteristics for the enhanced local bus interface when operating at $BV_{DD} = 1.8 \text{ V DC}$.

Table 57. Enhanced Local Bus DC Electrical Characteristics (1.8 V DC)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit |
|---|----------|------|----------|---------------|
| Input high voltage | V_{IH} | 1.25 | — | V |
| Input low voltage | V_{IL} | — | 0.6 | V |
| Input current ($V_{IN} = 0 \text{ V}$ or $V_{IN} = BV_{DD}$) | I_{IN} | — | ± 50 | μA |
| Output high voltage ($BV_{DD} = \text{min}$, $I_{OH} = -0.5 \text{ mA}$) | V_{OH} | 1.35 | — | V |
| Output low voltage ($BV_{DD} = \text{min}$, $I_{OL} = 0.5 \text{ mA}$) | V_{OL} | — | 0.4 | V |

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in [Table 3](#).
2. The symbol V_{IN} , in this case, represents the BV_{IN} symbol referenced in [Section 2.1.2, "Recommended Operating Conditions."](#)

2.13.2 Enhanced Local Bus AC Electrical Specifications

2.13.2.1 Test Condition

This figure provides the AC test load for the enhanced local bus.

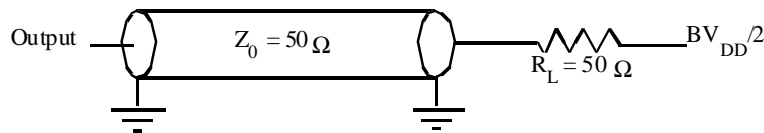


Figure 31. Enhanced Local Bus AC Test Load

2.13.2.2 Local Bus AC Timing Specifications for PLL Bypass Mode

All output signal timings are relative to the falling edge of any LCLKs for PLL bypass mode. The external circuit must use the rising edge of the LCLKs to latch the data.

All input timings except LGTA/LUPWAIT/LFRB are relative to the rising edge of LCLKs. LGTA/LUPWAIT/LFRB are relative to the falling edge of LCLKs.

This table describes the timing specifications of the local bus interface for PLL bypass mode.

Table 58. Enhanced Local Bus Timing Specifications ($BV_{DD} = 3.3\text{ V}, 2.5\text{ V}, \text{ and } 1.8\text{ V}$)—PLL Bypass Mode

For recommended operating conditions, see Table 3.

| Parameter | Symbol ¹ | Min | Max | Unit | Notes |
|---|---------------------|--|-----|-----------------------------|-------|
| Local bus cycle time | t_{LBK} | 12 | — | ns | — |
| Local bus duty cycle | t_{LBKH}/t_{LBK} | 45 | 55 | % | — |
| LCLK[n] skew to LCLK[m] or LSYNC_OUT | $t_{LBKSKEW}$ | — | 150 | ps | 2 |
| Input setup (except LGTA/LUPWAIT/LFRB) | t_{LBIVKH} | 6 | — | ns | — |
| Input hold (except LGTA/LUPWAIT/LFRB) | t_{LBIXKH} | 1 | — | ns | — |
| Input setup (for LGTA/LUPWAIT/LFRB) | t_{LBIVKL} | 6 | — | ns | — |
| Input hold (for LGTA/LUPWAIT/LFRB) | t_{LBIXKL} | 1 | — | ns | — |
| Output delay (Except LALE) | t_{LBKLOV} | — | 1.5 | ns | — |
| Output hold (Except LALE) | t_{LBKLOX} | –3.5 | — | ns | 5 |
| Local bus clock to output high impedance for LAD/LDP | t_{LBKLOZ} | — | 2 | ns | 3 |
| LALE output negation to LAD/LDP output transition (LATCH hold time) | t_{LBONOT} | 1/2 (LBCR[AHD]=1) 1 (LBCR[AHD]=0) | — | eLBC controller clock cycle | 4 |

Note:

1. All signals are measured from $BV_{DD}/2$ of rising/falling edge of LCLK to $BV_{DD}/2$ of the signal in question.
2. Skew measured between different LCLK signals at $BV_{DD}/2$.
3. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. t_{LBONOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBONOT} is determined by LBCR[AHD]. The unit is the eLBC controller clock cycle, which is the internal clock that runs the local bus controller, not the external LCLK. LCLK cycle = eLBC controller clock cycle \times LCRR[CLKDIV]. After power on reset, LBCR[AHD] defaults to 0 and eLBC runs at maximum hold time.
5. Output hold is negative. This means that output transition happens earlier than the falling edge of LCLK.

Electrical Characteristics

This figure shows the AC timing diagram for PLL bypass mode.

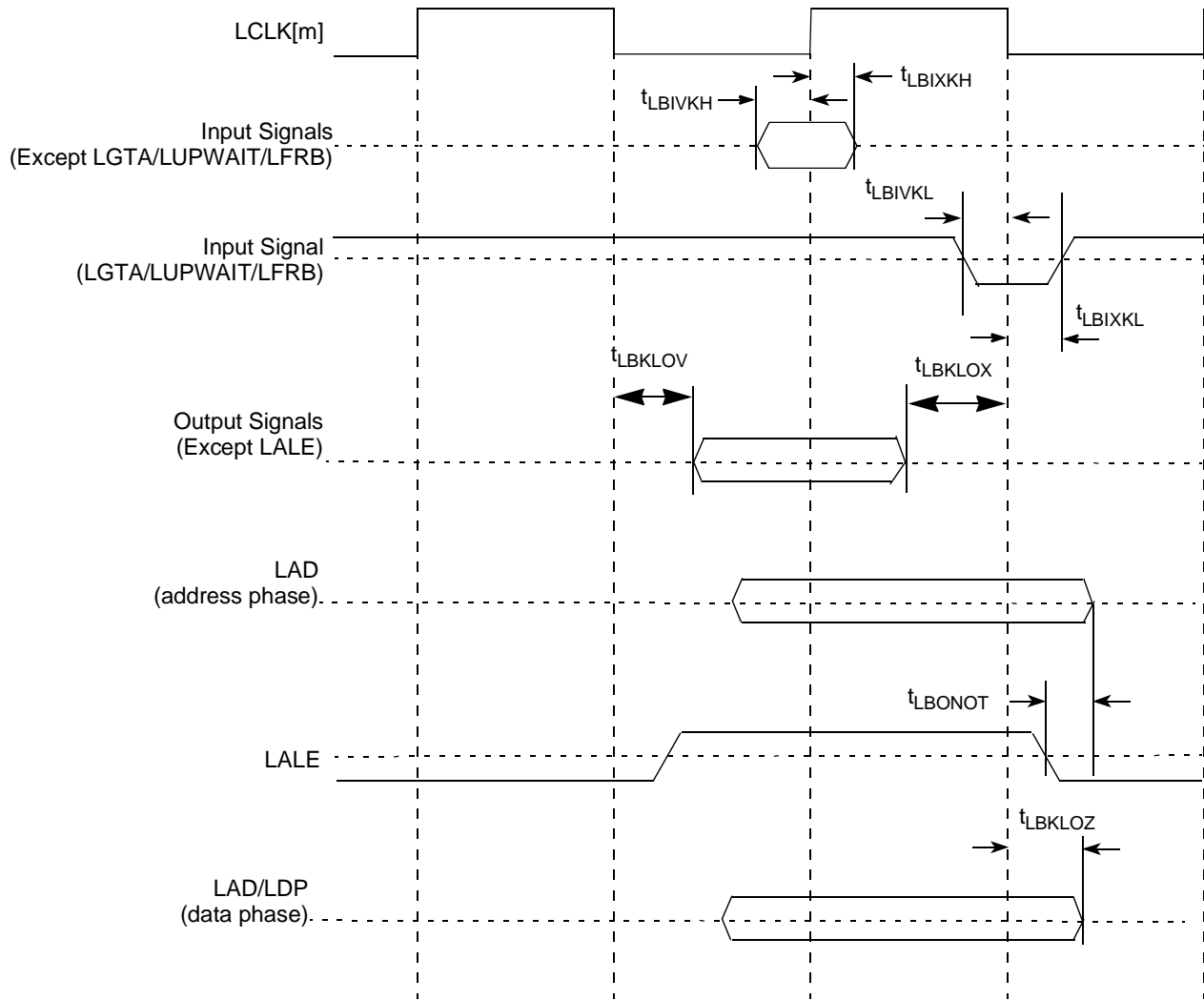


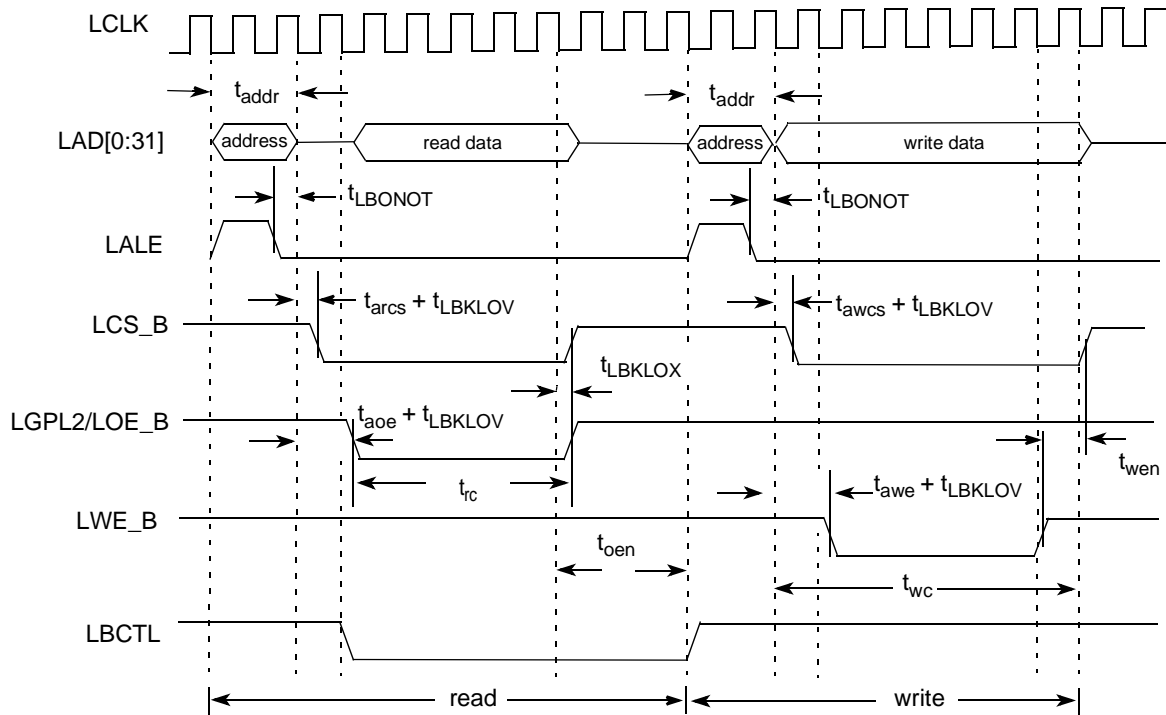
Figure 32. Enhanced Local Bus Signals (PLL Bypass Mode)

This figure applies to all three controllers that eLBC supports: GPCM, UPM, and FCM.

For input signals, the AC timing data is used directly for all three controllers.

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by t_{acs} (0, 1/4, 1/2, 1, 1 + 1/4, 1 + 1/2, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKLOV}$.

This figure shows how the AC timing diagram applies to GPCM in PLL bypass mode. The same principle applies to UPM and FCM.



- ¹ t_{addr} is programmable and determined by LCRR[EADC] and ORx[EAD].
- ² t_{arcs} , t_{awcs} , t_{aoe} , t_{rc} , t_{oen} , t_{awe} , t_{wc} , t_{wen} are determined by ORx. See the P1020 reference manual.

Figure 33. GPCM Output Timing Diagram (PLL Bypass Mode)

2.14 Enhanced Secure Digital Host Controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

2.14.1 eSDHC DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSDHC interface.

Table 59. eSDHC Interface DC Electrical Characteristics

At recommended operating conditions with $CV_{DD} = 3.3\text{ V}$

| Parameter | Symbol | Condition | Min | Max | Unit | Notes |
|---------------------|----------|--|------------------------|------------------------|------|-------|
| Input high voltage | V_{IH} | — | $0.625 \times CV_{DD}$ | — | V | 1 |
| Input low voltage | V_{IL} | — | — | $0.25 \times CV_{DD}$ | V | 1 |
| Output high voltage | V_{OH} | $I_{OH} = -100\text{ uA}$ at CV_{DD} min | $0.75 \times CV_{DD}$ | — | V | — |
| Output low voltage | V_{OL} | $I_{OL} = 100\text{ uA}$ at CV_{DD} min | — | $0.125 \times CV_{DD}$ | V | — |
| Output high voltage | V_{OH} | $I_{OH} = -100\text{ uA}$ | $CV_{DD} - 2$ | — | V | 2 |
| Output low voltage | V_{OL} | $I_{OL} = 2\text{ mA}$ | — | 0.3 | V | 2 |

Electrical Characteristics

Table 59. eSDHC Interface DC Electrical Characteristics (continued)

At recommended operating conditions with $C_{V_{DD}} = 3.3\text{ V}$

| Parameter | Symbol | Condition | Min | Max | Unit | Notes |
|------------------------------|-----------------|-----------|-----|-----|------|-------|
| Input/output leakage current | I_{IN}/I_{OZ} | — | -50 | 50 | uA | — |

Note:

- Note that the min V_{IL} and max V_{IH} values are based on the respective min and max $C_{V_{IN}}$ values found in [Figure 3](#).
- Open drain mode for MMC cards only.

2.14.2 eSDHC AC Timing Specifications

This table provides the eSDHC AC timing specifications as defined in [Figure 35](#).

Table 60. eSDHC AC Timing Specifications

At recommended operating conditions with $C_{V_{DD}} = 3.3\text{ V}$

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|-----------------------------|------|----------------|------|-------|
| SD_CLK clock frequency: SD/SDIO Full-speed/High-speed mode MMC Full-speed/High-speed mode | f_{SFCK} | 0 | 25/50 20/52 | MHz | 2, 4 |
| SD_CLK clock low time—Full-speed/High-speed mode | t_{SFCKL} | 10/7 | — | ns | 4 |
| SD_CLK clock high time—Full-speed/High-speed mode | t_{SFCKH} | 10/7 | — | ns | 4 |
| SD_CLK clock rise and fall times | $t_{SFCKR}/$ t_{SFCKF} | — | 3 | ns | 4 |
| Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK | $t_{SFSIVKH}$ | 5.0 | — | ns | 4 |
| Input hold times: SD_CMD, SD_DATx, SD_CD to SD_CLK | $t_{SFSIXKH}$ | 2.5 | — | ns | 3, 4 |
| Output delay time: SD_CLK to SD_CMD, SD_DATx valid | $t_{SHSKHOV}$ | -3 | 3 | ns | 4 |

Note:

- The symbols used for timing specifications herein follow the pattern of $t_{(\text{first three letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first three letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{FHSHKHOV}$ symbolizes eSDHC high speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that, in general, the clock reference symbol representation is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- In full speed mode, clock frequency value can be 0–25 MHz for a SD/SDIO card and 0–20 MHz for a MMC card. In high speed mode, clock frequency value can be 0–50 MHz for a SD/SDIO card and 0–52 MHz for a MMC card.
- To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.
- $C_{CARD} \leq 10\text{ pF}$, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40\text{ pF}$

This figure provides the eSDHC clock input timing diagram.

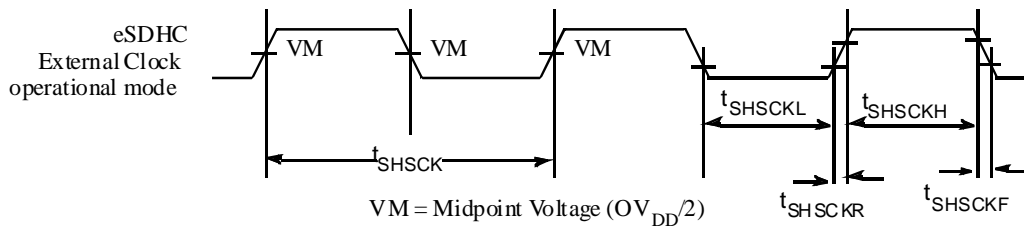


Figure 34. eSDHC Clock Input Timing Diagram

This figure provides the data and command input/output timing diagram.

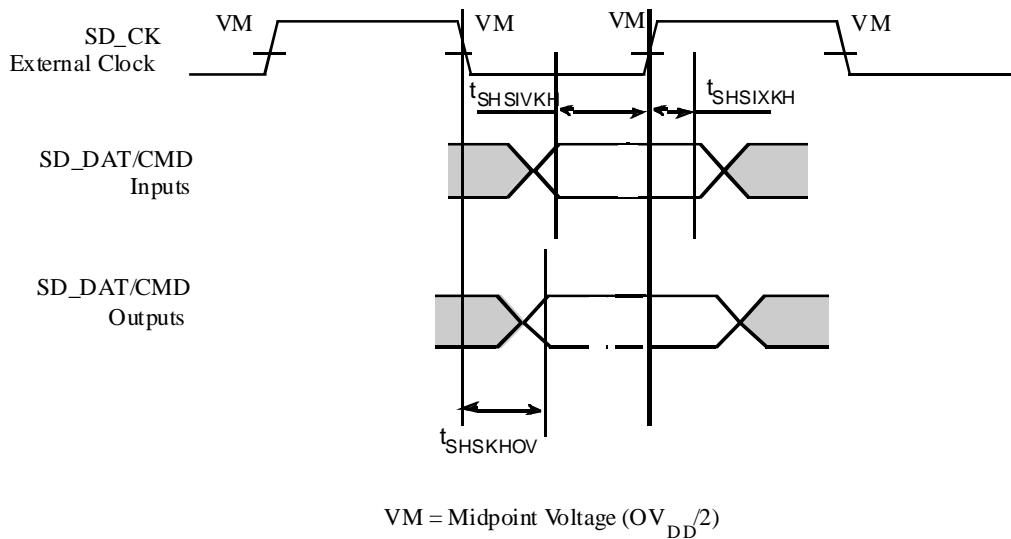


Figure 35. eSDHC Data and Command Input/Output Timing Diagram Referenced to Clock

2.15 Programmable Interrupt Controller (PIC) Specifications

This section describes the DC and AC electrical specifications for PIC.

2.15.1 PIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the PIC interface.

Table 61. PIC DC Electrical Characteristics

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|----------|-----|----------|---------|-------|
| Input high voltage | V_{IH} | 2 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.8 | V | 1 |
| Input current ($OV_{IN} = 0V$ or $OV_{IN} = OV_{DD}$) | I_{IN} | — | ± 50 | μA | 2 |
| Output high voltage ($OV_{DD} = \text{min}$, $I_{OH} = -2 \text{ mA}$) | V_{OH} | 2.4 | — | V | — |

Electrical Characteristics

Table 61. PIC DC Electrical Characteristics (continued)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|----------|-----|-----|------|-------|
| Output low voltage ($OV_{DD} = \text{min}$, $I_{OL} = 2 \text{ mA}$) | V_{OL} | — | 0.4 | V | — |

Note:

- Note that the min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in [Table 3](#).
- Note that the symbol OV_{IN} represents the input voltage of the supply. It is referenced in [Table 3](#).

2.15.2 PIC AC Timing Specifications

This table provides the PIC input and output AC timing specifications.

Table 62. PIC Input AC Timing Specifications

For recommended operating conditions, see [Table 3](#)

| Parameter | Symbol | Min | Max | Unit | Notes |
|--------------------------------|-------------|-----|-----|--------|-------|
| PIC inputs—minimum pulse width | t_{PIWID} | 3 | — | SYSCLK | 1 |

Note:

- PIC inputs and outputs are asynchronous to any visible clock. PIC outputs should be synchronized before use by any external synchronous logic. PIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge-triggered mode.

2.16 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the P1011.

2.16.1 JTAG DC Electrical Characteristics

This table provides the JTAG DC electrical characteristics.

Table 63. JTAG DC Electrical Characteristics

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|----------|-----|----------|---------------|-------|
| Input high voltage | V_{IH} | 2 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.8 | V | 1 |
| Input current ($OV_{IN} = 0V$ or $OV_{IN} = OV_{DD}$) | I_{IN} | — | ± 50 | μA | 2 |
| Output high voltage ($OV_{DD} = \text{min}$, $I_{OH} = -2 \text{ mA}$) | V_{OH} | 2.4 | — | V | — |
| Output low voltage ($OV_{DD} = \text{min}$, $I_{OL} = 2 \text{ mA}$) | V_{OL} | — | 0.4 | V | — |

Note:

- Note that the min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in [Table 3](#).
- Note that the symbol OV_{IN} represents the input voltage of the supply. It is referenced in [Table 3](#).

2.16.2 JTAG AC Timing Specifications

This table provides the JTAG AC timing specifications as defined in Figure 36 through Figure 39.

Table 64. JTAG AC Timing Specifications

For recommended operating conditions see Table 3.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|-----|------|------|-------|
| JTAG external clock frequency of operation | f_{JTG} | 0 | 33.3 | MHz | — |
| JTAG external clock cycle time | t_{JTG} | 30 | — | ns | — |
| JTAG external clock pulse width measured at 1.4 V | t_{JTKHKL} | 15 | — | ns | — |
| JTAG external clock rise and fall times | t_{JTGR} and t_{JTGF} | 0 | 2 | ns | — |
| $\overline{\text{TRST}}$ assert time | t_{TRST} | 25 | — | ns | 2 |
| Input setup times | t_{JTDVKH} | 4 | — | ns | — |
| Input hold times | t_{JTDXKH} | 10 | — | ns | — |
| Output valid times | t_{JTKLDV} | 4 | 10 | ns | 3 |
| Output hold times | t_{JTKLDX} | 30 | — | ns | 3 |

Notes:

- The symbols used for timing specifications follow the pattern $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that in general, the clock reference symbol representation is based on three letters representing the clock of a SerDes Transmitter particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
- All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50- Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

This figure provides the AC test load for TDO and the boundary-scan outputs.

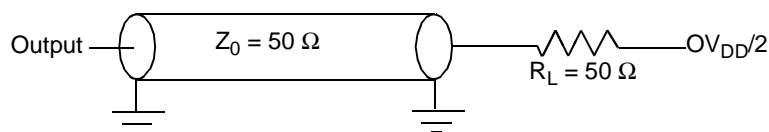


Figure 36. AC Test Load for the JTAG Interface

This figure provides the JTAG clock input timing diagram.

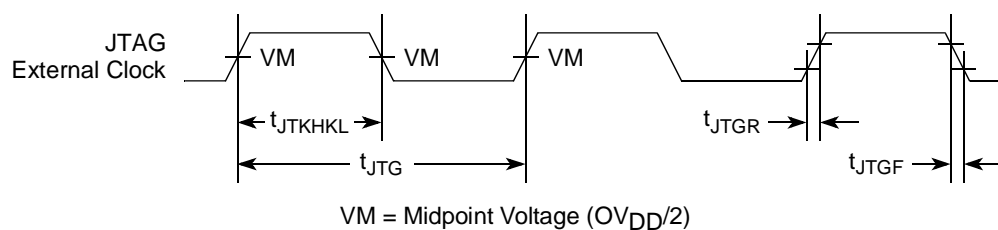


Figure 37. JTAG Clock Input Timing Diagram

Electrical Characteristics

This figure provides the $\overline{\text{TRST}}$ timing diagram.

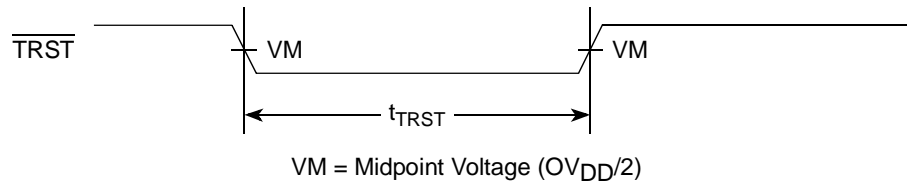


Figure 38. $\overline{\text{TRST}}$ Timing Diagram

This figure provides the boundary-scan timing diagram.

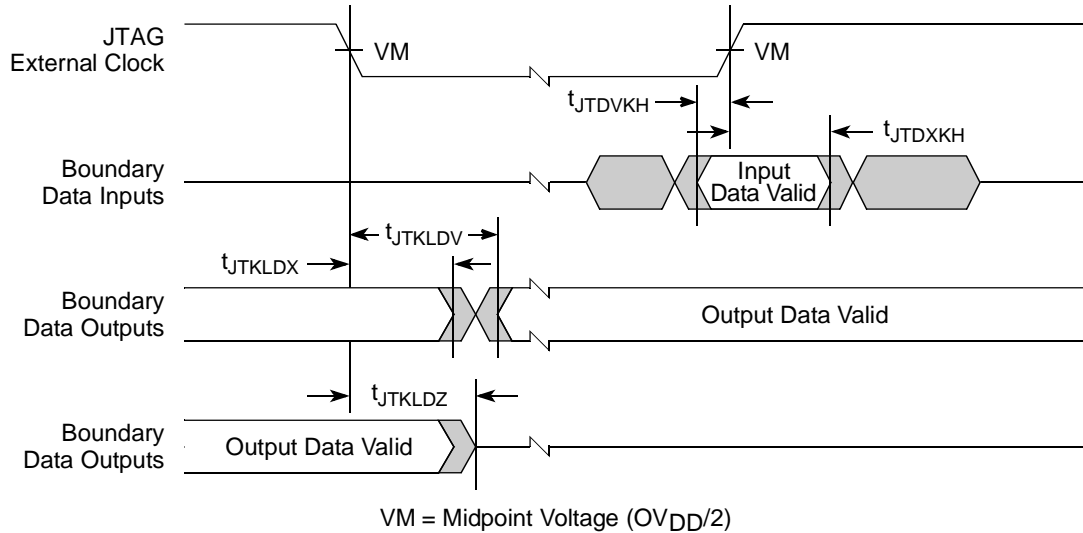


Figure 39. Boundary-Scan Timing Diagram

2.17 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces.

2.17.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I²C interfaces.

Table 65. I²C DC Electrical Characteristics

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Notes |
|--|--------------|-----|-----|---------------|-------|
| Input high voltage | V_{IH} | 2 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.8 | V | 1 |
| Output low voltage | V_{OL} | 0 | 0.4 | V | 2 |
| Pulse width of spikes which must be suppressed by the input filter | t_{I2KHKL} | 0 | 50 | ns | 3 |
| Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}(\text{max})$) | I_I | -50 | 50 | μA | 4 |

Table 65. I²C DC Electrical Characteristics (continued)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Notes |
|------------------------------|--------|-----|-----|------|-------|
| Capacitance for each I/O pin | C_I | — | 10 | pF | — |

Notes:

- Note that the min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in [Table 3](#).
- Output voltage (open drain or open collector) condition = 3 mA sink current.
- Refer to the *P1020 QorIQ Integrated Processor Reference Manual* for information on the digital filter used.
- I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

2.17.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I²C interfaces.

Table 66. I²C AC Electrical Specifications

For recommended operating conditions see [Table 3](#). All values refer to V_{IH} (min) and V_{IL} (max) levels (see [Table 65](#)).

| Parameter | Symbol | Min | Max | Unit | Notes |
|--|--------------|----------------------|--------|------|-------------------|
| SCL clock frequency | f_{I2C} | 0 | 400 | kHz | 2 |
| Low period of the SCL clock | t_{I2CL} | 1.3 | — | μs | — |
| High period of the SCL clock | t_{I2CH} | 0.6 | — | μs | — |
| Setup time for a repeated START condition | t_{I2SVKH} | 0.6 | — | μs | — |
| Hold time (repeated) START condition (after this period, the first clock pulse is generated) | t_{I2SXKL} | 0.6 | — | μs | — |
| Data setup time | t_{I2DVKH} | 100 | — | ns | — |
| Data hold time: CBUS compatible masters I ² C bus devices | t_{I2DXKL} | — 0 | — — | μs | 3 |
| Data output delay time | t_{I2OVKL} | — | 0.9 | μs | 4 |
| Set-up time for STOP condition | t_{I2PVKH} | 0.6 | — | μs | — |
| Bus free time between a STOP and START condition | t_{I2KHDX} | 1.3 | — | μs | — |
| Noise margin at the LOW level for each connected device (including hysteresis) | V_{NL} | $0.1 \times OV_{DD}$ | — | V | — |
| Noise margin at the HIGH level for each connected device (including hysteresis) | V_{NH} | $0.2 \times OV_{DD}$ | — | V | — |

Electrical Characteristics

Table 66. I²C AC Electrical Specifications (continued)

For recommended operating conditions see Table 3. All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 65).

| Parameter | Symbol | Min | Max | Unit | Notes |
|-----------------------------------|--------|-----|-----|------|-------|
| Capacitive load for each bus line | Cb | — | 400 | pF | |

Note:

1. The symbols used for timing specifications herein follow the pattern t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. The requirements for I²C frequency calculation must be followed. Refer to Freescale application note AN2919, “Determining the I²C Frequency Divider Ratio for SCL.”
3. As a transmitter, the processor provides a delay time of at least 300 ns for the SDA signal (referred to as the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the processor acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the device does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If under some rare condition, the 300 ns SDA output delay time is required for the processor as transmitter, refer to AN2919, “Determining the I²C Frequency Divider Ratio for SCL.”
4. The maximum t_{I2OVKL} only must be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

This figure provides the AC test load for the I²C.

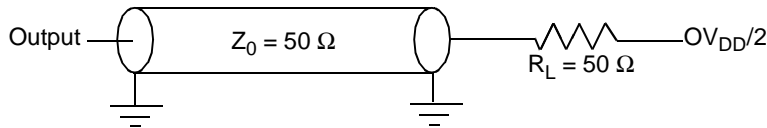


Figure 40. I²C AC Test Load

This figure shows the AC timing diagram for the I²C bus.

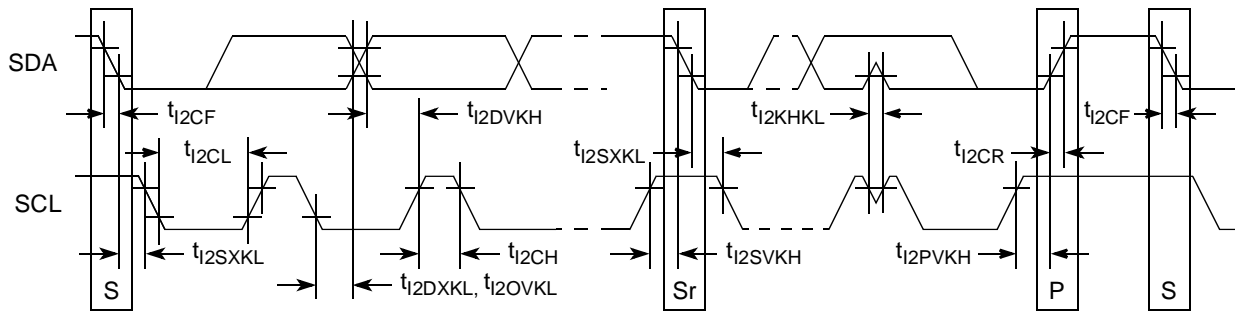


Figure 41. I²C Bus AC Timing Diagram

2.18 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface.

2.18.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO interface powered by OV_{DD} .

Table 67. GPIO[0:7] DC Electrical Characteristics

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|----------|-----|-----|------|-------|
| Input high voltage | V_{IH} | 2 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.8 | V | 1 |
| Input current ($OV_{IN} = 0$ V or $OV_{IN} = OV_{DD}$) | I_{IN} | — | ±50 | μA | 2 |
| Output high voltage ($OV_{DD} = \text{min}$, $I_{OH} = -2$ mA) | V_{OH} | 2.4 | — | V | — |
| Low-level output voltage ($OV_{DD} = \text{min}$, $I_{OL} = 2$ mA) | V_{OL} | — | 0.4 | V | — |

Note:

- Note that the min V_{IL} and max V_{IH} values are based on the min and max OV_{IN} respective values found in [Table 3](#).
- Note that the symbol OV_{IN} represents the input voltage of the supply. It is referenced in [Table 3](#).

This table provides the DC electrical characteristics for the GPIO interface powered by BV_{DD} when operating from 3.3 V supply.

Table 68. GPIO[8:15] DC Electrical Characteristics (3.3 V)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|----------|-----|-----|------|-------|
| Input high voltage | V_{IH} | 2 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.8 | V | 1 |
| Input current ($BV_{IN} = 0$ V or $BV_{IN} = BV_{DD}$) | I_{IN} | — | ±50 | μA | 2 |
| Output high voltage ($BV_{DD} = \text{min}$, $I_{OH} = -2$ mA) | V_{OH} | 2.4 | — | V | — |
| Low-level output voltage ($BV_{DD} = \text{min}$, $I_{OL} = 2$ mA) | V_{OL} | — | 0.4 | V | — |

Note:

- Note that the min V_{IL} and max V_{IH} values are based on the min and max BV_{IN} respective values found in [Table 3](#).
- Note that the symbol BV_{IN} represents the input voltage of the supply. It is referenced in [Table 3](#).

Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO interface powered by BV_{DD} when operating from 2.5 V supply.

Table 69. GPIO[8:15] DC Electrical Characteristics (2.5 V)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|----------|-----|----------|---------|-------|
| Input high voltage | V_{IH} | 1.7 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.7 | V | 1 |
| Input current ($BV_{IN} = 0$ V or $BV_{IN} = BV_{DD}$) | I_{IN} | — | ± 50 | μ A | 2 |
| Output high voltage ($BV_{DD} = \text{min}$, $I_{OH} = 2$ mA) | V_{OH} | 1.7 | — | V | — |
| Low-level output voltage ($BV_{DD} = \text{min}$, $I_{OL} = 2$ mA) | V_{OL} | — | 0.7 | V | — |

Note:

- Note that the min V_{IL} and max V_{IH} values are based on the min and max BV_{IN} respective values found in [Table 3](#).
- Note that the symbol BV_{IN} represents the input voltage of the supply. It is referenced in [Table 3](#).

This table provides the DC electrical characteristics for the GPIO interface powered by BV_{DD} when operating from 1.8 V supply.

Table 70. GPIO[8:15] DC Electrical Characteristics (1.8 V)

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Notes |
|--|----------|------|----------|---------|-------|
| Input high voltage | V_{IH} | 1.2 | — | V | 1 |
| Input low voltage | V_{IL} | — | 0.6 | V | 1 |
| Input current ($BV_{IN} = 0$ V or $BV_{IN} = BV_{DD}$) | I_{IN} | — | ± 40 | μ A | 2 |
| Output high voltage ($BV_{DD} = \text{min}$, $I_{OH} = -0.5$ mA) | V_{OH} | 1.35 | — | V | — |
| Low-level output voltage ($BV_{DD} = \text{min}$, $I_{OL} = 0.5$ mA) | V_{OL} | — | 0.4 | V | — |

Note:

- Note that the min V_{IL} and max V_{IH} values are based on the min and max BV_{IN} respective values found in [Table 3](#).
- Note that the symbol BV_{IN} represents the input voltage of the supply. It is referenced in [Table 3](#).

2.18.2 GPIO AC Timing Specifications

This table provides the GPIO input and output AC timing specifications.

Table 71. GPIO Input AC Timing Specifications

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Unit | Notes |
|---------------------------------|-------------|-----|------|-------|
| GPIO inputs—minimum pulse width | t_{PIWID} | 20 | ns | 1 |

Notes:

- GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.

This figure provides the AC test load for the GPIO.

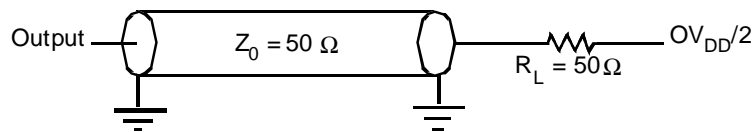


Figure 42. GPIO AC Test Load

2.19 TDM

This section describes the DC and AC electrical specifications for the TDM.

2.19.1 TDM DC Electrical Characteristics

This table provides the DC electrical characteristics TDM.

Table 72. TDM DC Electrical Characteristics

For recommended operating conditions, see [Table 3](#).

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|----------|------|----------|---------|-------|
| Input high voltage | V_{IH} | 2.0 | — | V | 1 |
| Input low voltage | V_{IL} | -0.3 | 0.8 | V | 1 |
| Input current ($OV_{IN} = 0V$ or $OV_{IN} = OV_{DD}$) | I_{IN} | — | ± 50 | μA | 2 |
| Output high voltage ($OV_{DD} = \text{min}$, $I_{OH} = -2 \text{ mA}$) | V_{OH} | 2.4 | — | V | — |
| Output low voltage ($OV_{DD} = \text{min}$, $I_{OL} = 2 \text{ mA}$) | V_{OL} | — | 0.4 | V | — |

Note:

- Note that the min V_{IL} and max V_{IH} values are based on the min and max BV_{IN} respective values found in [Table 3](#).
- Note that the symbol BV_{IN} represents the input voltage of the supply. It is referenced in [Table 3](#).

2.19.2 TDM AC Electrical Characteristics

This table provides input and output AC timing specifications for TDM interface.

Table 73. TDM AC Timing specifications

| Parameter | Symbol | Min | Max | Units | Notes |
|--|-----------------|------|------|-------|-------|
| TDMxRCK/TDMxTCK | t_{DM} | 20.0 | — | ns | — |
| TDMxRCK/TDMxTCK high pulse width | t_{DM_HIGH} | 8.0 | — | ns | — |
| TDMxRCK/TDMxTCK low pulse width | t_{DM_LOW} | 8.0 | — | ns | — |
| TDM all input setup time | t_{DMIVKH} | 3.0 | — | ns | — |
| TDMxRD hold time | $t_{DMRDIXKH}$ | 3.5 | — | ns | — |
| TDMxTFS/TDMxRFS input hold time | $t_{DMFSIXKH}$ | 2.0 | — | ns | 2 |
| TDMxTCK high to TDMxTD output active | t_{DM_OUTAC} | 4.0 | — | ns | 2 |
| TDMxTCK high to TDMxTD output valid | $t_{DMTKHOV}$ | — | 14.0 | ns | — |
| TDMxTD hold time | $t_{DMTKHOX}$ | 2.0 | — | ns | — |
| TDMxTCK High to TDMxTD output high impedance | t_{DM_OUTH} | — | 10.0 | ns | — |
| TDMxTFS/TDMxRFS output valid | $t_{DMFSKHOV}$ | — | 13.5 | ns | — |
| TDMxTFS/TDMxRFS output hold time | $t_{DMFSKHOX}$ | 2.5 | — | ns | — |

Notes:

- The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$ (reference)(state) for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{DMIVKH} symbolizes TDM timing (DM) with respect to the time the input signals (I) reach the valid state (V) relative to the TDM Clock, t_{TC} , reference (K) going to the high (H) state or setup time. Also, output signals (O), hold (X).
- Output values are based on 30 pF capacitive load.
- Inputs are referenced to the sampling that the TDM is programmed to use. Outputs are referenced to the programming edge they are programmed to use. Use of the rising edge or falling edge as a reference is programmable. TDMxTCK and TDMxRCK are shown using the rising edge.

This figure shows the TDM receive signal timing.

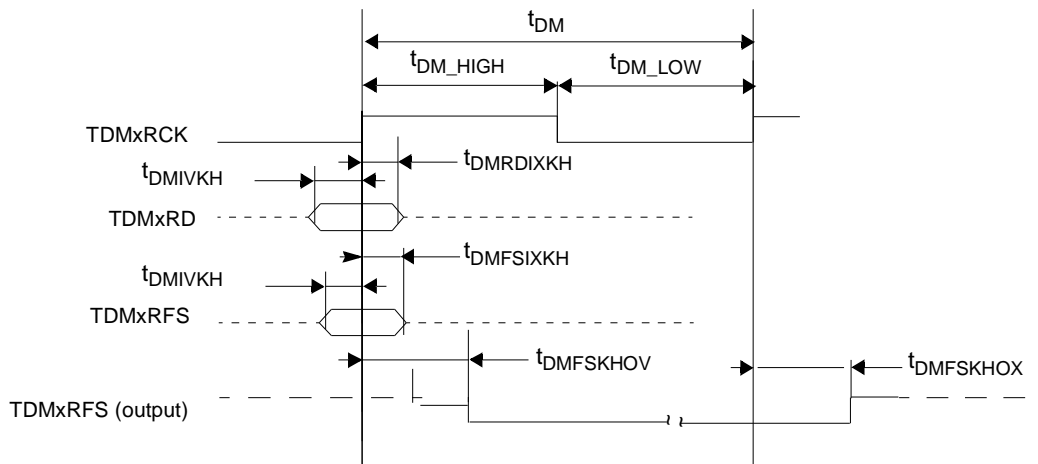


Figure 43. TDM Receive Signals

This figure shows the TDM transmit signal timing.

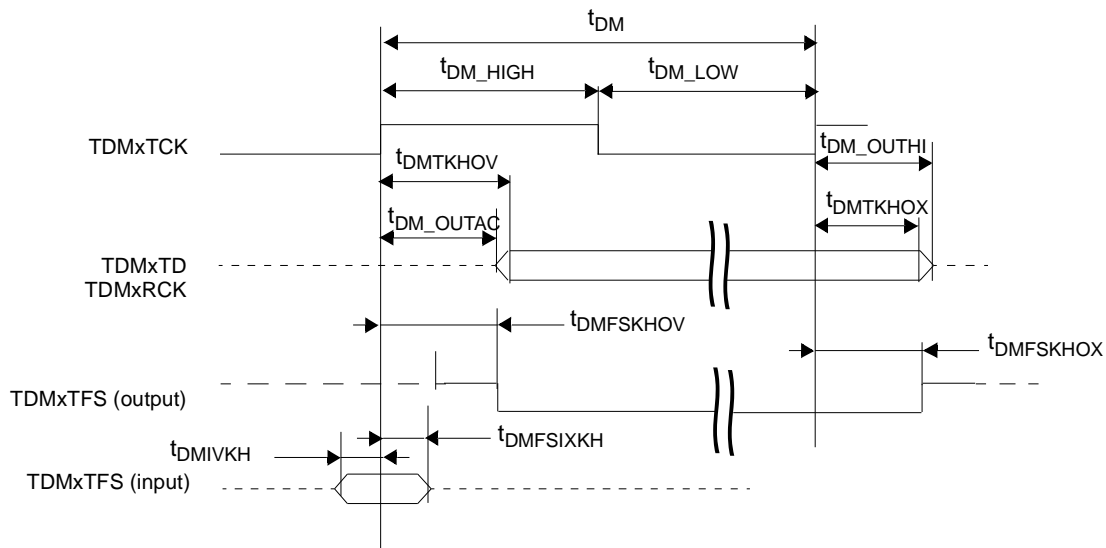


Figure 44. TDM Transmit Signals

2.20 High-Speed Serial Interfaces (HSSI)

The P1011 features one Serializer/Deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express data transfers and for SGMII application.

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

2.20.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 45 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows a waveform for either a transmitter output (SDn_TX and $\overline{SDn_TX}$) or a receiver input (SDn_RX and $\overline{SDn_RX}$). Each signal swings between A volts and B volts where $A > B$.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

- Single-Ended Swing**
 The transmitter output signals and the receiver input signals SDn_TX , $\overline{SDn_TX}$, SDn_RX and $\overline{SDn_RX}$ each have a peak-to-peak swing of $A - B$ volts. This is also referred as each signal wire's Single-Ended Swing.
- Differential Output Voltage, V_{OD} (or Differential Output Swing):**
 The Differential Output Voltage (or Swing) of the transmitter, V_{OD} , is defined as the difference of the two complimentary output voltages: $V_{SDn_TX} - V_{\overline{SDn_TX}}$. The V_{OD} value can be either positive or negative.
- Differential Input Voltage, V_{ID} (or Differential Input Swing):**
 The Differential Input Voltage (or Swing) of the receiver, V_{ID} , is defined as the difference of the two complimentary input voltages: $V_{SDn_RX} - V_{\overline{SDn_RX}}$. The V_{ID} value can be either positive or negative.

Electrical Characteristics

- **Differential Peak Voltage, V_{DIFFp}**

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp} = |A - B|$ Volts.

- **Differential Peak-to-Peak, $V_{DIFFp-p}$**

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from $A - B$ to $-(A - B)$ Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.

- **Differential Waveform**

The differential waveform is constructed by subtracting the inverting signal (SDn_TX , for example) from the non-inverting signal (SDn_TX , for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to [Figure 45](#) as an example for differential waveform.

- **Common Mode Voltage, V_{cm}**

The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = (V_{SDn_TX} + V_{SDn_TX})/2 = (A + B) / 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may even be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset occasionally.

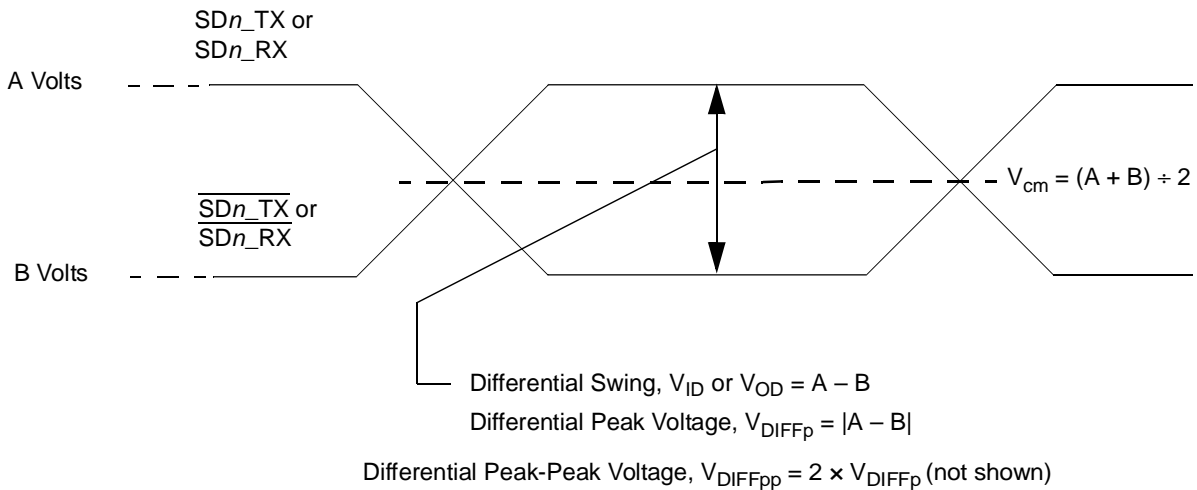


Figure 45. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, \overline{TD} and TD , has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or \overline{TD}) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and -500 mV, in other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

2.20.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clock inputs are `SD_REF_CLK` and `SD_REF_CLK` for PCI Express and SGMII interface.

The following sections describe the SerDes reference clock requirements and some application information.

2.20.2.1 SerDes Reference Clock Receiver Characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

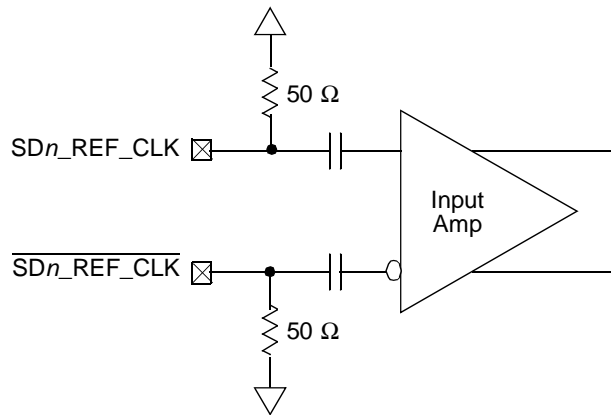


Figure 46. Receiver of SerDes Reference Clocks

The characteristics of the clock signals are as follows:

- The supply voltage requirements for V_{DD_SRDS2} are specified in [Table 2](#) and [Table 3](#).
- SerDes reference clock receiver reference circuit structure
 - The `SD_REF_CLK` and `SD_REF_CLK` are internally AC-coupled differential inputs as shown in [Figure 46](#). Each differential clock input (`SD_REF_CLK` or `SD_REF_CLK`) has a 50- Ω termination to `SGND_SRDS` followed by on-chip AC-coupling.
 - The external reference clock driver must be able to drive this termination.
 - The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode descriptions in [Section 2.20.2.2, “DC Level Requirement for SerDes Reference Clocks,”](#) for requirements.
- The maximum average current requirement that also determines the common mode voltage range.
 - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
 - This current limitation sets the maximum common mode input voltage to be less than 0.4 V ($0.4\text{ V} \div 50 = 8\text{ mA}$) while the minimum common mode input level is 0.1 V above `SGND_SRDS`. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
 - If the device driving the `SD_REF_CLK` and `SD_REF_CLK` inputs cannot drive 50 Ω to `SGND_SRDS` DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.

2.20.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
 - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
 - For **external DC-coupled** connection, as described in [Section 2.20.2.1, “SerDes Reference Clock Receiver Characteristics,”](#) the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 mV and 400 mV. [Figure 47](#) shows the SerDes reference clock input requirement for DC-coupled connection scheme.
 - For **external AC-coupled** connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND_SRDS. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND_SRDS). [Figure 48](#) shows the SerDes reference clock input requirement for AC-coupled connection scheme.

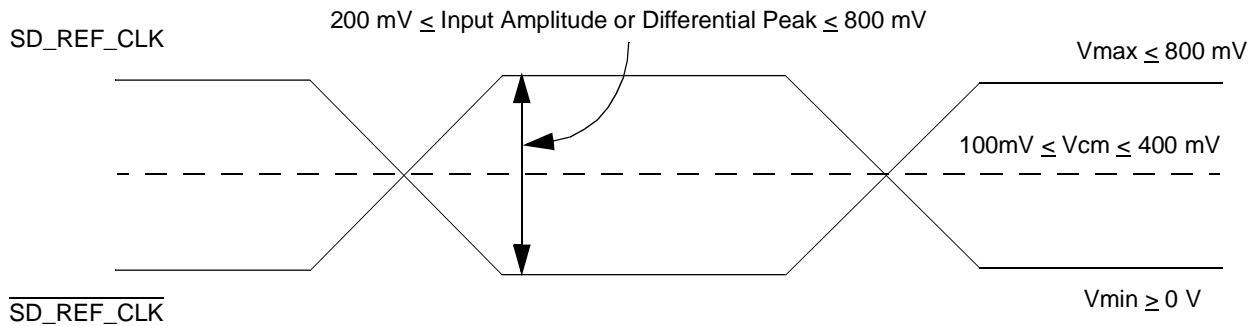


Figure 47. Differential Reference Clock Input DC Requirements (External DC-Coupled)

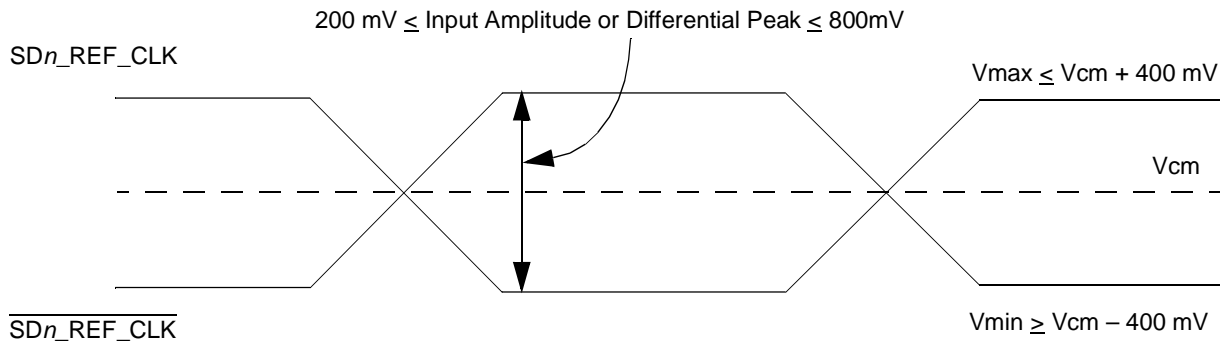


Figure 48. Differential Reference Clock Input DC Requirements (External AC-Coupled)

- **Single-ended Mode**

- The reference clock can also be single ended. The SD_REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from V_{MIN} to V_{MAX}) with $\overline{SD_REF_CLK}$ either left unconnected or tied to ground.
- The SD_REF_CLK input average voltage must be between 200 and 400 mV. Figure 49 shows the SerDes reference clock input requirement for single-ended signaling mode.
- To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC coupled externally. For the best noise performance, the reference of the clock could be DC or AC coupled into the unused phase ($\overline{SD_REF_CLK}$) through the same source impedance as the clock input (SD_REF_CLK) in use.

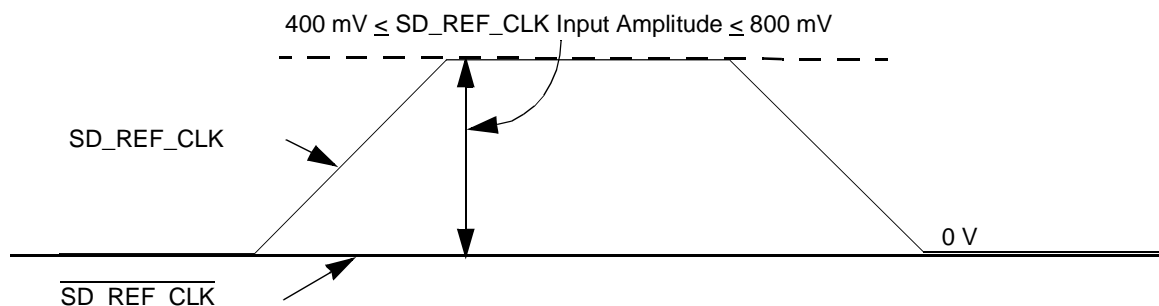


Figure 49. Single-Ended Reference Clock Input DC Requirements

2.20.2.3 AC Requirements for SerDes Reference Clocks

This table lists AC requirements for the PCI Express and SGMII SerDes reference clocks to be guaranteed by the customer's application design.

Table 74. $\overline{SD_REF_CLK}$ and $\overline{SD_REF_CLK}$ Input Clock Requirements

| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
|---|-----------------|------|---------|------|------|-------|
| SD_REF_CLK/ $\overline{SD_REF_CLK}$ frequency range | t_{CLK_REF} | — | 100/125 | — | MHz | 1 |
| SD_REF_CLK/ $\overline{SD_REF_CLK}$ clock frequency tolerance | t_{CLK_TOL} | -350 | — | +350 | ppm | — |
| SD_REF_CLK/ $\overline{SD_REF_CLK}$ reference clock duty cycle | t_{CLK_DUTY} | 40 | 50 | 60 | % | 4 |
| SD_REF_CLK/ $\overline{SD_REF_CLK}$ max deterministic peak-peak Jitter at 10^{-6} BER | t_{CLK_DJ} | — | — | 42 | ps | — |
| SD_REF_CLK/ $\overline{SD_REF_CLK}$ total reference clock jitter at 10^{-6} BER (Peak-to-peak jitter at refClk input) | t_{CLK_TJ} | — | — | 86 | ps | 2 |

Table 74. SD_REF_CLK and $\overline{\text{SD_REF_CLK}}$ Input Clock Requirements (continued)

| Parameter | Symbol | Min | Typical | Max | Unit | Notes |
|---|--------------------------------------|-----|---------|-----|------|-------|
| SD_REF_CLK/ $\overline{\text{SD_REF_CLK}}$ rising/falling edge rate | $t_{\text{CLKRRR}}/t_{\text{CLKFR}}$ | 1 | — | 4 | V/ns | 3 |

Notes:

1. Only 100/125 have been tested, other in between values will not work correctly with the rest of the system.
2. Limits from PCI Express CEM Rev 2.0.
3. Measured from -200 mV to +200 mV on the differential waveform (derived from $\overline{\text{SDn_REF_CLK}}$ minus SDn_REF_CLK). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 50.
4. Measurement taken from differential waveform.
5. Measurement taken from single-ended waveform.
6. Matching applies to rising edge for $\overline{\text{SDn_REF_CLK}}$ and falling edge rate for SDn_REF_CLK . It is measured using a 200 mV window centered on the median cross point where $\overline{\text{SDn_REF_CLK}}$ rising meets SDn_REF_CLK falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of $\overline{\text{SDn_REF_CLK}}$ should be compared to the fall edge rate of SDn_REF_CLK , the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 51.

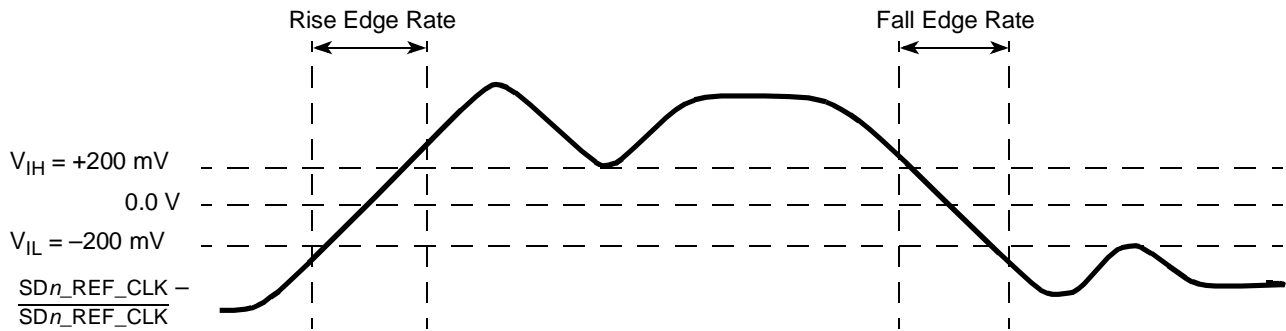


Figure 50. Differential Measurement Points for Rise and Fall Time

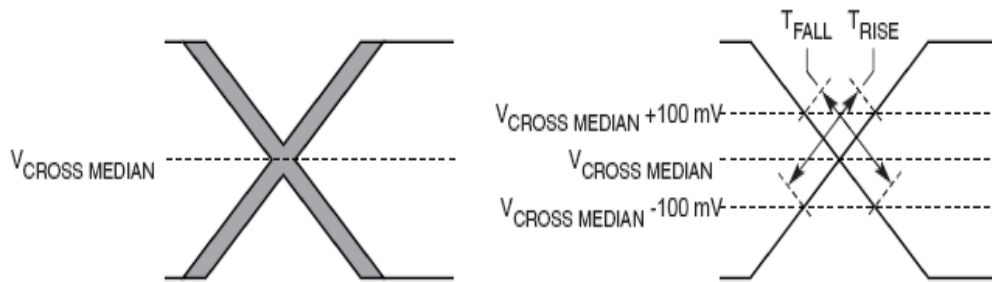


Figure 51. Single-Ended Measurement Points for Rise and Fall Time Matching

2.20.2.4 SerDes Transmitter and Receiver Reference Circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

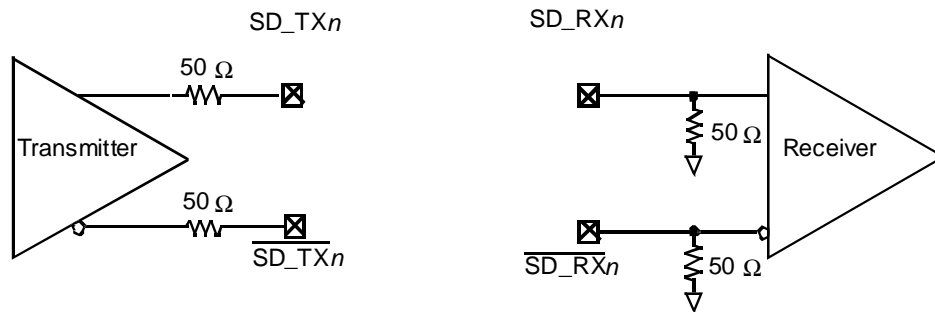


Figure 52. SerDes Transmitter and Receiver Reference Circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below (PCI Express, Serial Rapid IO or SGMII) in this document based on the application usage:

- [Section 2.11.4, “SGMII Interface Electrical Characteristics”](#)
- [Section 2.21, “PCI Express”](#)

Note that an external AC-coupling capacitor is required for the above three serial transmission protocols per the protocol's standard requirements.

2.21 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus.

2.21.1 PCI Express DC Requirements for PCI Express SD_REF_CLK and SD_REF_CLK

For more information, see [Section 2.20.2.2, “DC Level Requirement for SerDes Reference Clocks.”](#)

2.21.2 PCI Express DC Physical Layer Specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.21.2.1 PCI Express DC Physical Layer Transmitter Specifications

This section discusses PCI Express DC physical layer transmitter specifications for 2.5 Gb/s.

This table defines the PCI Express (2.5 Gb/s) DC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins.

Table 75. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output DC Specifications

| Symbol | Parameter | Min | Typical | Max | Units | Comments |
|-------------------|---|-----|---------|------|----------|--|
| $V_{TX-DIFFp-p}$ | Differential Peak-to-Peak Output Voltage | 800 | 1000 | 1200 | mV | $V_{TX-DIFFp-p} = 2 \times V_{TX-D+} - V_{TX-D-} $ See Note 1. |
| $V_{TX-DE-RATIO}$ | De-emphasized Differential Output Voltage (Ratio) | 3.0 | 3.5 | 4.0 | dB | Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1. |
| $Z_{TX-DIFF-DC}$ | DC Differential TX Impedance | 80 | 100 | 120 | Ω | TX DC Differential mode low Impedance |
| Z_{TX-DC} | Transmitter DC Impedance | 40 | 50 | 60 | Ω | Required TX D+ as well as D- DC impedance during all states |

Note:

1. Specified at the measurement point into a timing and voltage compliance test load as shown in [Figure 53](#) and measured over any 250 consecutive TX UIs.

2.21.2.2 PCI Express DC Physical Layer Receiver Specifications

This section discusses PCI Express DC physical layer receiver specifications for 2.5 Gb/s.

This table defines the PCI Express (2.5 Gb/s) DC specifications for the differential output at all receivers (RXs). The parameters are specified at the component pins.

Table 76. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input DC Specifications

| Symbol | Parameter | Min | Typical | Max | Units | Comments |
|---------------------------|---|------|---------|------|----------|--|
| $V_{RX-DIFFp-p}$ | Differential Input Peak-to-Peak Voltage | 175 | — | 1200 | mV | $V_{RX-DIFFp-p} = 2 \times V_{RX-D+} - V_{RX-D-} $ See Note 1. |
| $Z_{RX-DIFF-DC}$ | DC Differential Input Impedance | 80 | 100 | 120 | Ω | RX DC differential mode impedance. See Note 2 |
| Z_{RX-DC} | DC Input Impedance | 40 | 50 | 60 | Ω | Required RX D+ as well as D– DC impedance ($50 \pm 20\%$ tolerance). See Notes 1 and 2. |
| $Z_{RX-HIGH-IMP-DC}$ | Powered Down DC Input Impedance | 50 k | — | — | Ω | Required RX D+ as well as D– DC impedance when the receiver terminations do not have power. See Note 3. |
| $V_{RX-IDLE-DET-DIFFp-p}$ | Electrical Idle Detect Threshold | 65 | — | 175 | mV | $V_{RX-IDLE-DET-DIFFp-p} = 2 \times V_{RX-D+} - V_{RX-D-} $ Measured at the package pins of the receiver |

Notes:

1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 53 should be used as the RX device when taking measurements. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The RX DC common mode Impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the Receiver Detect circuit will not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.

2.21.3 PCI Express AC Physical Layer Specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.21.3.1 PCI Express AC Physical Layer Transmitter Specifications

This section discusses the PCI Express AC physical layer transmitter specifications for 2.5Gb/s.

This table defines the PCI Express (2.5Gb/s) AC specifications for the differential output at all transmitters (TXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 77. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output AC Specifications

| Symbol | Parameter | Min | Typical | Max | Units | Comments |
|--------------|----------------------|--------|---------|--------|-------|--|
| UI | Unit Interval | 399.88 | 400.00 | 400.12 | ps | Each UI is $400 \text{ ps} \pm 300 \text{ ppm}$. UI does not account for spread-spectrum-clock-dictated variations. See Note 1. |
| T_{TX-EYE} | Minimum TX Eye Width | 0.70 | — | — | UI | The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3 \text{ UI}$. See Notes 2 and 3. |

Table 77. PCI Express (2.5Gb/s) Differential Transmitter (TX) Output AC Specifications (continued)

| Symbol | Parameter | Min | Typical | Max | Units | Comments |
|-----------------------------------|---|-----|---------|------|-------|---|
| $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ | Maximum time between the jitter median and maximum deviation from the median. | — | — | 0.15 | UI | Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3. |
| C_{TX} | AC Coupling Capacitor | 75 | — | 200 | nF | All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 4. |

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 53 and measured over any 250 consecutive TX UIs.
3. A $T_{TX-EYE} = 0.70$ UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX} = 0.30$ UI for the Transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. SerDes transmitter does not have CTX built-in. An external AC-coupling capacitor is required.

2.21.3.2 PCI Express AC Physical Layer Receiver Specifications

This section discusses the PCI Express AC physical layer receiver specifications for 2.5 Gb/s.

This table defines the AC specifications for the PCI Express (2.5 Gb/s) differential input at all receivers (RXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 78. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input AC Specifications

| Symbol | Parameter | Min | Typical | Max | Units | Comments |
|--------------|----------------------------|--------|---------|--------|-------|---|
| UI | Unit Interval | 399.88 | 400.00 | 400.12 | ps | Each UI is 400 ps \pm 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1. |
| T_{RX-EYE} | Minimum Receiver Eye Width | 0.4 | — | — | UI | The maximum interconnect media and Transmitter jitter that can be tolerated by the Receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3. |

Table 78. PCI Express (2.5 Gb/s) Differential Receiver (RX) Input AC Specifications (continued)

| Symbol | Parameter | Min | Typical | Max | Units | Comments |
|--|---|-----|---------|-----|-------|--|
| $T_{\text{RX-EYE-MEDIAN-to-MAX-JITTER}}$ | Maximum time between the jitter median and maximum deviation from the median. | — | — | 0.3 | UI | Jitter is defined as the measurement variation of the crossing points ($V_{\text{RX-DIFFP-P}} = 0 \text{ V}$) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3 and 4. |

Notes:

- No test load is necessarily associated with this value.
- Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 53 should be used as the RX device when taking measurements. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
- A $T_{\text{RX-EYE}} = 0.40 \text{ UI}$ provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The $T_{\text{RX-EYE-MEDIAN-to-MAX-JITTER}}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
- It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

2.21.3.3 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in this figure.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

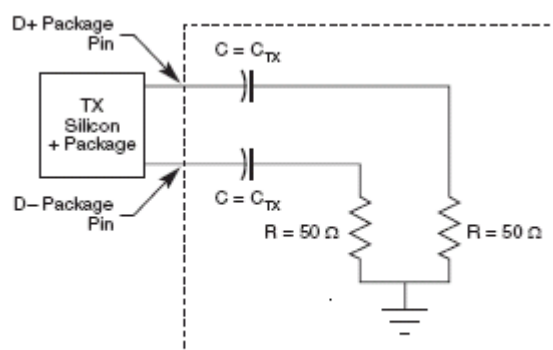


Figure 53. Compliance Test/Measurement Load

3 Thermal

This section describes the thermal specifications.

3.1 Thermal Characteristics

This table provides the package thermal characteristics.

Table 79. Package Thermal Characteristics

| Parameter | JEDEC Board | Symbol | Value | Unit | Notes |
|--|-------------------------|-----------------|-------|------|-------|
| Junction-to-ambient Natural Convection | Single layer board (1s) | $R_{\theta JA}$ | 23 | °C/W | 1, 2 |
| Junction-to-ambient Natural Convection | Four layer board (2s2p) | $R_{\theta JA}$ | 17 | °C/W | 1, 2 |
| Junction-to-ambient (at 200 ft/min) | Single layer board (1s) | $R_{\theta JA}$ | 18 | °C/W | 1, 2 |
| Junction-to-ambient (at 200 ft/min) | Four layer board (2s2p) | $R_{\theta JA}$ | 14 | °C/W | 1, 2 |
| Junction-to-board thermal | — | $R_{\theta JB}$ | 9 | °C/W | 3 |
| Junction-to-case thermal | — | $R_{\theta JC}$ | 7 | °C/W | 4 |
| Junction-to-package top thermal | Natural Convection | Ψ_{JT} | 7 | °C/W | 5 |

Notes

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 and JESD51-6 with the board (JESD51-9) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.2 Temperature Diode

The device have a thermal diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as On Semiconductor, NCT1008™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment.

The following are the specifications of the P1011 on-board temperature diode:

Operating range: 10 – 230 μ A

Ideality factor over 13.5 – 220 μ A; $n = 1.006 \pm 0.008$

4 Package Information

This section provides the package parameters and ordering information.

4.1 Package Parameters for the P1011 WB-TePBGA II

The package parameters are provided in the following list. The package type is 31 mm × 31 mm, 689 plastic ball grid array (WB-TePBGA II).

Package outline

31 mm × 31 mm

| | |
|-------------------------|-----------------------------|
| Interconnects | 689 |
| Pitch | 1.00 mm |
| Module height | 2.0 mm to 2.46 mm (Maximum) |
| Solder Balls | 3.5% Ag, 96.5% Sn |
| Ball diameter (typical) | 0.60 mm |

This figure shows the P1011 package.

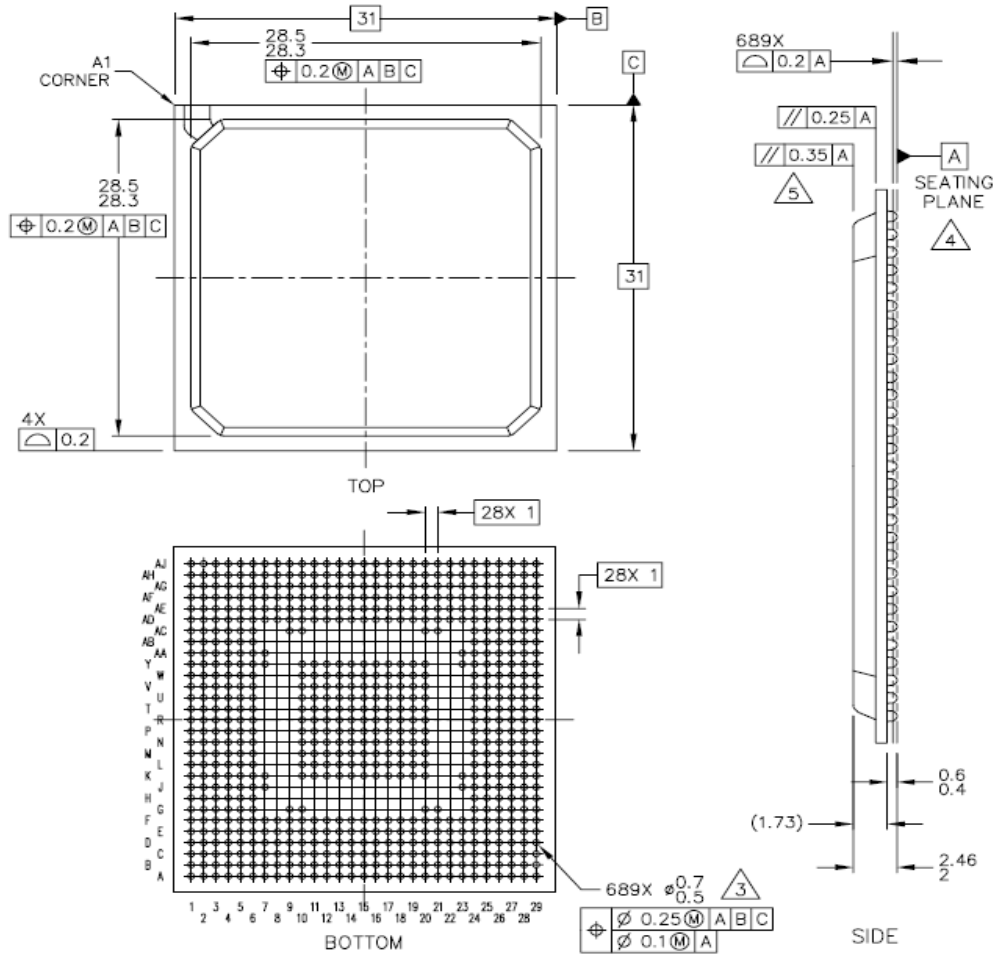
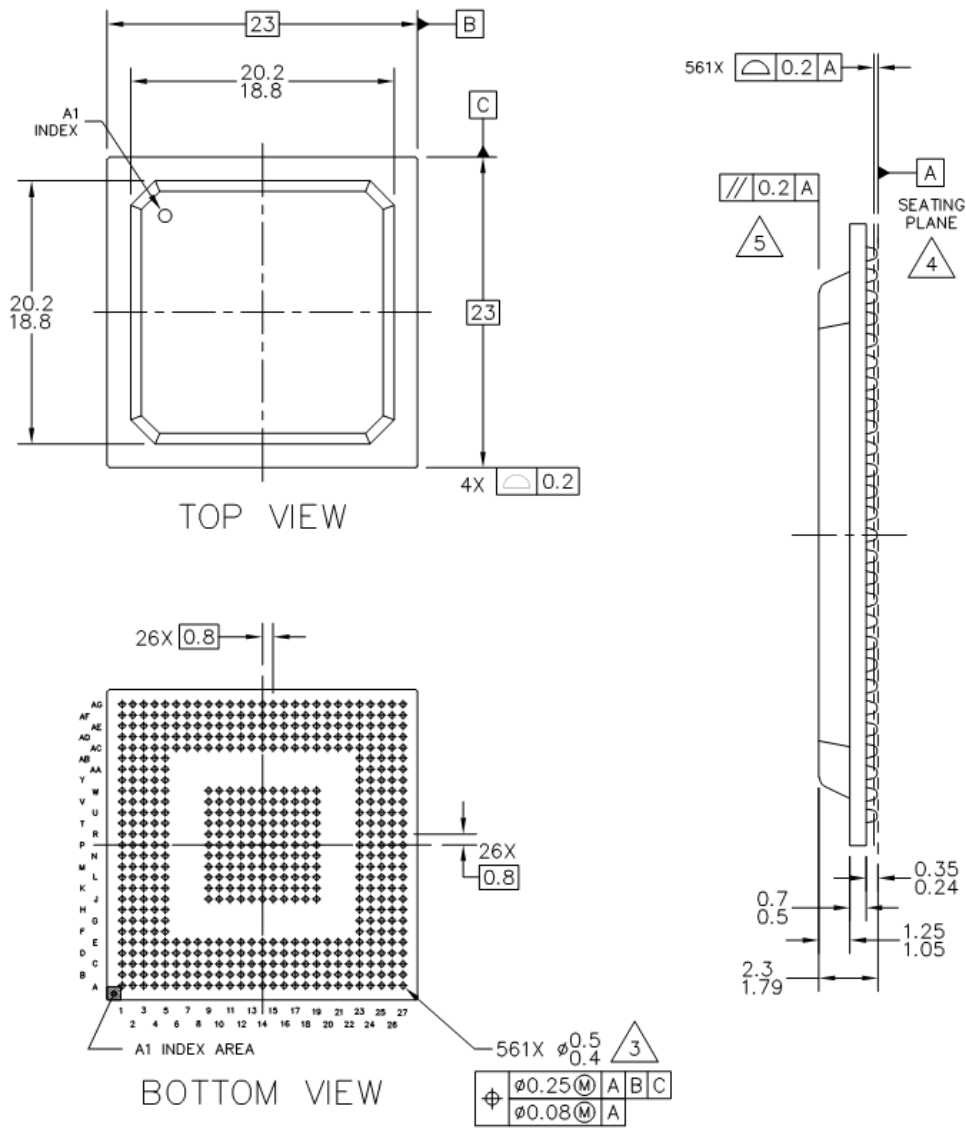


Figure 54. P1011 Package

NOTES for Figure 54:

1. All dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14. 5M-1994.
3. Maximum solder ball diameter measured parallel to Datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

Package Information



Notes:

1. All dimensions are in millimeters.
2. Dimensioning and tolerancing per ASME Y14. 5M-1994.
3. Maximum solder ball diameter measured parallel to Datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

4.2 Ordering Information

This table provides the Freescale part numbering nomenclature. Each part number also contains a revision code which refers to the die mask revision number.

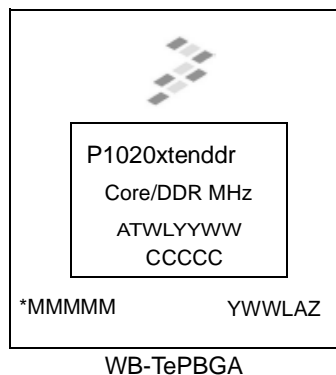
Table 80. Part Numbering Nomenclature

| P | 1 | 02 or 01 | 1 | q | t | e | n | dd | r |
|----------------|----------|--|----------------|--|-------------------------------|---|-------------------------------|--|--------------------|
| Generat ion | Platform | Number of Cores | Deriva tive | Qual Status | Temperature Range | Encryptio n | Package Type | CPU/CCB/DDR Frequency (MHz) | Die Revisio n |
| P = 45 nm | 1 | 01 = Single Core 02 = Dual Core | 0-9 | P = Prototype N = Qual'd to Industrial Tier S = Special | S = Std Temp X = Ext. Temp | E = SEC Present N = SEC Not Present | 2 = TePBGA II Pbfree | HF = 800/400/667 FF = 667/333/667 DF = 533/267/667 | A = 1.0 B = 1.1 |

Notes:

1. See [Section 4, "Package Information,"](#) for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

Parts are marked as the example shown in this figure.



Notes:

- P1020xtenddr is the orderable part number
- *MMMMM is the mask number
- YWWLAZ is the assembly traceability code.
- CCCCC is the country code
- ATWLYYWW is the standard assembly, test, year, and work week codes.

Figure 55. Part Marking for WB-TePBGA II Device

5 Product Documentation

The following documents are required for a complete description of the device and are needed to design properly with the part:

- *P1020 QorIQ Integrated Processor Reference Manual* (document number P1020RM)
- e500 PowerPC Core Reference Manual (E500CORERM)

6 Revision History

This table provides revision history for this document.

Table 81. Document Revision History

| Rev. Number | Date | Substantive Change(s) |
|-------------|---------|--|
| 1 | 03/2012 | <ul style="list-style-type: none"> • In Table 1, replaced the signals NC107, NC108, and NC109 (along with their details, such as Package Pin Number, Pin Type, and Power Supply) with the signals CKSTP_IN1_B, CKSTP_OUT1_B, and READY_P1 respectively. • Changed the power supply from XVDD_SRDS to SVDD_SRDS for all SD_RX_n pins as well as SD_REF_CLK and SD_REF_CLK_B in Table 1. • Changed Note 13 in Table 1. The note says "These pins must NOT be pulled down by a resistor or the component they are connected to during power-on reset". • Added Table 18. • In Table 30, made the following changes: <ul style="list-style-type: none"> • Changed the min value of 'SPI outputs—Master data (internal clock) hold time' from 0.5 to the formula: $0.5 + (t_{\text{PLATFORM_CLK}} * \text{SPMODE} [\text{HO_ADJ}])$. • Changed the max value of 'SPI outputs—Master data (internal clock) delay' from 6.0 to the formula: $0.5 + (t_{\text{PLATFORM_CLK}} * \text{SPMODE} [\text{HO_ADJ}])$. • Added note 3 that reads: See the P1025 QorIQ Integrated Processor Reference Manual for detail about the register SPMODE. • In Table 41, changed "LSTS = 0" to "LSTS = 001" and changed "LSTS = 1" to "LSTS = 100" • In Table 41, changed note 4 to "The LSTS shown in the table refers to the EIC2[0:2] or EIC3[0:2] bit field of the GUTS_SRDSR4 register, depending on the SerDes lane usage" • Modified Figure 21. • Changed value of minimum AC coupling capacitor from 5nF to 10nF and removed typical value of 100nF in Table 42. • Changed min frequency of DRCLK from 66.7Mhz to 66.66MHz. • Changed pin E16 from NC20 to THERM1 (Internal Diode Anode) and pin E15 from NC21 to THERM0 (Internal Diode Cathode) and added Note 26 in Table 1. Also added THERM0 and THERM1 in ball map. • Added Section 3.2, "Temperature Diode". • Updated Figure 14. • Removed "Measured at 1.6 V" from "SD_REF_CLK/ SD_REF_CLK reference clock duty cycle" cell of Table 74. • In Table 49, changed min value of t_{T1588CLK} from 3.8 to 5. • Added Section 2.11.6.1, "eTSEC IEEE Std 1588 DC Electrical Characteristics". • Changed input leakage current of all interfaces to +50uA. |
| 0 | 08/2011 | Initial release |

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