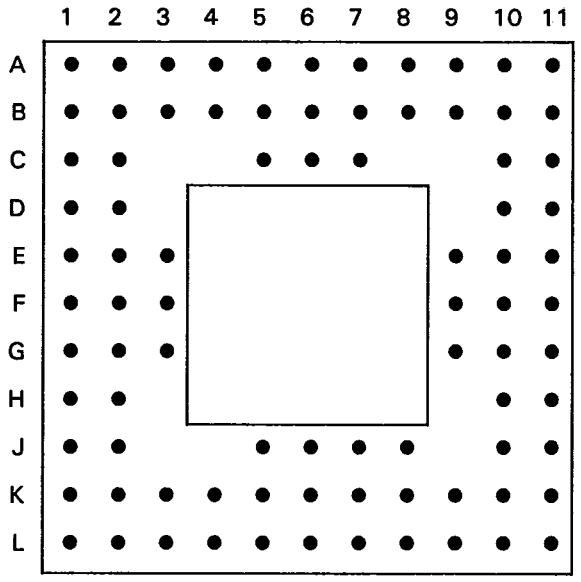
TIET890A MICROSEQUENCER

D3111, APRIL 1988—REVISED AUGUST 1988

- **IMPACT-X™ Technology with TTL I/O Compatibility**
- **14 Bits Wide—Addresses Up to 16,384 Words of Microcode with One Chip**
- **Selects Address from One of Eight Sources**
- **Independent Read Pointer for Aid in Microcode Diagnostics**
- **Supports Real-Time Interrupts**
- **Two Independent Loop Counters**
- **Supports 64 Powerful Instructions**

TIET890A . . . GA PACKAGE
(TOP VIEW)



description

The TIET890A is a powerful microsequencer that is implemented using Texas Instruments IMPACT-X™ technology providing ECL internal circuitry with TTL input and output compatibility. It is functionally equivalent to the SN74AS890 and requires a 5-volt power supply.

The microsequencer selects a 14-bit microaddress from one of eight sources to provide the proper microinstruction sequence for bit-slice processor or other microcode based systems. These high-performance devices are capable of addressing 16,384 control store memory locations either sequentially or via conditional branching algorithms. This multiway branching capability, coupled with a nine-word-deep LIFO (last in, first out) stack, allows the microprogrammer to arrange his code in blocks so that microprograms may be structured in the same fashion as such high-level languages as ALGOL, Pascal, or Ada.

Both polled and real-time interrupt routines are supported by the TIET890A to enhance system throughput capability. Vectored interrupts may occur during any instruction, including PUSHes and POPs.

Two 14-bit loadable registers/counters may be used for temporary storage of data or utilized as down counters for iterative instructions such as multiplication and division or as loop counters when iterative routines are required.

TIET890A PIN ALLOCATIONS

PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
A1	GND	D1	Y12	J6	V_{CC}
A2	DRB10	D2	Y9	J7	GND
A3	DRB9	D10	S2	J8	GND
A4	DRB8	D11	S0	J10	RC2
A5	DRB7	E1	Y11	J11	OSEL
A6	DRB6	E2	Y8	K1	Y1
A7	DRB5	E3	V_{CC}	K2	Y0
A8	DRB4	E91	V_{CC}	K3	B1
A9	DRB3	E10	NC	K4	DRA13
A10	DRB1	E11	RC0	K5	DRA11
A11	GND	F1	Y7	K6	DRA8
B1	DRB13	F2	GND	K7	DRA7
B2	$\overline{INT}$	F3	V_{CC}	K8	DRA0
B3	DRB12	F9	GND	K9	DRA1
B4	DRB11	F10	V_{CC}	K10	DRA3
B5	B3	F11	MUX2	K11	DRA2
B6	$\overline{RBOE}$	G1	Y5	L1	GND
B7	DRB2	G2	$\overline{YOE}$	L2	B2
B8	DRB0	G3	GND	L3	INC
B9	STKWRN/RER	G9	V_{CC}	L4	DRA12
B10	ZERO	G10	RC1	L5	DRA10
B11	CLK	G11	MUX1	L6	DRA9
C1	Y13	H1	Y4	L7	$\overline{RAOE}$
C2	Y10	H2	Y6	L8	DRA6
C5	GND	H10	B0	L9	DRA5
C6	V_{CC}	H11	MUX0	L10	DRA4
C7	GND	J1	Y3	L11	GND
C10	$\overline{CC}$	J2	Y2		
C11	S1	J5	GND		

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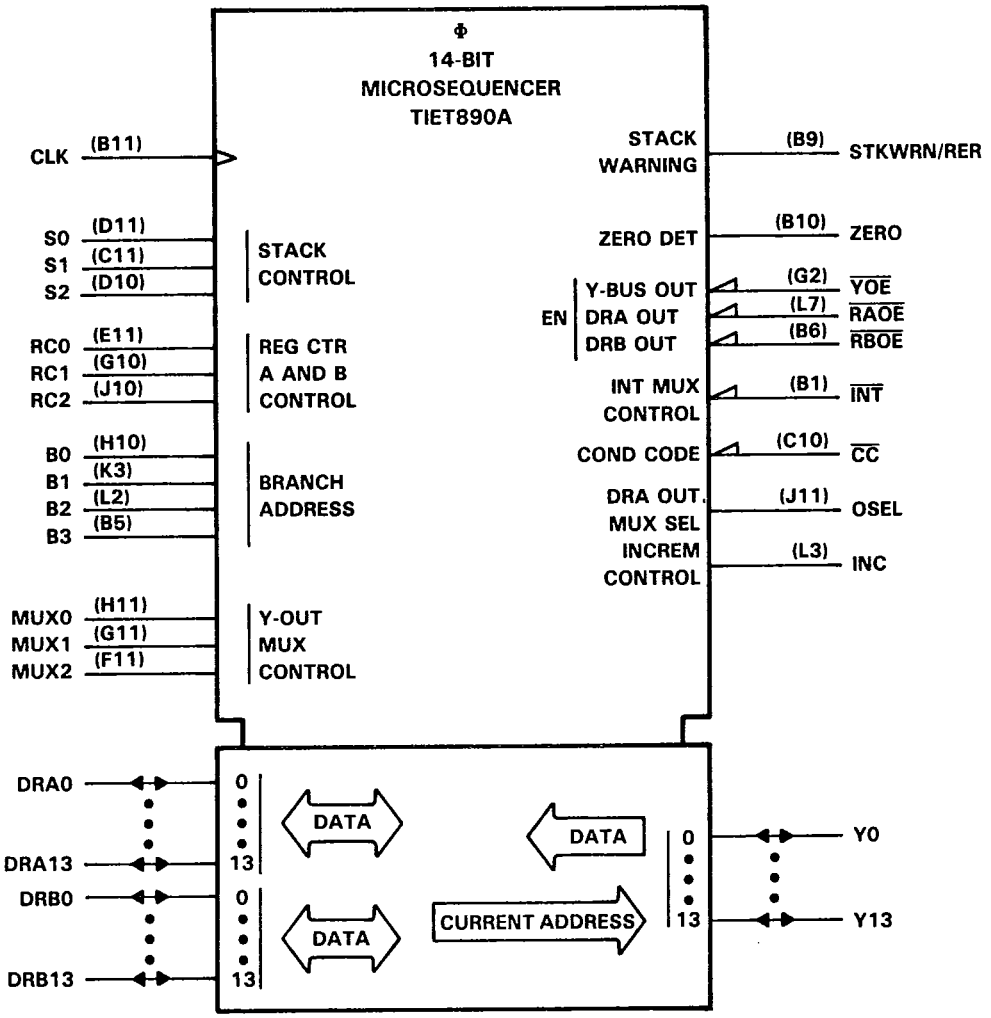
description (continued)

An additional feature is a 4-bit port that appends four user-definable bits to the DRA or DRB address value for support of 16-way branches for the execution of relative branch addressing schemes.

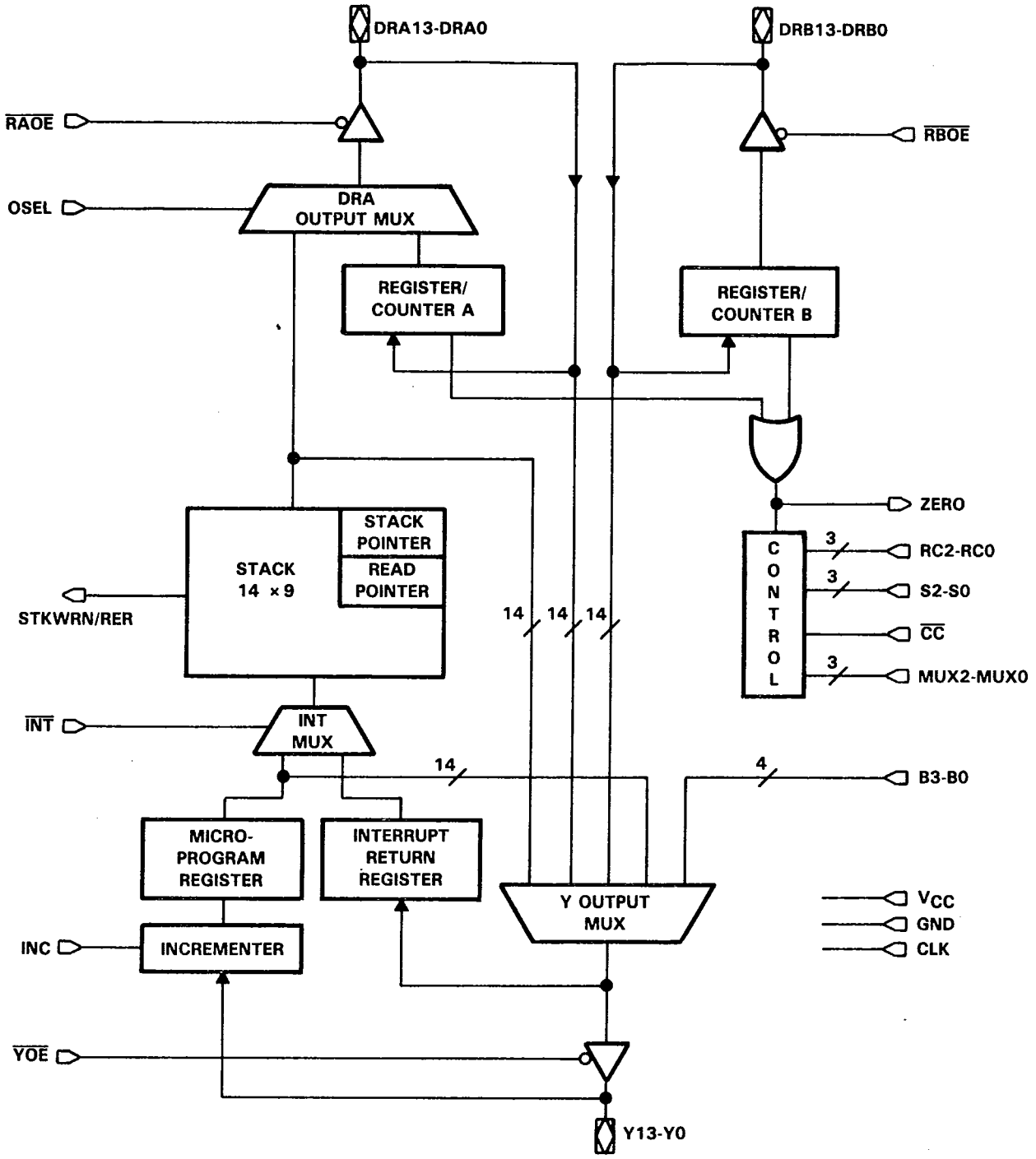
The TIET890A is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984.

functional block diagram (positive logic)



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PIN NAME	PIN NO.	I/O	DESCRIPTION
B0	H10	I	Input bits for 16-way branch
B1	K3		
B2	L2		
B3	B5		
$\overline{CC}$	C10	I	Condition code
CLK	B11	I	Clock active on low-to-high transition
DRA0	K8	I/O	Bidirectional DRA data port
DRA1	K9		
DRA2	K11		
DRA3	K10		
DRA4	L10		
DRA5	L9		
DRA6	L8		
DRA7	K7		
DRA8	K6		
DRA9	L6		
DRA10	L5		
DRA11	K5		
DRA12	L4		
DRA13	K4		
DRB0	B8	I/O	Bidirectional DRB data port
DRB1	A10		
DRB2	B7		
DRB3	A9		
DRB4	A8		
DRB5	A7		
DRB6	A6		
DRB7	A5		
DRB8	A4		
DRB9	A3		
DRB10	A2		
DRB11	B4		
DRB12	B3		
DRB13	B1		
GND	A1		Ground pins. All pins must be used. J8 is internally connected to J7.
GND	A11		
GND	C5		
GND	C7		
GND	F2		
GND	F9		
GND	G3		
GND	J5		
GND	J7 (J8)		
GND	L1		
GND	L11		
INC	L3	I	Incrementer control pin
$\overline{INT}$	B2	I	Selects INT RT register to stack, active low
MUX0	H11	I	MUX control for Y output bus (See Table 1)
MUX1	G11		
MUX2	F11		

PIN NAME	PIN NO.	I/O	DESCRIPTION
OSEL	J11	I	MUX control for the source to DRA. Low selects RA, high selects stack.
$\overline{\text{RAOE}}$	L7	I	DRA output enable, active low
$\overline{\text{RBOE}}$	B6	I	DRB output enable, active low
RC0	E11	I	Register/Counter controls (See Table 3)
RC1	G10		
RC2	J10		
S0	D11	I	Stack control (See Table 2)
S1	C11		
S2	D10		
STKWRN/RER	B9	O	Stack overflow, underflow/read error flag
VCC	C6		5-volt power supply
V_{CC}	E3		
V_{CC}	E9		
V_{CC}	F3		
V_{CC}	F10		
V_{CC}	G9		
V_{CC}	J6		
Y0	K2	I/O	Bidirectional Y data port
Y1	K1		
Y2	K2		
Y3	J1		
Y4	H1		
Y5	G1		
Y6	H2		
Y7	F1		
Y8	E2		
Y9	D2		
Y10	C2		
Y11	E1		
Y12	D1		
Y13	C1		
$\overline{\text{YOE}}$	G2		Y output bus enable, active low
ZERO	B10		Zero detect flag for register A and B

PRINCIPLES OF OPERATIONS

Y output multiplexer

The Y output multiplexer of the TIET890A is capable of selecting the next branch address from one of eight locations. Addresses may be sourced from:

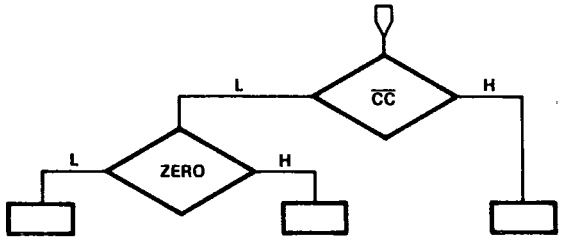
1. The top of the 14-bit by 9-word address stack
2. An external input on the DRA port, potentially a pipeline register
3. An external input on the DRB port, potentially a pipeline register
4. Internal register/counter A
5. Internal register/counter B
6. An internal microprogram counter (MPC register)
7. An external input onto the bidirectional Y output port
8. A 16-way branch—4 bits appended to DRA, DRB, register/counter A or register/counter B.

The source of the next address is dependent upon the previous state of the microsequencer, the MUX controls (MUX2-MUX0), the condition code ($\overline{CC}$) input, and the state of an internal status flag (status externally available at the ZERO output) that indicates that one of the on-chip registers is being decremented to zero.

The entire instruction set may be made conditional by manipulation of the condition code ($\overline{CC}$) input. Allowing the $\overline{CC}$ value to vary as a result of data or status provides for state-dependent or data-dependent branching. Unconditional branches may be achieved by forcing $\overline{CC}$ high when selecting control store addresses. Holding this pin low will provide for conditional or unconditional branches as dictated by the state of the zero-detect flag. The required control signals for selection of the Y output source are listed in Table 1. Note that the dependence of the TIET890A on two variables for conditional branches and jumps allows a conditional branch or conditional jump to subroutine in any clock cycle. Also note that all multiplexer inputs are overridden when all of the stack control inputs are pulled low. This instruction resets the stack and read pointers to zero and places all lines of the Y output bus at the low level.

TABLE 1. Y OUTPUT CONTROL

MUX CONTROL			RESET*	Y OUTPUT SOURCE		Y OUTPUT SOURCE
MUX2	MUX1	MUX0		$\overline{CC}$ = L ZERO = L	$\overline{CC}$ = L ZERO = H	$\overline{CC}$ = H
X	X	X	YES	ALL LOW	ALL LOW	ALL LOW
L	L	L	NO	STK	MPC	DRA
L	L	H	NO	STK	MPC	DRB
L	H	L	NO	STK	DRA	MPC
L	H	H	NO	STK	DRB	MPC
H	L	L	NO	DRA	MPC	DRB
H	L	H	NO	DRA' (16-WAY BRANCH)	MPC	DRB' (16-WAY BRANCH)
H	H	L	NO	DRA	STK	MPC
H	H	H	NO	DRB	STK	MPC



H = high level, L = low level, X = irrelevant.
*Reset command is implemented by setting S2-S0 = LLL.

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14-bit by 9-word address stack

The positive-edge-triggered 14-bit address stack supplies on-board storage of nine control store addresses that support up to nine nested levels of microsubroutine, looping, and real-time interrupt functions. The stack pointer (SP), which operates as an up-down counter, is updated after the execution of each PUSH operation and before each POP. In a PUSH operation, the address stored in the selected register (either MPC or INT RT) is loaded into the stack location addressed by the stack pointer, and the stack pointer is incremented. This address is available at the DRA port by enabling DRA ($\overline{RAOE}$ low and OSEL high).

A POP operation causes the stack pointer to be decremented on the first rising clock edge following the arrival of the POP instruction at the S2-S0 pins. The value that was indexed by the stack pointer is effectively removed from the top of the stack. All PUSH and POP instructions are conditionally dependent upon the stack control inputs (S2-S0), the condition code ($\overline{CC}$), the input value, and the zero-detect status. The desired option may be selected using the stack control inputs listed in Table 2.

TABLE 2. STACK CONTROL

STACK CONTROL			STACK OPERATION, $\overline{CC}$ = L			
S2	S1	S0	OSEL	ZERO = L	ZERO = H	$\overline{CC}$ = H
L	L	L	X	RESET/CLEAR	RESET/CLEAR	RESET/CLEAR
L	L	H	X	CLEAR SP, RP	HOLD	HOLD
L	H	L	X	HOLD	POP	POP
L	H	H	X	POP	HOLD	HOLD
H	L	L	X	HOLD	PUSH	PUSH
H	L	H	X	PUSH	HOLD	HOLD
H	H	L	X	PUSH	HOLD	PUSH
H	H	H	H	READ	READ	READ
H	H	H	L	HOLD	HOLD	HOLD

The read pointer (RP) is a useful tool in debugging microcoded systems. A microprogrammer now has the ability to perform a nondestructive, sequential read of the stack contents from the DRA port. This capability provides the user with a method of backtracking through the address sequence to determine the cause of overflow without affecting program flow, the status of the stack-pointer or the internal data of the stack. Placing a high value on all of the stack inputs (S2-S0) and OSEL places the TIET890A into the read mode. At each low-to-high clock transition, the value pointed to by the read pointer is available at the DRA port and the read pointer is decremented. Microcode diagnostics are simplified by the ability of the TIET890 to sequentially dump the contents of its stack. The bottom of the stack is detected by monitoring the STKWRN/RER (stack warning/read error) pin. A high will appear when the stack contains one word and a READ instruction is applied to the S2-S0 pins. This signifies that the last address has been read. The stack pointer and stack contents are unaffected by the READ operation. Under normal PUSH and POP operations the read pointer is updated with the stack pointer and contains identical information.

The STKWRN/RER pin alerts the system to a potential stack overflow or underflow condition. STKWRN/RER becomes active under two additional conditions. If seven of the nine stack locations (0-8) are full (the stack pointer is at 7) and a PUSH occurs, the STKWRN/RER pin will produce a high-level signal to warn that the stack is approaching its capacity, and will be full after one more PUSH. Knowledge that overflow potential exists allows bit-slice-based systems to continuously process real-time interrupt vectors. This signal will remain high, if HOLD, PUSH, or POP instructions occur, until the stack pointer is decremented to 7.

The user may be protected from attempting to POP an empty stack by monitoring STKWRN/RER before POP operations. A high level at this pin signifies that the last address has been removed from the stack (SP = 0). This condition remains until an address is pushed onto the stack and the stack pointer is incremented to one.

Clearing the stack and read pointer is accomplished by placing low levels onto the stack control lines (S2-S0). This function overrides all of the Y output MUX controls and places the Y bus into a low state.

register/counters

Two loadable 14-bit registers extend the looping and branching capabilities. Addresses may be loaded directly into register/counter A (RA) and register/counter B (RB) through the direct data ports DRA13-DRA0 and DRB13-DRB0. The values stored in these registers may either be held, decremented, or read as a result of the register control inputs (RC2-RC0), $\overline{\text{RAOE}}$, and $\overline{\text{RBOE}}$. All combinations of these functions are supported with the exception of a simultaneous decrement of both registers. Generation of iteration routines may be accomplished by loading RA and/or RB and operating them as a down counter. Loop termination is acknowledged by the ZERO output going high to indicate that a register contains a binary one and that a decrement is about to take place. Because of this facility, a "decrement and branch on loop termination" may be executed in the same clock cycle.

The contents of RA are accessible to the DRA port when OSEL is low and the output bus is enabled by $\overline{\text{RAOE}}$ being low. Data from RB is available when DRB is enabled by $\overline{\text{RBOE}}$ being low. Note that control of the registers is maintained while an external value is active on the DRA and DRB ports. A value being directed from the DRA and DRB buses to the output will not inhibit the decrement operation.

Register/counter controls are listed in Table 3.

TABLE 3. REGISTER CONTROL

RC2	RC1	RC0	REG A	REG B
L	L	L	HOLD	HOLD
L	L	H	DEC	HOLD
L	H	L	LOAD	HOLD
L	H	H	DEC	LOAD
H	L	L	LOAD	LOAD
H	L	H	HOLD	DEC
H	H	L	HOLD	LOAD
H	H	H	LOAD	DEC

microprogram register and increment

The microprogram register (MPC) and the incrementer (INC) provide the means for generating the next microprogram address for sequential addressing operations. The MPC may be loaded with either the outgoing address on the Y bus or may receive an external address for processing interrupt vectors.

The current address on the Y bus is passed to the MPC at each rising clock edge, either unaltered (INC low) for repeating statements, or incremented by one (INC high) for addressing sequential control store locations.

The MPC may also be externally loaded for subroutine and interrupt functions. Taking $\overline{\text{YOE}}$ high and forcing the new address onto the bidirectional Y bus loads the MPC with the new address at the positive clock edge. This value may also be incremented prior to storage in the MPC for sequential addressing of subroutines or interrupt routines.

interrupts

Real-time vectored interrupt routines are supported for those applications where polling would impede system throughput. Any instruction, including PUSHes and POPs, may be interrupted. To process an interrupt, the following procedure should be followed:

1. The bidirectional Y bus is placed into the high-impedance state by forcing $\overline{\text{YOE}}$ high.
2. The interrupt entry point vector is then forced onto the Y bus and incremented to become the second microinstruction of the interrupt routine. This is accomplished by making INC high.

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3. At the following clock edge, the second microaddress is stored in the MPC and the interrupted address will be stored in the INT RT register which always contains the outgoing value from the Y mux. This edge also causes the processor to begin execution of the first instruction of the interrupt routine. This first instruction must PUSH the address stored in the INT RT register onto the stack so that the proper return linkage is maintained. This is accomplished by making $\overline{\text{INT}}$ low and performing a PUSH. If this instruction were to be interrupted, the process would be repeated and the proper return linkage preserved.

control inputs

A listing of the response of internal elements to various control inputs is given in Table 4.

TABLE 4. RESPONSE TO CONTROL INPUTS

PIN NAME	LOGIC LEVEL	
	HIGH	LOW
$\overline{\text{RAOE}}$	DRA output in high-Z state	DRA output is active
$\overline{\text{RBOE}}$	DRB output in high-Z state	DRB output is active
$\overline{\text{YOE}}$	Y output in high-Z state	Y output is active
$\overline{\text{INT}}$	MPC to stack	INT RT register to stack
OSEL	Stack to DRA buffer input	RA to DRA buffer input
INC	Adds one to Y output and stores in MPC	Passes Y output to MPC unaltered
MUX2-MUX0	Table 1	Table 1
S2-S0	Table 2	Table 2
RC2-RC0	Table 3	Table 3

instruction set

Sixty-four microsequencing instructions enable the TIET890A to generate micro-addresses for up to 16,384 locations. Any instruction can be made conditional depending upon the value of the externally applied condition code ($\overline{\text{CC}}$) and the value stored in either of the internal register/counters.

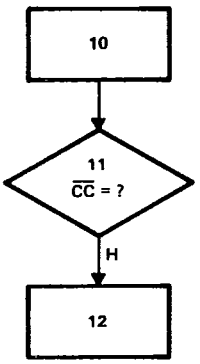
The required signals for selection of the Y output source were listed in Table 1. Suggested methods for implementing a few commonly used instructions are given in Table 5 and flowcharts showing execution examples are illustrated in Figure 1.

It should be noted that the term jump refers to a subroutine call that must be accompanied by a return instruction. The term branch implies that a deviation from the program flow is accomplished but no return is required.

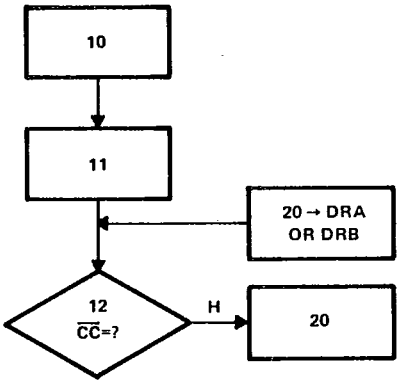
TABLE 5. SUGGESTED CODING FOR REPRESENTATIVE INSTRUCTIONS

FUNCTION	MNEMONIC	MUX2	MUX1	MUX0	S2	S1	S0	$\overline{CC}$	FIGURE
Continue	CONT	X	H	X	H	H	H	H	1(a)
Unconditional branch	BR	L	L	X	H	H	H	H	1(b)
Conditional branch	CBR	H	H	X	H	H	H	V	1(c)
Three-way branch	BR2W	H	L	L	H	H	H	V	1(d)
Conditional loop on stack	LOOPS	L	L	X	L	H	L	L	1(e)
Repeat	REPEAT	L	L	X	H	H	H	L	1(f)
Loop on stack with exit	LSWE	L	L	X	L	H	L	V	1(g)
Conditional jump to subroutine	CJSR	H	H	X	H	L	H	V	1(h)
Jump to subroutine	JSR	L	L	X	H	L	H	H	1(i)
Two-way jump to subroutine	JSR2W	H	L	L	H	H	L	V	1(j)
Repeat until	UNTIL	L	H	X	L	H	L	V	1(k)
Return from subroutine	RTS	L	H	X	L	H	H	L	1(l)
Conditional return from subroutine	CRTS	L	H	X	L	H	H	V	1(m)
Conditional return from subroutine or branch	CRTSB	L	H	X	L	H	H	V	1(n)
Conditional branch and PUSH	CBRP	H	H	X	H	L	H	V	1(o)
Conditional branch and POP	CBRPO	H	H	X	L	H	H	V	1(p)
PUSH and continue	PUSH	L	H	X	H	L	L	H	1(q)
POP and continue	POP	X	H	X	L	H	L	H	1(r)
Exit from loop	EXITLP	L	L	X	L	H	L	V	1(s)
Reset and clear stack/read pointer	RESET	X	X	X	L	L	L	X	1(t)
32-way branch	BR32W	H	L	H	H	H	H	V	1(u)
Execute n times	NEX	L	L	X	L	H	L	L	1(v)

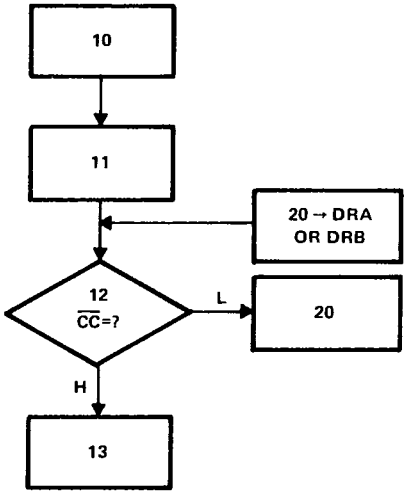
H = high level, L = low level, X = irrelevant, V = varies (condition code value is dependent upon machine and data status and will vary accordingly).



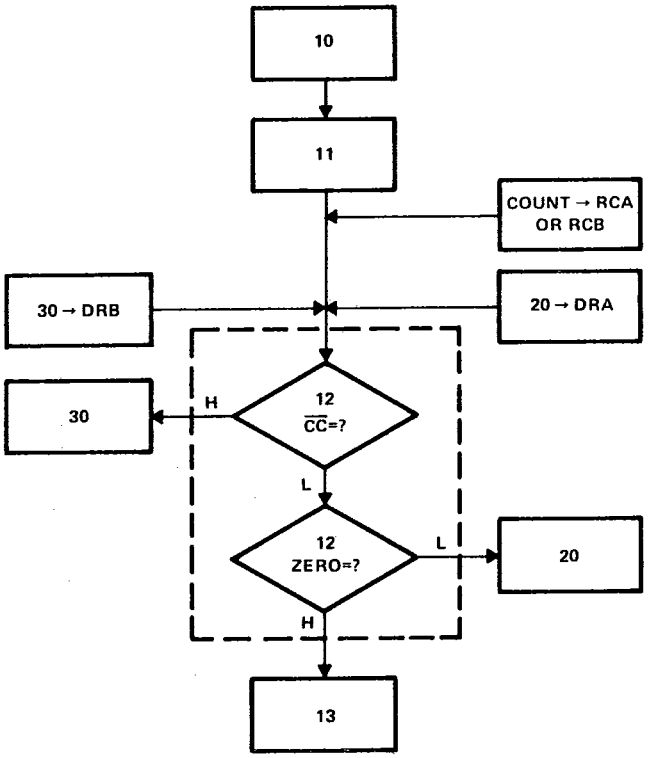
(a) CONTINUE ($\overline{CC}$ FORCED)



(b) UNCONDITIONAL BRANCH ($\overline{CC}$ FORCED)



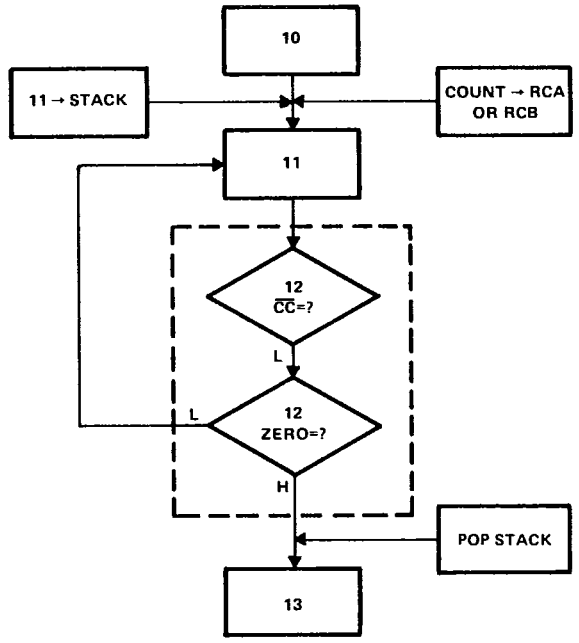
(c) CONDITIONAL BRANCH (DEC DISABLED)



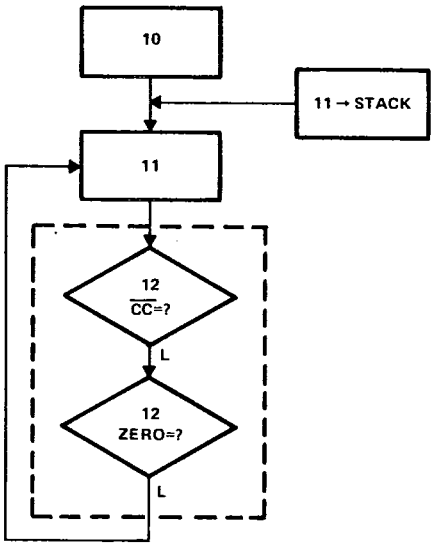
(d) THREE-WAY BRANCH (DEC ENABLED)†

†$\overline{CC}$ and ZERO are completed in the same clock cycle.

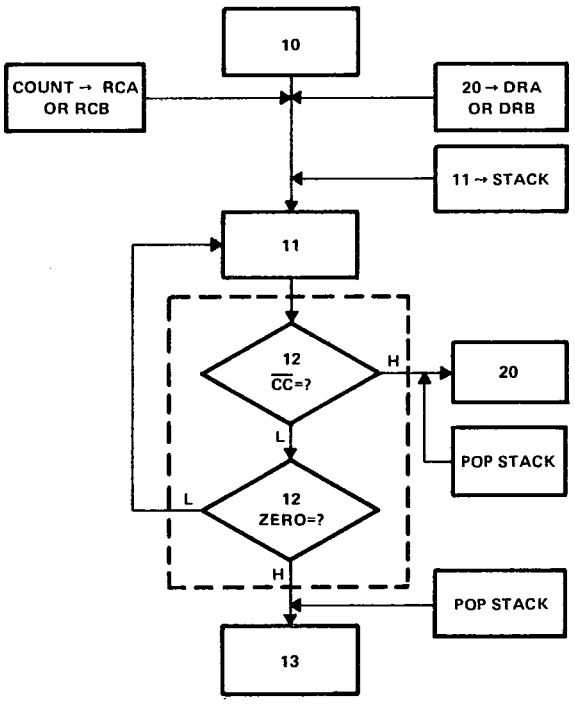
FIGURE 1. INSTRUCTION SET FLOWCHARTS



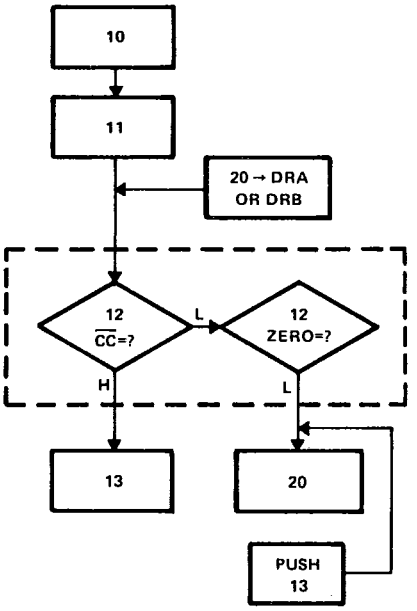
(e) CONDITIONAL LOOP ON STACK ($\overline{CC}$ FORCED, DEC ENABLED)†



(f) REPEAT ($\overline{CC}$ FORCED, DEC DISABLED)†



(g) CONDITIONAL LOOP ON STACK WITH EXIT (DEC ENABLED)†



(h) CONDITIONAL JUMP TO SUBROUTINE (DEC DISABLED)†

†$\overline{CC}$ and ZERO are completed in the same clock cycle.

FIGURE 1. INSTRUCTION SET FLOWCHARTS (continued)

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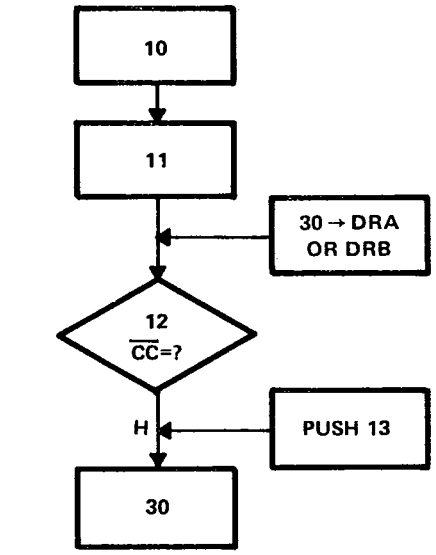
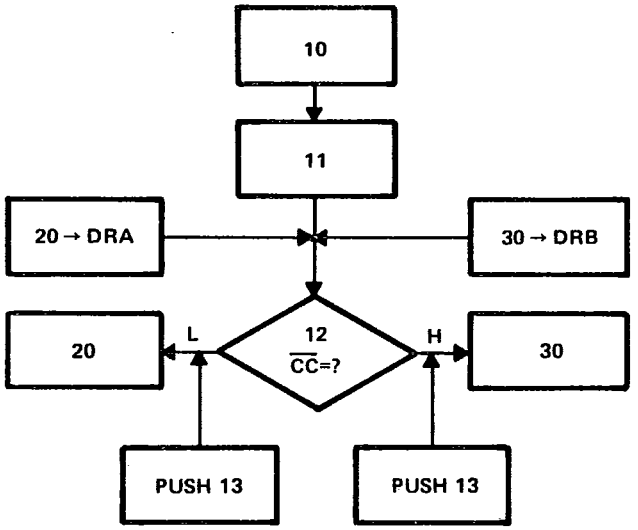
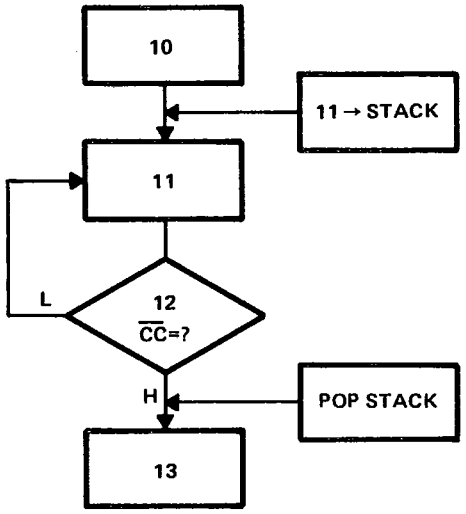


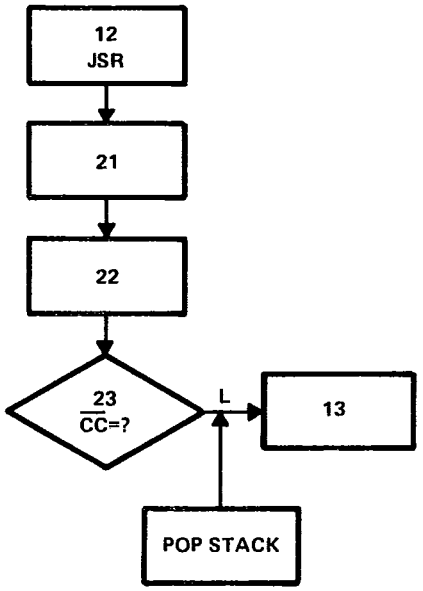
(i) JUMP TO SUBROUTINE (CC FORCED)



(j) TWO-WAY JUMP TO SUBROUTINE (DEC DISABLED)

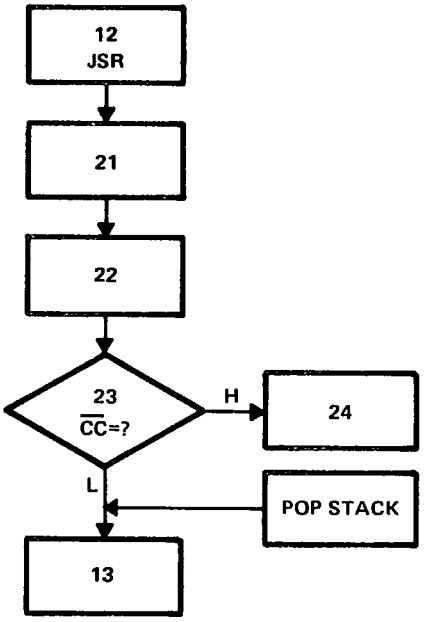


(k) REPEAT UNTIL (DEC DISABLED)

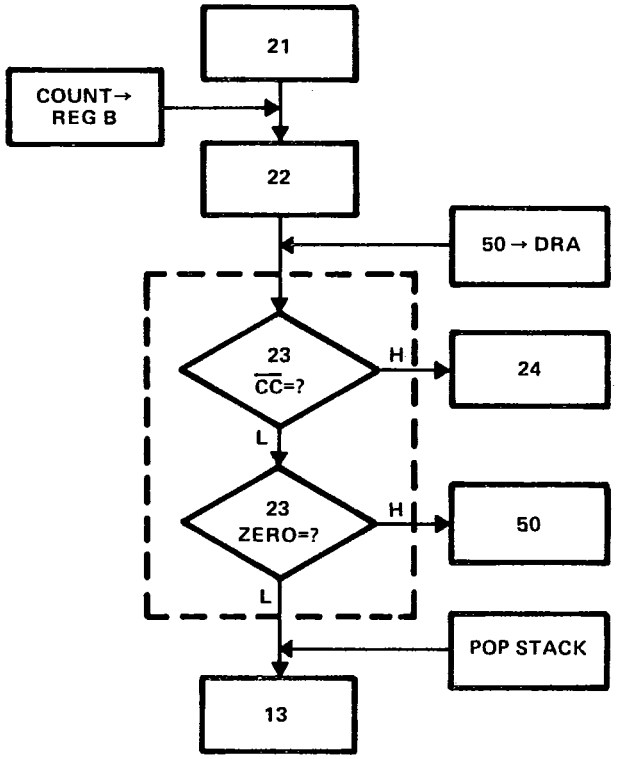


(l) RETURN FROM SUBROUTINE (CC FORCED, DEC DISABLED)

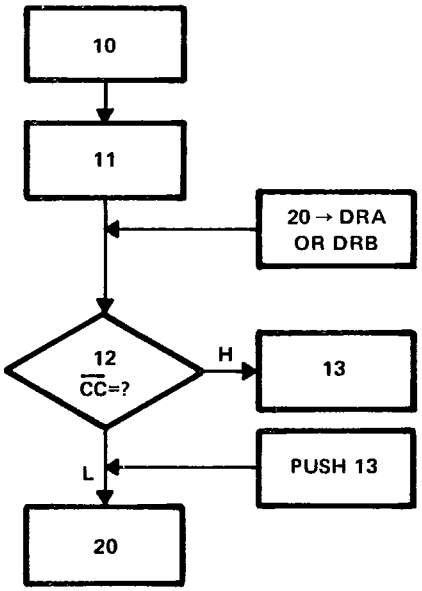
FIGURE 1. INSTRUCTION SET FLOWCHARTS (continued)



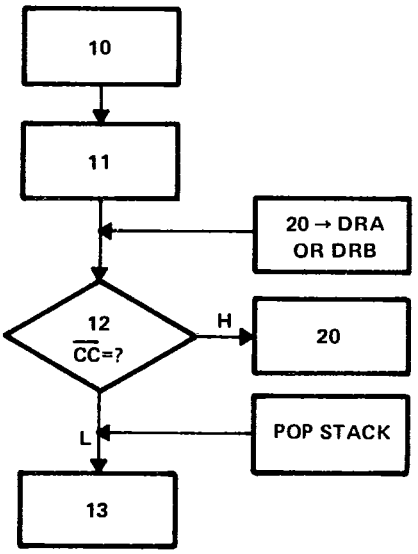
(m) CONDITIONAL RETURN FROM SUBROUTINE (DEC DISABLED)



(n) CONDITIONAL RETURN FROM SUBROUTINE OR BRANCH (DEC ENABLED)†



(o) CONDITIONAL BRANCH AND PUSH (DEC DISABLED)



(p) CONDITIONAL BRANCH AND POP (DEC DISABLED)

†$\overline{CC}$ and ZERO are completed in the same clock cycle.

FIGURE 1. INSTRUCTION SET FLOWCHARTS (continued)

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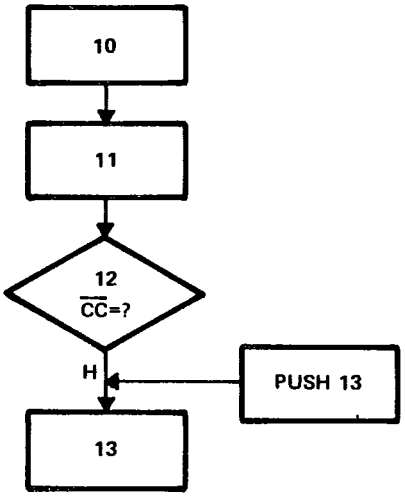
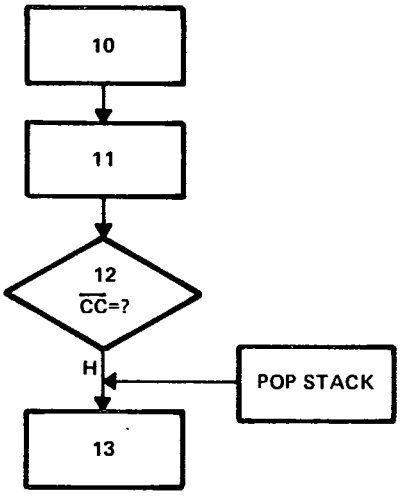
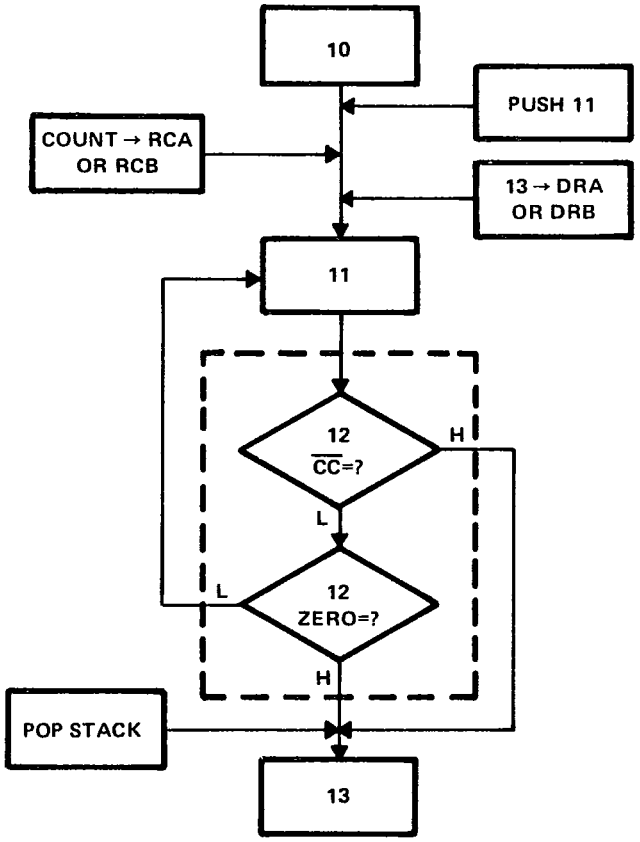


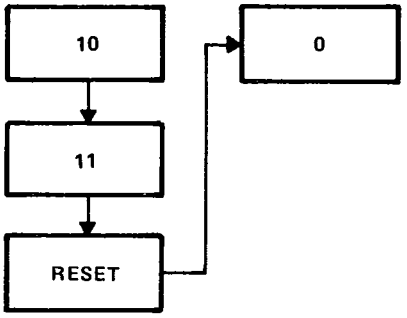
(q) PUSH AND CONTINUE ($\overline{CC}$ FORCED)



(r) POP AND CONTINUE ($\overline{CC}$ FORCED)



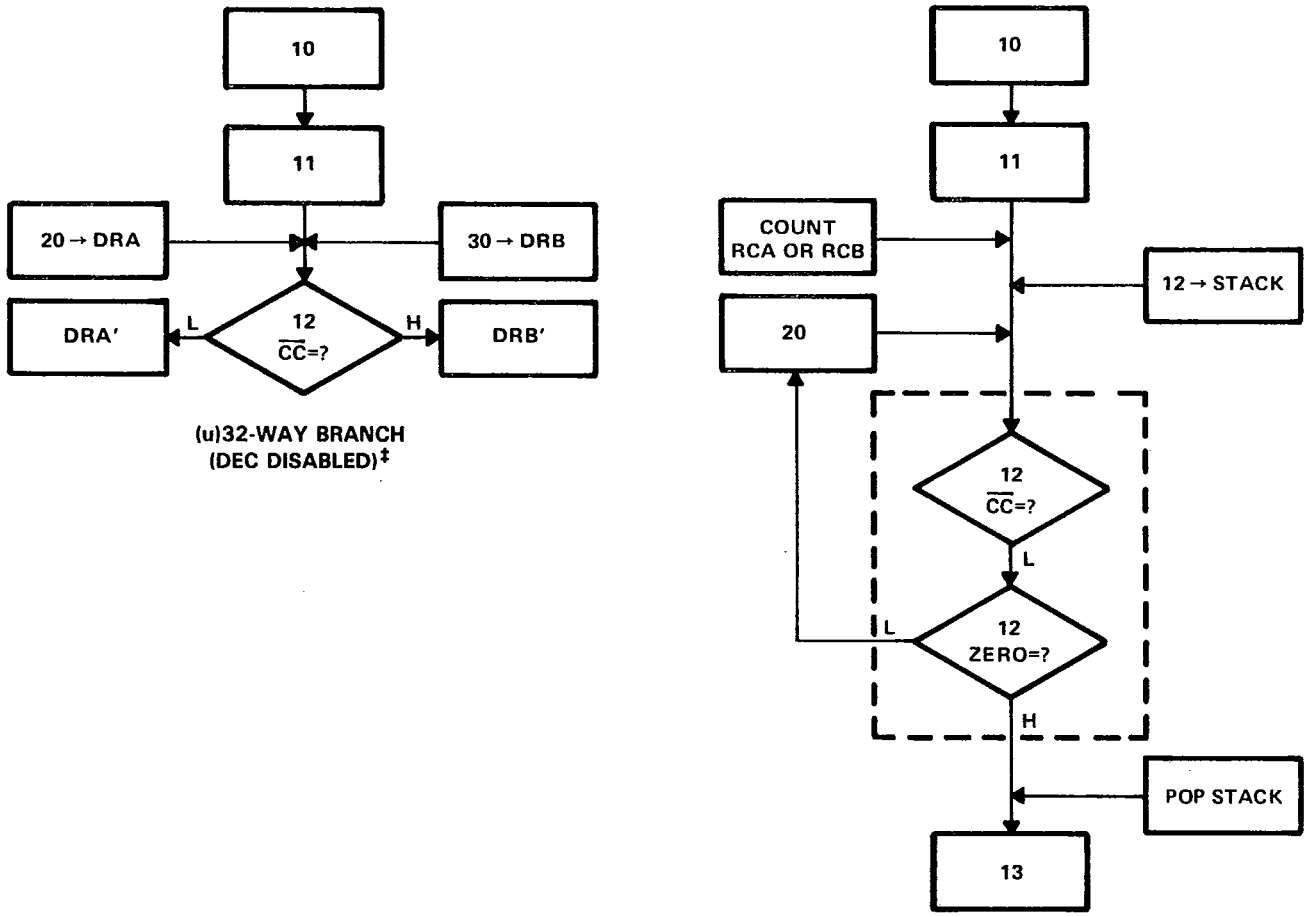
(s) EXIT FROM LOOP (DEC ENABLED)†



(t) RESET AND CLEAR

†$\overline{CC}$ and ZERO are completed in the same clock cycle.

FIGURE 1. INSTRUCTION SET FLOWCHARTS (continued)



†$\overline{CC}$ and ZERO are completed in the same clock cycle.
‡The least significant four bits, DRA and DRB, will be stripped off and four new bits appended to them from the B3-B0 port.

FIGURE 1. INSTRUCTION SET FLOWCHARTS (concluded)

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absolute maximum ratings

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: I/O ports . . . . . 5.5 V
All other inputs . . . . . 7 V
Operating case temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions (see Note 1)

PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	I/O supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−2.6	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free air temperature	0		70	°C

NOTE 1: The specified limits shown apply only after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 2.5 meters/s (500 ft/min) is maintained.

electrical characteristics over recommended conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA	2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 24 mA		0.35	0.5	V
I_I	All inputs except $\overline{RAOE}$, $\overline{RBOE}$, and $\overline{YOE}$	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
	$\overline{RAOE}$, $\overline{RBOE}$, and $\overline{YOE}$	V_{CC} = 5.5 V,	V_I = 7 V			0.2	
	I/O ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1	
I_{IH}‡	All inputs except $\overline{RAOE}$, RBOE, and $\overline{YOE}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
	I/O ports, $\overline{RAOE}$, $\overline{RBOE}$, and $\overline{YOE}$					40	
I_{IL}‡	$\overline{RAOE}$, $\overline{RBOE}$, and $\overline{YOE}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−400	μA
	All other inputs and I/O					−200	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			650	725	mA

† All typical values are for V_{CC} = 5 V and T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the output buffer off-state current.
§ The output conditions for I_O have been selected to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

maximum switching characteristics over recommended operating ranges of temperature and supply voltages (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)					UNIT
		Y	ZERO	DRA	DRB	STKWRN	
t_{pd}	$\overline{CC}$	16					ns
	CLK	15		15	11	12	
		19†	15†				
	DRA13-DRA0	14					
	DRB13-DRB0	14					
	MUX2-MUX0	15					
	RC2-RC0	19	12				
	S2-S0	18					
	B2-B0	12					
	OSEL			15			
t_{en}	$\overline{YOE}$	10					ns
	$\overline{RAOE}$			12			
	$\overline{RBOE}$				11		
t_{dis}	$\overline{YOE}$	11					ns
	$\overline{RAOE}$			6			
	$\overline{RBOE}$				6		

†Decrementing Register/Counter A or B and sensing a zero.
NOTE 2: For load circuit and voltage waveforms, see page 1-12 of *The TTL Data Book,* Volume 3, 1984.

setup and hold times

PARAMETER	FROM	TO (DESTINATION)	MIN	MAX	UNIT
t_{su} before CLK↑	$\overline{CC}$	Stack	10		ns
	DRA13-DRA0	RCA	3		
		INT RT	7		
	DRB13-DRB0	RCB	4		
		INT RT	7		
	INC	MPC	4		
	$\overline{INT}$	Stack	9		
	RC2-RC0	Stack	8		
		RCA, RCB	6		
		INT RT	6		
	S2-S0	Stack	11		
		INT RT	9		
	MUX2-MUX0	INT RT	11		
	B3-B0	INT RT	12		
	Y13-Y0	MPC	5		
t_h after CLK↑	DRA	RCA	1		ns
	DRB	RCB	1		
	Y	MPC	1		
	All other	Any Destination	0		

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minimum clock requirements (see Note 3)

PARAMETER		MIN	MAX	UNIT
t_{wL}	Pulse duration, clock low	6		ns
t_{wH}	Pulse duration, clock high	7		
t_c	Clock cycle time	20		

NOTE 3: The total clock period of clock high and clock low must not be less than clock cycle time. The minimum pulse durations specified are only for clock high or clock low, but not for both simultaneously.