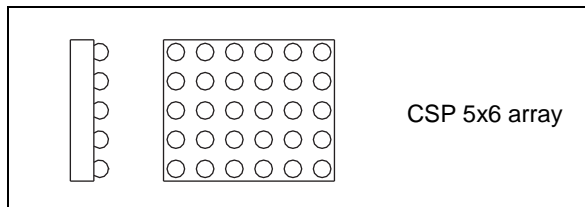


# Sound Terminal<sup>®</sup>

## 2-channel high-efficiency digital audio system

Datasheet - production data



### Features

- Wide-range supply voltage (4.5 V - 20 V)
- 2 channels of ternary PWM (stereo mode)
- 2 channels of 24-bit FFX<sup>™</sup>
- 100 dB SNR and dynamic range
- Selectable 32- to 192-kHz input sampling rates
- Digital gain -80 dB to +48 dB in 0.5 dB steps
- Software volume update
- Individual channel and master gain/attenuation
- Individual channel and master software and hardware mute
- Independent channel volume bypass
- Automatic zero-detect mute
- Automatic invalid input detect mute
- Short-circuit detection at startup (Out-Vcc, Out-Gnd, Out 1b-Out 2a)
- 2-channel I<sup>2</sup>S input data interface
- 2 Hz DC cut filter (input)
- Input channel mapping
- Automatic volume control for limiting maximum power
- 96 kHz internal processing sampling rate, 24-bit precision
- Advanced modes for AM interference frequency switching and noise suppression
- Embedded thermal-overload and short-circuit protection
- Video application: 576 \* f<sub>S</sub> input mode support

### Applications

- LCDs
- DVDs
- Cradles
- Digital speakers
- Wireless-speaker cradles

### Description

The STA333IS is an integrated circuit comprising digital audio processing, digital amplifier control and an FFX<sup>™</sup> power output stage to create a high-power, single-chip FFX solution for all-digital amplification with high quality and high efficiency.

The STA333IS power section consists of four independent half-bridge stages. Two channels can be provided by two full bridges, delivering up to 10 W + 10 W of power.

Also featured in the STA333IS are new advanced modes for reducing AM radio interference. The serial audio data input interface accepts all possible formats, including the popular I<sup>2</sup>S format. Two channels of FFX<sup>™</sup> processing are provided.

The STA333IS is part of the Sound Terminal<sup>®</sup> family that provides full digital audio streaming to the speaker, offering cost effectiveness, low-power dissipation and sound enrichment.

**Table 1. Device summary**

| Order code | Package       | Packaging     |
|------------|---------------|---------------|
| STA333IS   | CSP 5x6 array | Tape and reel |

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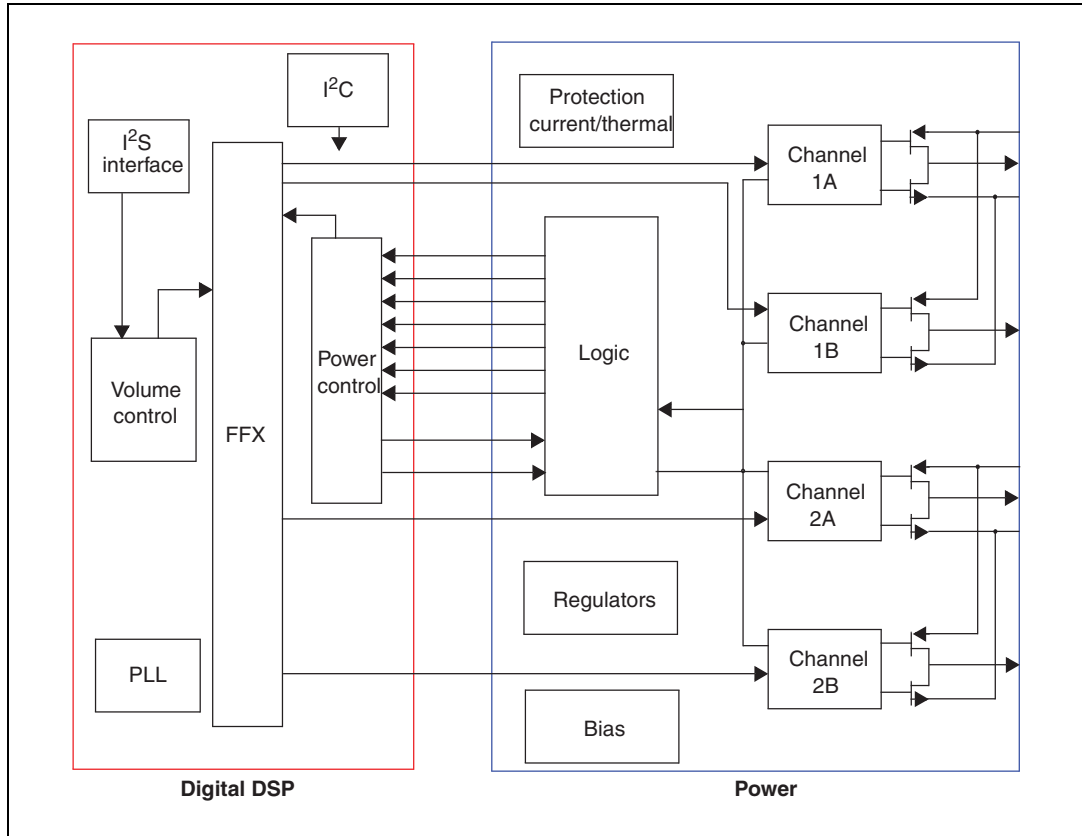
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# 1 Block diagram

Figure 1. Block diagram



## 2 Pin description

### 2.1 Pinout

Figure 2. Pin connections (package top view)

|   | 1     | 2     | 3      | 4      | 5       |
|---|-------|-------|--------|--------|---------|
| A | GND1  | OUT1  | NC     | VDDREG | SDI     |
| B | GND1  | VCC1  | NC     | LRCKI  | VDD_DIG |
| C | OUT1B | VCC1  | GNDREG | BICKI  | GND_DIG |
| D | OUT2A | VCC2  | VCCREG | SDA    | XTI     |
| E | GND2  | VCC2  | NC     | SCL    | VDD_PLL |
| F | GND2  | OUT2B | NC     | VSS    | GND_PLL |



## 2.2 Pin list

Table 2. Pin description

| Pin number                          | Name    | Description   | Pad information  |
|-------------------------------------|---------|---|--|
| <b>I/O pins</b>                     |         |   |  |
| B4                                  | LRCKI   | I <sup>2</sup> S Left/Right clock                         |  |
| C4                                  | BICKI   | I <sup>2</sup> S serial clock                             |  |
| A5                                  | SDI     | I <sup>2</sup> S serial data channels 1 & 2               |  |
| D5                                  | XTI     | Master clock input  |  |
| E4                                  | SCL     | I <sup>2</sup> C serial clock                             |  |
| D4                                  | SDA     | I <sup>2</sup> C serial data                              |  |
| <b>Power output pins</b>            |         |   |  |
| A2                                  | OUT1A   | Positive output 1   |  |
| C1                                  | OUT1B   | Negative output 1   |  |
| D1                                  | OUT2A   | Positive output 2   |  |
| F2                                  | OUT2B   | Negative output 2   |  |
| <b>Power supplies (preliminary)</b> |         |   |  |
| B2/C2                               | VCC1    | Positive supply (upper MOSFET) to left H-bridge P output  |  |
| E2/D2                               | VCC2    | Positive supply (upper MOSFET) to right H-bridge P output |  |
| A1/B1                               | GND1    | Negative supply (lower MOSFET) to left H-bridge P output  |  |
| E1/F1                               | GND2    | Negative supply (lower MOSFET) to right H-bridge P output |  |
| D3                                  | VCCREG  | Reference voltage to Vcc                                  | These pins are output pins that must be externally filtered. Do not connect these pins to external supply voltage. |
| C3                                  | GNDREG  | Reference voltage to ground                               |  |
| A4                                  | VDDREG  | Reference voltage to 3.3 V                                |  |
| F4                                  | VSS     | Reference voltage to Vcc - 3.3 V                          |  |
| B5                                  | VDD_DIG | Digital supply  |  |
| C5                                  | GND_DIG | Digital ground  |  |
| E5                                  | VDD_PLL | PLL supply  |  |
| F5                                  | GND_PLL | PLL ground  |  |
| A3, B3, E3, F3                      | NC      | Not connected   |  |

## 3 Electrical specifications

### 3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

| Symbol           | Parameter                             | Min. | Typ. | Max. | Unit |
|------------------|---------------------------------------|------|------|------|------|
| V <sub>CC</sub>  | Analog supply voltage (pins VCCx)     | -0.3 | -    | 22   | V    |
| V <sub>DD</sub>  | Digital supply voltage (pins VDD_DIG) | -0.3 | -    | 4.0  | V    |
| I <sub>L</sub>   | Logic input interface                 | -0.3 | -    | 4.0  | V    |
| T <sub>op</sub>  | Operating junction temperature        | 0    | -    | 150  | °C   |
| T <sub>stg</sub> | Storage temperature                   | -40  | -    | 150  | °C   |

**Warning:** Stresses beyond those listed in [Table 3: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Table 5: Recommended operating conditions](#) are not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. In the real application, a power supply with nominal value rated within the limits of the recommended operating conditions may rise beyond the maximum operating conditions for a short time when no or very low current is sunk (amplifier in mute state). In this case the reliability of the device is guaranteed, provided that the absolute maximum ratings are not exceeded.

### 3.2 Thermal data

Table 4. Thermal data

| Symbol               | Parameter   | Min. | Typ. | Max. | Unit |
|----------------------|---|------|------|------|------|
| R <sub>Th(j-a)</sub> | Thermal resistance junction-to-ambient <sup>(1)</sup> | -    | 45   | -    | °C/W |
| T <sub>sd</sub>      | Thermal shutdown junction temperature                 | 140  | 150  | 160  | °C   |
| T <sub>w</sub>       | Thermal warning temperature                           | -    | 130  | -    | °C   |
| T <sub>hsd</sub>     | Thermal shutdown hysteresis                           | 18   | 20   | 22   | °C   |

1. Measurements performed on ST 2-layer reference board (1 oz. PCB, 3.8 cm<sup>2</sup> exposed copper dissipation area)

### 3.3 Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol    | Parameter                        | Min. | Typ. | Max. | Unit |
|-----------|----------------------------------|------|------|------|------|
| $V_{CC}$  | Analog supply voltage (VCCx)     | 4.5  | -    | 20   | V    |
| $V_{DD}$  | Digital supply voltage (VDD_DIG) | 3.0  | 3.3  | 3.6  | V    |
| $I_L$     | Logic input interface            | 3.0  | 3.3  | 3.6  | V    |
| $T_{amb}$ | Ambient temperature              | 0    | -    | 70   | °C   |

### 3.4 Electrical specifications - digital section

Table 6. Electrical characteristics for digital section

| Symbol   | Parameter                                       | Conditions                    | Min.                   | Typ. | Max.           | Unit             |
|----------|---|-------------------------------|------------------------|------|----------------|------------------|
| $I_{il}$ | Input current, no pull-up or pull-down resistor | $V_i = 0\text{ V}$            | -                      | -    | $\pm 10$       | $\mu\text{A}$    |
| $I_{ih}$ |   | $V_i = V_{DD} = 3.6\text{ V}$ | -                      | -    | $\pm 10$       | $\mu\text{A}$    |
| $V_{il}$ | Low-level input voltage                         | -                             | -                      | -    | $0.2^* V_{DD}$ | V                |
| $V_{ih}$ | High-level input voltage                        | -                             | $0.8^* V_{DD}$         | -    | -              | V                |
| $V_{ol}$ | Low-level output voltage                        | $I_{ol} = 2\text{ mA}$        | -                      | -    | 0.3V           | V                |
| $V_{oh}$ | High-level output voltage                       | $I_{oh} = 2\text{ mA}$        | $V_{DD} - 0.3\text{V}$ | -    | -              | V                |
| $I_{pu}$ | Pull-up current                                 | -                             | 25                     | 66   | 125            | $\mu\text{A}$    |
| $R_{pu}$ | Equivalent pull-up resistance                   | -                             | -                      | 50   | -              | $\text{k}\Omega$ |

### 3.5 Electrical specifications - power section

The specifications in [Table 7](#) below are given for the conditions  $V_{CC} = 13\text{ V}$ ,  $V_{DD} = 3.3\text{ V}$ ,  $f_{SW} = 384\text{ kHz}$ ,  $T_{amb} = 25\text{ °C}$  and  $R_L = 8\ \Omega$ , unless otherwise specified.

**Table 7. Electrical specifications for power section**

| Symbol         | Parameter  | Conditions  | Min. | Typ. | Max. | Unit          |
|----------------|--|---|------|------|------|---------------|
| Po             | Output power BTL                                   | THD = 1%  | -    | 8    | -    | W             |
|                |  | THD = 10%   | -    | 10   | -    |               |
| $R_{dsON}$     | Power P-channel/N-channel MOSFET (total bridge)    | $I_d = 1\text{ A}$  | -    | 110  | -    | m $\Omega$    |
| $I_{dss}$      | Power P-channel/N-channel leakage                  | $V_{CC} = 20\text{ V}$  | -    | -    | 10   | $\mu\text{A}$ |
| gP             | Power P-channel $R_{dsON}$ matching                | $I_d = 1\text{ A}$  | 95   | -    | -    | %             |
| gN             | Power N-channel $R_{dsON}$ matching                | $I_d = 1\text{ A}$  | 95   | -    | -    | %             |
| $I_{LDT}$      | Low-current dead time (static)                     | Resistive load, refer to <a href="#">Figure 4</a>                                       | -    | 5    | 10   | ns            |
| $I_{HDT}$      | High-current dead time (dynamic)                   | Refer to <a href="#">Figure 5</a>   | -    | 10   | 20   | ns            |
| $t_r$          | Rise time  | Resistive load, refer to <a href="#">Figure 4</a>                                       | -    | 8    | 10   | ns            |
| $t_f$          | Fall time  | Resistive load, refer to <a href="#">Figure 4</a>                                       | -    | 8    | 10   | ns            |
| $V_{CC}$       | Supply voltage                                     | -   | 4.5  | -    | 20   | V             |
| $I_{VCC}$      | Supply current from $V_{CC}$ in power-down         | At power-ON (EAPD bit = 0)  | 30   | 60   | 200  | $\mu\text{A}$ |
|                | Supply current from $V_{CC}$ in operation          | PCM input signal = -60 dBfs<br>Internal clock = 49.152 MHz                              | -    | 30   | 50   | mA            |
| $I_{VDD\_DIG}$ | Supply current for FFX processing (reference only) | Switching frequency = 384 kHz<br>No LC filters  | -    | 30   | 50   | mA            |
|                | Supply current in standby                          | (PWDN bit = 0)  | -    | 11   | 25   | mA            |
| $I_{LIM}$      | Overcurrent limit                                  | Non-linear output <sup>(1)</sup>  | 2.2  | 3.5  | 4.3  | A             |
| $I_{SCP}$      | Short-circuit protection                           | High-impedance output <sup>(2)</sup>  | 2.7  | 3.8  | 5.0  | A             |
| $V_{UVP}$      | Undervoltage protection threshold                  | -   | -    | 3.5  | 4.3  | V             |
| $t_{min}$      | Output minimum pulse width                         | No load   | 20   | 30   | 60   | ns            |
| THD+N          | Total harmonic distortion and noise                | FFX stereo mode, $P_o = 1\text{ W}$ , $f = 1\text{ kHz}$                                | -    | 0.05 | -    | %             |
| DR             | Dynamic range                                      | -   | -    | 100  | -    | dB            |
| SNR            | Signal to noise ratio in ternary mode              | A-weighted  | -    | 100  | -    | dB            |
|                | Signal to noise ratio in binary mode               | A-weighted  | -    | 90   | -    |               |
| PSRR           | Power supply rejection ratio                       | FFX stereo mode, < 5 kHz,<br>$V_{RIPPLE} = 1\text{ V RMS}$<br>audio input = dither only | -    | 80   | -    | dB            |

**Table 7. Electrical specifications for power section (continued)**

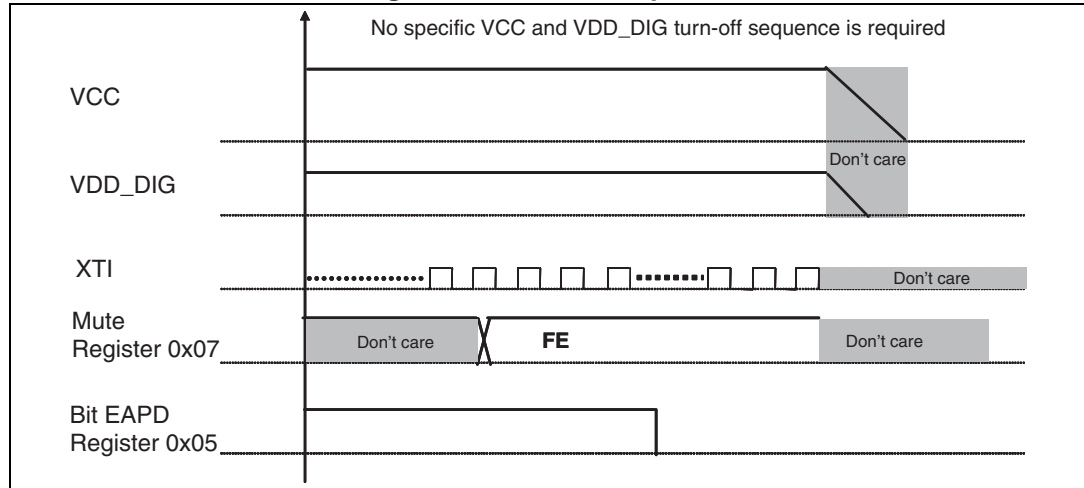
| Symbol            | Parameter                   | Conditions   | Min. | Typ. | Max. | Unit |
|-------------------|-----------------------------|--|------|------|------|------|
| X <sub>TALK</sub> | Crosstalk                   | FFX stereo mode, < 5 kHz,<br>One channel driven at 1 W<br>the other channel measured | -    | 80   | -    | dB   |
| $\eta$            | Peak efficiency in FFX mode | Po = 2 x 10 W into 8 $\Omega$  | -    | 90   | -    | %    |

1. The I<sub>LIM</sub> data is for 1 channel of BTL configuration, thus, 2 \* I<sub>LIM</sub> drives the 2-channel BTL configuration. The current limit is active when OCRB = 0 (see [Table 23: Overcurrent warning detect adjustment bypass on page 26](#)). When OCRB = 1, then I<sub>SC</sub> applies.
2. The I<sub>SCP</sub> current limit data is for 1 channel of BTL configuration, thus, 2 \* I<sub>SCP</sub> drives the 2-channel BTL configuration. The short-circuit current is applicable when OCRB = 1 (see [Table 23: Overcurrent warning detect adjustment bypass on page 26](#)).

### 3.6 Power-off sequence

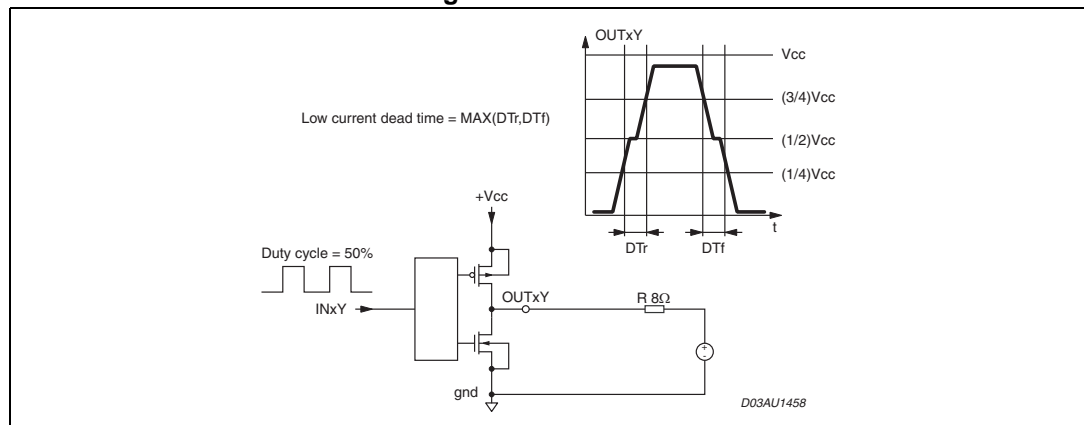
The power-off sequence shown in *Figure 3* below ensures a pop-free turn-off.

**Figure 3. Power-off sequence**

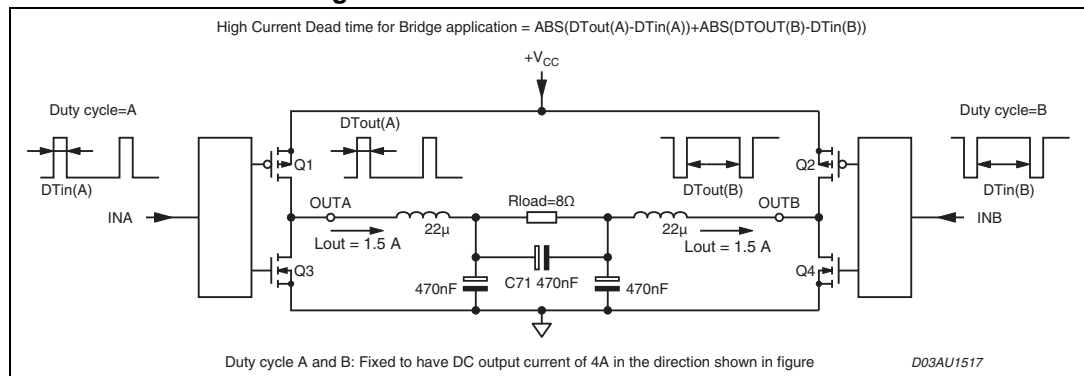


### 3.7 Testing

**Figure 4. Test circuit**



**Figure 5. Current deadtime test circuit**



### 3.8 Serial audio interface description

#### 3.8.1 Serial audio interface protocols

The STA333IS serial audio input was designed to interface with standard digital audio components and to accept serial data formats. The STA333IS always acts as a slave when receiving audio input from standard digital audio components. Serial data for two channels is provided using 3 input pins: left/right clock LRCKI (pin B4), serial clock BICKI (pin C4), and serial data SDI (pin A5).

The available formats are shown in [Figure 6](#) and [Figure 7](#), and set through [Configuration register B \(addr 0x01\)](#) on page 22.

Figure 6. I<sup>2</sup>S

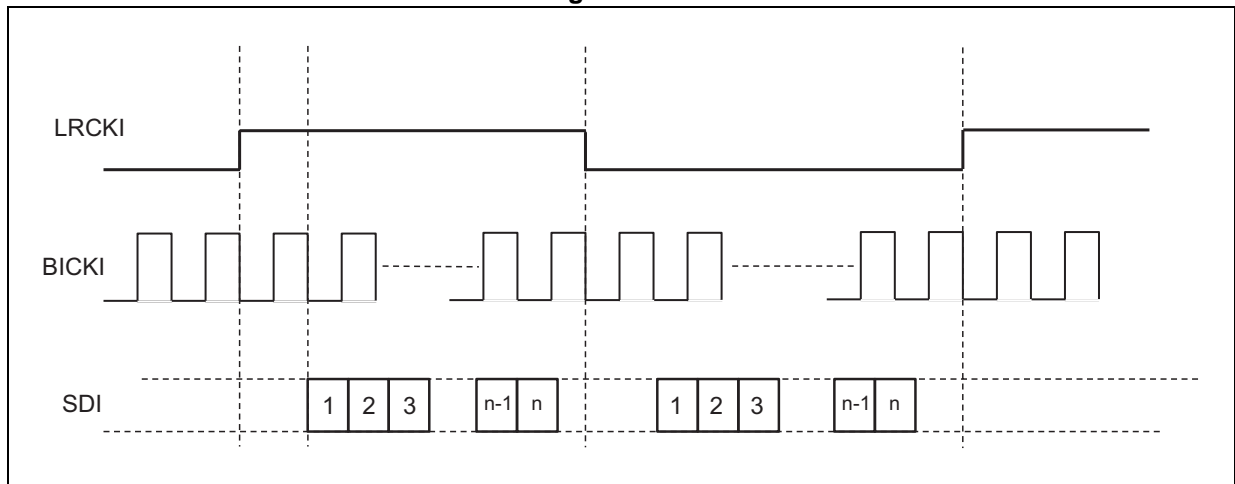
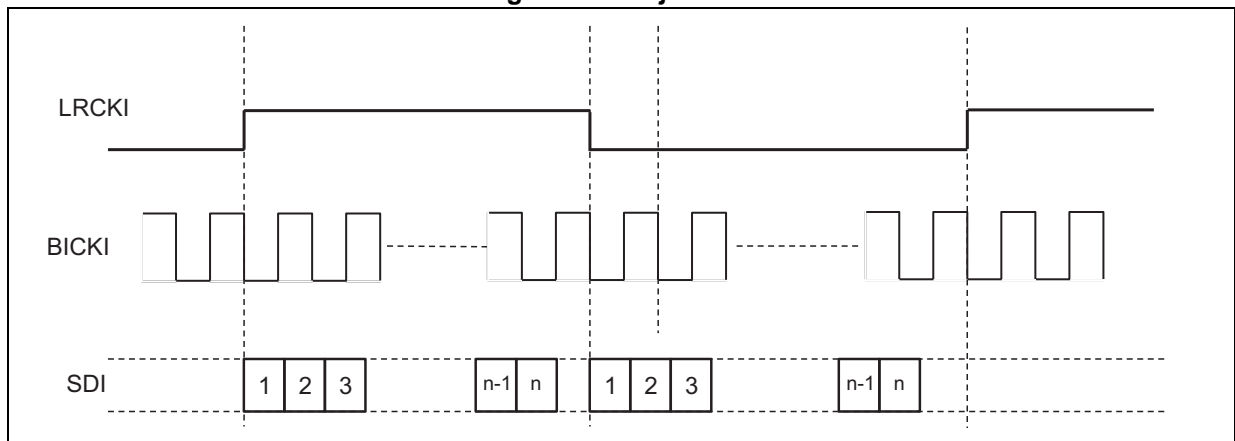


Figure 7. Left-justified



## 4 I<sup>2</sup>C bus specification

The STA333IS supports the I<sup>2</sup>C protocol via the input ports SCL and SDA. This protocol defines any device that sends data to the bus as a transmitter and any device that reads the data as a receiver. The device that controls the data transfer is known as the master and the other as the slave. The master always starts the transfer and provides the serial clock for synchronization. The STA333IS is always a slave device in all of its communications. It supports up to 400 kb/s (fast-mode bit rate).

### 4.1 Communication protocol

#### 4.1.1 Data transition or change

Data changes on the SDA line must only occur when the SCL clock is low. An SDA transition while the clock is high is used to identify a START or STOP condition.

#### 4.1.2 Start condition

START is identified by a high-to-low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A START condition must precede any command for data transfer.

#### 4.1.3 Stop condition

STOP is identified by a low-to-high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A STOP condition terminates communication between the STA333IS and the bus master.

#### 4.1.4 Data input

During data input the STA333IS samples the SDA signal on the rising edge of clock SCL. For correct device operation the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

### 4.2 Device addressing

To start communication between the master and the STA333IS, the master must initiate a start condition. Following this, the master sends to the SDA line 8 bits (MSB first) corresponding to the device select address and read or write mode.

The 7 most significant bits are the device address identifiers, corresponding to the I<sup>2</sup>C bus definition. In the STA333IS the I<sup>2</sup>C interface has device address 0x38.

The 8<sup>th</sup> bit (LSB) identifies the read or write operation RW, this bit is set to 1 for read mode and 0 for write mode. After a START condition the STA333IS identifies the device address on the SDA bus and if a match is found, acknowledges the identification during the 9<sup>th</sup> bit time. The byte following the device identification byte is the internal space address.



### 4.3 Write operation

Following the START condition the master sends a device select code with the RW bit set to 0. The STA333IS acknowledges this and then waits for the byte of internal address. After receiving the internal byte address, the STA333IS again responds with an acknowledgement.

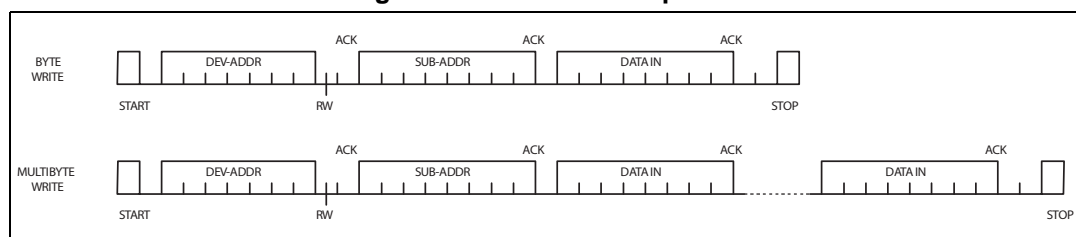
#### 4.3.1 Byte write

In the byte write mode the master sends one data byte which is acknowledged by the STA333IS. The master then terminates the transfer by generating a STOP condition.

#### 4.3.2 Multi-byte write

The multi-byte write modes can start from any internal address. The master generating a STOP condition terminates the transfer.

Figure 8. Write-mode sequence



### 4.4 Read operation

#### 4.4.1 Current address byte read

Following the START condition the master sends a device select code with the RW bit set to 1. The STA333IS acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

#### 4.4.2 Current address multi-byte read

The multi-byte read modes can start from any internal address. Sequential data bytes are read from sequential addresses within the STA333IS. The master acknowledges each data byte read and then generates a STOP condition, terminating the transfer.

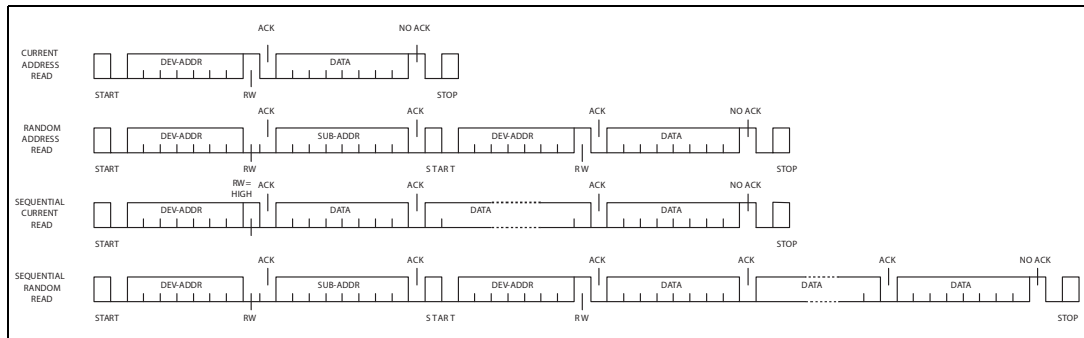
#### 4.4.3 Random address byte read

Following the START condition the master sends a device select code with the RW bit set to 0. The STA333IS acknowledges this and then the master writes the internal address byte. After receiving the internal byte address, the STA333IS again responds with an acknowledgement. The master then initiates another START condition and sends the device select code with the RW bit set to 1. The STA333IS acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a STOP condition.

### 4.4.4 Random address multi-byte read

The multi-byte read modes can start from any internal address. Sequential data bytes are read from sequential addresses within the STA333IS. The master acknowledges each data byte read and then generates a STOP condition to terminate the transfer.

Figure 9. Read-mode sequence



# 5 Register description

**Table 8. Register summary**

| Addr | Name     | D7       | D6       | D5       | D4       | D3       | D2       | D1        | D0       |
|------|----------|----------|----------|----------|----------|----------|----------|-----------|----------|
| 0x00 | CONFA    | FDRB     | TWAB     | TWRB     | IR1      | IR0      | MCS2     | MCS1      | MCS0     |
| 0x01 | CONFB    | C2IM     | C1IM     | Reserved | SAIFB    | SAI3     | SAI2     | SAI1      | SAI0     |
| 0x02 | CONFC    | OCRB     | Reserved | CSZ3     | CSZ2     | CSZ1     | CSZ0     | OM1       | OM0      |
| 0x03 | CONFD    | Reserved | ZDE      | Reserved |          |          |          |           |          |
| 0x04 | CONF E   | SVE      | ZCE      | DCCV     | PWMS     | AME      | NSBW     | MPC       | MPCV     |
| 0x05 | CONFF    | EAPD     | PWDN     | ECL E    | LDTE     | BCLE     | IDE      | Reserved  |          |
| 0x06 | MUTE     | Reserved |          |          |          |          | C2M      | C1M       | MMUTE    |
| 0x07 | MVOL     | MV7      | MV6      | MV5      | MV4      | MV3      | MV2      | MV1       | MV0      |
| 0x08 | C1VOL    | C1V7     | C1V6     | C1V5     | C1V4     | C1V3     | C1V2     | C1V1      | C1V0     |
| 0x09 | C2VOL    | C2V7     | C2V6     | C2V5     | C2V4     | C2V3     | C2V2     | C2V1      | C2V0     |
| 0x0C | AUTO     | Reserved |          |          |          | AMAM2    | AMAM1    | AMAM0     | AMAME    |
| 0x0E | C1CFG    | Reserved |          |          |          |          | C1VBP    | Reserved  |          |
| 0x0F | C2CFG    | Reserved |          |          |          |          | C2VBP    | Reserved  |          |
| 0x27 | MPCC1    | MPCC15   | MPCC14   | MPCC13   | MPCC12   | MPCC11   | MPCC10   | MPCC9     | MPCC8    |
| 0x28 | MPCC2    | MPCC7    | MPCC6    | MPCC5    | MPCC4    | MPCC3    | MPCC2    | MPCC1     | MPCC0    |
| 0x29 | DCC1     | DCC15    | DCC14    | DCC13    | DCC12    | DCC11    | DCC10    | DCC9      | DCC8     |
| 0x2A | DCC2     | DCC7     | DCC6     | DCC5     | DCC4     | DCC3     | DCC2     | DCC1      | DCC0     |
| 0x2B | FDRC1    | FDRC15   | FDRC14   | FDRC13   | FDRC12   | FDRC11   | FDRC10   | FDRC9     | FDRC8    |
| 0x2C | FDRC2    | FDRC7    | FDRC6    | FDRC5    | FDRC4    | FDRC3    | FDRC2    | FDRC1     | FDRC0    |
| 0x2D | STATUS   | PLLUL    | FAULT    | UVFAULT  | OVFAULT  | OCFAULT  | OCWARN   | TFault    | TWARN    |
| 0x2E | BIST1    | Reserved |          | RO1BACT  | R5BACT   |          |          |           | R1BACT   |
| 0x2F | BIST2    | Reserved |          | R01BEND  | R5BEND   |          |          |           | R1BEND   |
| 0x30 | BIST3    | Reserved |          |          | R5BBAD   |          |          |           | R1BBAD   |
| 0x31 | TSTCTL   | Reserved |          |          |          |          |          |           |          |
| 0x32 | C1PS     | C1PS7    | C1PS6    | C1PS5    | C1PS4    | C1PS3    | C1PS2    | C1PS1     | C1PS0    |
| 0x33 | C2PS     | C2PS7    | C2PS6    | C2PS5    | C2PS4    | C2PS3    | C2PS2    | C2PS1     | C2PS0    |
| 0x34 | OLIM     | OLIM7    | OLIM6    | OLIM5    | OLIM4    | OLIM3    | OLIM2    | OLIM1     | OLIM0    |
| 0x35 | SHEN     | Reserved |          |          |          |          |          | ENABLE_SH | Reserved |
| 0x36 | Reserved |          |          |          |          |          |          |           |          |
| 0x37 | SHORT    | SHGND1A  | SHGND1B  | SHGND2A  | SHGND2B  | SHVCC1A  | SHVCC1B  | SHVCC2A   | SHVCC2B  |
| 0x38 | SHOUT    | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved  | SHOUT    |

## 5.1 Configuration registers (addr 0x00 to 0x05)

### 5.1.1 Configuration register A (addr 0x00)

|      |      |      |     |     |      |      |      |
|------|------|------|-----|-----|------|------|------|
| D7   | D6   | D5   | D4  | D3  | D2   | D1   | D0   |
| FDRB | TWAB | TWRB | IR1 | IR0 | MCS2 | MCS1 | MCS0 |
| 0    | 1    | 1    | 0   | 0   | 0    | 1    | 1    |

#### Master clock select

Table 9. Master clock select

| Bit | R/W | RST | Name | Description   |
|-----|-----|-----|------|---|
| 0   | R/W | 1   | MCS0 | Master clock select: Selects the ratio between the input I <sup>2</sup> S sampling frequency and the input clock. |
| 1   | R/W | 1   | MCS1 |   |
| 2   | R/W | 0   | MCS2 |   |

The STA333IS supports sampling rates of 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz. Therefore the internal clock is:

- 32.768 MHz for 32 kHz
- 45.1584 MHz for 44.1 kHz, 88.2 kHz, and 176.4 kHz
- 49.152 MHz for 48 kHz, 96 kHz, and 192 kHz

The external clock frequency provided to the XTI pin must be a multiple of the input sampling frequency ( $f_S$ ).

The relationship between the input clock and the input sampling rate is determined by both the MCSx and the IR (input rate) register bits. The MCSx bits determine the PLL factor generating the internal clock and the IR bit determines the oversampling ratio used internally.

Table 10. MCS bits

| Input sampling rate<br>$f_S$ (kHz) | IR | MCS[2:0]    |             |             |             |             |             |
|------------------------------------|----|-------------|-------------|-------------|-------------|-------------|-------------|
|                                    |    | 101         | 100         | 011         | 010         | 001         | 000         |
| 32, 44.1, 48                       | 00 | $576 * f_S$ | $128 * f_S$ | $256 * f_S$ | $384 * f_S$ | $512 * f_S$ | $768 * f_S$ |
| 88.2, 96                           | 01 | NA          | $64 * f_S$  | $128 * f_S$ | $192 * f_S$ | $256 * f_S$ | $384 * f_S$ |
| 176.4, 192                         | 1X | NA          | $32 * f_S$  | $64 * f_S$  | $96 * f_S$  | $128 * f_S$ | $192 * f_S$ |

**Interpolation ratio select**

**Table 11. Interpolation ratio select**

| Bit | R/W | RST | Name     | Description  |
|-----|-----|-----|----------|--|
| 4:3 | R/W | 00  | IR [1:0] | Interpolation ratio select: Selects internal interpolation ratio based on input I <sup>2</sup> S sampling frequency. |

The STA333IS has variable interpolation (oversampling) settings such that internal processing and FFX output rates remain consistent. The first processing block interpolates by either 2 times or 1 time (pass-through) or provides a 2-time downsampling. The oversampling ratio of this interpolation is determined by the IR bits.

**Table 12. IR bit settings as a function of input sampling rate**

| Input sampling rate $f_s$ (kHz) | IR | 1 <sup>st</sup> stage interpolation ratio |
|---------------------------------|----|---|
| 32                              | 00 | 2-time oversampling                       |
| 44.1                            | 00 | 2-time oversampling                       |
| 48                              | 00 | 2-time oversampling                       |
| 88.2                            | 01 | Pass-through                              |
| 96                              | 01 | Pass-through                              |
| 176.2                           | 10 | 2-time downsampling                       |
| 192                             | 10 | 2-time downsampling                       |

**Thermal warning recovery bypass**

**Table 13. Thermal warning recovery**

| Bit | R/W | RST | Name | Description   |
|-----|-----|-----|------|---|
| 5   | R/W | 1   | TWRB | Thermal warning recovery bypass:<br>0: thermal warning recovery enabled<br>1: thermal warning recovery disabled |

If the thermal warning adjustment is enabled (TWAB = 0), then the thermal warning recovery determines if the -3 dB output limit is removed when thermal warning is negative.

If TWRB = 0 and TWAB = 0, then when a thermal warning disappears, the -3 dB output limit is removed and the gain is added back to the system. If TWRB = 1 and TWAB = 0, then when a thermal warning disappears, the -3 dB output limit remains until TWRB is changed to zero or the device is reset.

### Thermal warning adjustment bypass

**Table 14. Thermal warning adjustment**

| Bit | R/W | RST | Name | Description   |
|-----|-----|-----|------|---|
| 6   | R/W | 1   | TWAB | Thermal warning adjustment bypass:<br>0: thermal warning adjustment enabled<br>1: thermal warning adjustment disabled |

The on-chip STA333IS power output block provides feedback to the digital controller using inputs to the power control block. The TWARN input is used to indicate a thermal warning condition. When TWARN is asserted (set to 0) for a period of time greater than 400 ms, the power control block will force a -3 dB output limit (determined by TWOCL in coefficient RAM) to the modulation limit in an attempt to eliminate the thermal warning condition. Once the thermal warning output limit adjustment is applied, it remains in this state until reset unless FDRB = 0.

### Fault-detect recovery bypass

**Table 15. Fault-detect recovery**

| Bit | R/W | RST | Name | Description  |
|-----|-----|-----|------|--|
| 7   | R/W | 0   | FDRB | Fault-detect recovery bypass:<br>0: fault-detect recovery enabled<br>1: fault-detect recovery disabled |

The on-chip STA333IS power output block provides feedback to the digital controller using inputs to the power control block. The FAULT input is used to indicate a fault condition (either overcurrent or thermal). When FAULT is asserted (set to 0), the power control block attempts a recovery from the fault by asserting the 3-state output (setting it to 0 which directs the power output block to begin recovery), holding it at 0 for period of time in the range of 0.1 ms to 1 second as defined by the fault-detect recovery constant register (FDRC registers 0x2B, 0x2C), then toggling it back to 1. This sequence is repeated as long as the fault indication exists. This feature is enabled by default but can be bypassed by setting the FDRB control bit to 1.

### 5.1.2 Configuration register B (addr 0x01)

| D7   | D6   | D5       | D4    | D3   | D2   | D1   | D0   |
|------|------|----------|-------|------|------|------|------|
| C2IM | C1IM | Reserved | SAIFB | SAI3 | SAI2 | SAI1 | SAI0 |
| 1    | 0    | 0        | 0     | 0    | 0    | 0    | 0    |

**Serial audio input interface format**

**Table 16. Serial audio input interface format**

| Bit | R/W | RST | Name | Description  |
|-----|-----|-----|------|--|
| 0   | R/W | 0   | SAI0 | Determines the interface format of the input serial digital audio interface. |
| 1   | R/W | 0   | SAI1 |  |
| 2   | R/W | 0   | SAI2 |  |
| 3   | R/W | 0   | SAI3 |  |

**Serial data interface**

The STA333IS audio serial input interfaces with standard digital audio components and accepts a number of serial data formats. The STA333IS always acts as a slave when receiving audio input from standard digital audio components. Serial data for two channels is provided using three inputs: left/right clock LRCKI, serial clock BICKI, and serial data SDI.

Bits SAIx and bit SAIFB are used to specify the serial data format. The default serial data format is I<sup>2</sup>S, MSB first. Available formats are shown in the tables that follow.

**Serial data first bit**

**Table 17. Serial data first bit**

| SAIFB | Format    |
|-------|-----------|
| 0     | MSB-first |
| 1     | LSB-first |

**Table 18. Support serial audio input formats for MSB-first (SAIFB = 0)**

| BICKI               | SAI [3:0] | SAIFB | Interface format                    |
|---------------------|-----------|-------|-------------------------------------|
| 32 * f <sub>S</sub> | 0000      | 0     | I <sup>2</sup> S 15-bit data        |
|                     | 0001      | 0     | Left/right justified 16-bit data    |
| 48* f <sub>S</sub>  | 0000      | 0     | I <sup>2</sup> S 16- to 23-bit data |
|                     | 0001      | 0     | Left-justified 16- to 24-bit data   |
|                     | 0010      | 0     | Right-justified 24-bit data         |
|                     | 0110      | 0     | Right-justified 20-bit data         |
|                     | 1010      | 0     | Right-justified 18-bit data         |
| 64* f <sub>S</sub>  | 1110      | 0     | Right-justified 16-bit data         |
|                     | 0000      | 0     | I <sup>2</sup> S 16- to 24-bit data |
|                     | 0001      | 0     | Left-justified 16- to 24-bit data   |
|                     | 0010      | 0     | Right-justified 24-bit data         |
|                     | 0110      | 0     | Right-justified 20-bit data         |
|                     | 1010      | 0     | Right-justified 18-bit data         |
|                     | 1110      | 0     | Right-justified 16-bit data         |

Table 19. Supported serial audio input formats for LSB-first (SAIFB = 1)

| BICKI              | SAI[3:0] | SAIFB                       | Interface format                       |
|--------------------|----------|-----------------------------|--|
| 32* f <sub>S</sub> | 1100     | 1                           | I <sup>2</sup> S 15-bit data           |
|                    | 1110     | 1                           | Left/right justified 16-bit data       |
| 48* f <sub>S</sub> | 0100     | 1                           | I <sup>2</sup> S 20-bit data           |
|                    | 1000     | 1                           | I <sup>2</sup> S 18-bit data           |
|                    | 1100     | 1                           | LSB-first I <sup>2</sup> S 16-bit data |
|                    | 0001     | 1                           | Left-justified 24-bit data             |
|                    | 0101     | 1                           | Left-justified 20-bit data             |
|                    | 1001     | 1                           | Left-justified 18-bit data             |
|                    | 1101     | 1                           | Left-justified 16-bit data             |
| 48* f <sub>S</sub> | 0010     | 1                           | Right-justified 24-bit data            |
|                    | 0110     | 1                           | Right-justified 20-bit data            |
|                    | 1010     | 1                           | Right-justified 18-bit data            |
| 64* f <sub>S</sub> | 1110     | 1                           | Right-justified 16-bit data            |
|                    | 0000     | 1                           | I <sup>2</sup> S 24-bit data           |
|                    | 0100     | 1                           | I <sup>2</sup> S 20-bit data           |
|                    | 1000     | 1                           | I <sup>2</sup> S 18-bit data           |
|                    | 1100     | 1                           | LSB-first I <sup>2</sup> S 16-bit data |
|                    | 0001     | 1                           | Left-justified 24-bit data             |
|                    | 0101     | 1                           | Left-justified 20-bit data             |
|                    | 1001     | 1                           | Left-justified 18-bit data             |
|                    | 1101     | 1                           | Left-justified 16-bit data             |
|                    | 0010     | 1                           | Right-justified 24-bit data            |
|                    | 0110     | 1                           | Right-justified 20-bit data            |
|                    | 1010     | 1                           | Right-justified 18-bit data            |
| 1110               | 1        | Right-justified 16-bit data |  |



**Channel input mapping**

**Table 20. Channel input mapping**

| Bit | R/W | RST | Name | Description   |
|-----|-----|-----|------|---|
| 6   | R/W | 0   | C1IM | 0: processing channel 1 receives left I <sup>2</sup> S input<br>1: processing channel 1 receives right I <sup>2</sup> S input |
| 7   | R/W | 0   | C2IM | 0: processing channel 2 receives left I <sup>2</sup> S input<br>1: processing channel 2 receives right I <sup>2</sup> S input |

Each channel received via I<sup>2</sup>S can be mapped to any internal processing channel via the channel input mapping registers. This allows for flexibility in processing. The default settings of these registers map each I<sup>2</sup>S input channel to its corresponding processing channel.

**5.1.3 Configuration register C (addr 0x02)**

| D7   | D6       | D5   | D4   | D3   | D2   | D1  | D0  |
|------|----------|------|------|------|------|-----|-----|
| OCRB | Reserved | CSZ3 | CSZ2 | CSZ1 | CSZ0 | OM1 | OM0 |
| 1    | 0        | 0    | 1    | 0    | 1    | 1   | 1   |

**FFX power output mode**

**Table 21. FFX power output mode**

| Bit | R/W | RST | Name | Description   |
|-----|-----|-----|------|---|
| 0   | R/W | 1   | OM0  | The FFX power output mode selects the configuration of the FFX output:<br>00: drop compensation<br>01: discrete output stage: tapered compensation<br>10: full-power mode<br>11: variable drop compensation (CSZx bits) |
| 1   | R/W | 1   | OM1  |   |

**FFX compensation pulse size register**

**Table 22. FFX compensating pulse size**

| Bit | R/W | RST | Name | Description   |
|-----|-----|-----|------|---|
| 2   | R/W | 1   | CSZ0 | When OM[1:0] = 11, this register determines the size of the FFX compensating pulse from 0 to 15 clock periods:<br>0000: 0 ns (0 ticks) compensating pulse size<br>0001: 20 ns (1 tick) clock period compensating pulse size<br>1111: 300 ns (15 ticks) clock period compensating pulse size |
| 3   | R/W | 0   | CSZ1 |   |
| 4   | R/W | 1   | CSZ2 |   |
| 5   | R/W | 0   | CSZ3 |   |
|     |     |     |      |   |

**Overcurrent warning detect adjustment bypass**

**Table 23. Overcurrent warning detect adjustment bypass**

| Bit | R/W | RST | Name | Description   |
|-----|-----|-----|------|---|
| 7   | R/W | 1   | OCRB | 0: overcurrent warning adjustment enabled<br>1: overcurrent warning adjustment disabled |

The status bit OCWARN is used to warn of an overcurrent condition. When OCWARN is asserted (set to 0), the power control block forces an adjustment to the modulation limit (default -3 dB) in an attempt to eliminate the overcurrent warning condition. Once the overcurrent warning volume adjustment is applied, it remains applied until the device is reset. The overcurrent limit can be changed via register OLIM (*Output limit register (addr 0x34) on page 35*).

**5.1.4 Configuration register D (addr 0x03)**

| D7       | D6  | D5       | D4 | D3 | D2 | D1 | D0 |
|----------|-----|----------|----|----|----|----|----|
| Reserved | ZDE | Reserved |    |    |    |    |    |
| 0        | 1   | 0        | 0  | 0  | 0  | 0  | 0  |

**Zero-detect mute enable**

**Table 24. Zero-detect mute enable**

| Bit | R/W | RST | Name | Description                              |
|-----|-----|-----|------|--|
| 6   | R/W | 1   | ZDE  | 1: enable the automatic zero-detect mute |

Setting the ZDE bit enables the zero-detect automatic mute. The zero-detect circuit looks at the data for each processing channel at the output of the crossover (bass management) filter. If any channel receives 2048 consecutive zero-value samples (regardless of  $f_s$ ) then that individual channel is muted if this function is enabled.

**5.1.5 Configuration register E (addr 0x04)**

| D7  | D6  | D5   | D4   | D3  | D2   | D1  | D0   |
|-----|-----|------|------|-----|------|-----|------|
| SVE | ZCE | DCCV | PWMS | AME | NSBW | MPC | MPCV |
| 1   | 1   | 0    | 0    | 0   | 0    | 1   | 0    |

**Max power correction variable**

**Table 25. Max power correction variable**

| Bit | R/W | RST | Name | Description   |
|-----|-----|-----|------|---|
| 0   | R/W | 0   | MPCV | 0: use standard MPC coefficient<br>1: use MPCC bits for MPC coefficient |

**Max power correction**

**Table 26. Max power correction**

| Bit | R/W | RST | Name | Description  |
|-----|-----|-----|------|--|
| 1   | R/W | 1   | MPC  | 1: enable power bridge correction for THD reduction near maximum power output. |

Setting the MPC bit turns on special processing that corrects the STA333IS power device at high power. This mode lowers the THD+N of a full FFX system at maximum power output and slightly below. If enabled, MPC is operational in all output modes except tapered (OM[1:0] = 01) and binary. When OCFG = 00, MPC does not affect channels 3 and 4, the line-out channels.

**Noise-shaper bandwidth selection**

**Table 27. Noise-shaper bandwidth selection**

| Bit | R/W | RST | Name | Description  |
|-----|-----|-----|------|--|
| 2   | R/W | 0   | NSBW | 1: 3 <sup>rd</sup> order NS<br>0: 4 <sup>th</sup> order NS |

**AM mode enable**

**Table 28. AM mode enable**

| Bit | R/W | RST | Name | Description   |
|-----|-----|-----|------|---|
| 3   | R/W | 0   | AME  | 0: normal FFX operation<br>1: AM reduction mode FFX operation |

The STA333IS features an FFX processing mode that minimizes the amount of noise generated in the frequency range of AM radio. This mode is intended for use when FFX is operating in a device with an active AM tuner. The SNR of the FFX processing is reduced to approximately 83 dB in this mode, which is still greater than the SNR of AM radio.

**PWM speed mode**

**Table 29. PWM speed mode**

| Bit | R/W | RST | Name | Description   |
|-----|-----|-----|------|---|
| 4   | R/W | 0   | PWMS | 0: normal speed (384 kHz) all channels<br>1: odd speed (341.3 kHz) all channels |

**Distortion compensation variable enable**

**Table 30. Distortion compensation variable enable**

| Bit | R/W | RST | Name | Description  |
|-----|-----|-----|------|--|
| 5   | R/W | 0   | DCCV | 0: uses preset DC coefficient<br>1: uses DCC coefficient |

**Zero-crossing volume enable****Table 31. Zero-crossing volume enable**

| Bit | R/W | RST | Name | Description   |
|-----|-----|-----|------|---|
| 6   | R/W | 1   | ZCE  | 1: volume adjustments will only occur at digital zero-crossings<br>0: volume adjustments will occur immediately |

The ZCE bit enables zero-crossing volume adjustments. When the volume is adjusted on digital zero-crossings, no clicks will be audible.

**Soft volume update enable****Table 32. Zero-crossing volume enable**

| Bit | R/W | RST | Name | Description  |
|-----|-----|-----|------|--|
| 7   | R/W | 1   | SVE  | 1: volume adjustments ramp according to SVR settings<br>0: volume adjustments will occur immediately |

**5.1.6 Configuration register F (addr 0x05)**

| D7   | D6   | D5   | D4   | D3   | D2  | D1       | D0 |
|------|------|------|------|------|-----|----------|----|
| EAPD | PWDN | ECLE | LDTE | BCLE | IDE | Reserved |    |
| 0    | 1    | 0    | 1    | 1    | 1   | 0        | 0  |

**Invalid input detect mute enable****Table 33. Invalid input detect mute enable**

| Bit | R/W | RST | Name | Description  |
|-----|-----|-----|------|--|
| 2   | R/W | 1   | IDE  | 1: enables the automatic invalid input detect mute |

Setting the IDE bit enables this function, which looks at the input I<sup>2</sup>S data and will automatically mute if the signals are perceived as invalid.

**Binary output mode clock loss detection****Table 34. Binary output mode clock loss detection**

| Bit | R/W | RST | Name | Description                                    |
|-----|-----|-----|------|--|
| 3   | R/W | 1   | BCLE | Binary output mode clock loss detection enable |

The BCLE bit detects loss of input MCLK in binary mode and outputs 50% of the duty cycle.

**LRCK double trigger protection**

**Table 35. LRCK double trigger protection**

| Bit | R/W | RST | Name | Description                            |
|-----|-----|-----|------|--|
| 4   | R/W | 1   | LDTE | LRCLK double trigger protection enable |

The LDTE bit actively prevents double triggering of LRCLK.

**Auto EAPD on clock loss**

**Table 36. Auto EAPD on clock loss**

| Bit | R/W | RST | Name | Description             |
|-----|-----|-----|------|-------------------------|
| 5   | R/W | 0   | ECLE | Auto EAPD on clock loss |

When active, the ECLE bit will issue a device power-down signal (EAPD) on clock loss detection.

**IC power-down**

**Table 37. Power-down**

| Bit | R/W | RST | Name | Description   |
|-----|-----|-----|------|---|
| 6   | R/W | 1   | PWDN | 0: power-down, low-power condition<br>1: normal operation |

The PWDN register is used to put the IC in a low-power state. When PWDN is 0, the output begins a soft-mute. After the mute condition is reached, EAPD is asserted to power down the power stage, then the master clock to all internal hardware except the I<sup>2</sup>C block is gated. This puts the IC in a very low power consumption state.

**External amplifier power down**

**Table 38. External amplifier power-down**

| Bit | R/W | RST | Name | Description  |
|-----|-----|-----|------|--|
| 7   | R/W | 1   | EAPD | 0: external power stage power-down active<br>1: normal operation |

The EAPD register directly disables/enables the internal power circuitry.

When EAPD = 0, the internal power section is placed in a low-power state (disabled).

## 5.2 Volume control registers (addr 0x06 to 0x09)

### 5.2.1 Mute/line output configuration register (addr 0x06)

|          |    |    |    |    |     |     |       |
|----------|----|----|----|----|-----|-----|-------|
| D7       | D6 | D5 | D4 | D3 | D2  | D1  | D0    |
| Reserved |    |    |    |    | C2M | C1M | MMUTE |
| 0        | 0  | 0  | 0  | 0  | 0   | 0   | 0     |

#### Master mute

Table 39. Master mute

| Bit | R/W | RST | Name  | Description  |
|-----|-----|-----|-------|--|
| 0   | R/W | 0   | MMUTE | 0: normal operation<br>1: all channels are in mute condition |

#### Channel mute

Table 40. Channel mute

| Bit | R/W | RST | Name | Description  |
|-----|-----|-----|------|--|
| 1   | R/W | 0   | C1M  | Channel 1 mute:<br>0: not muted, it is possible to set the channel volume<br>1: hardware muted |
| 2   | R/W | 0   | C2M  | Channel 2 mute:<br>0: not muted, it is possible to set the channel volume<br>1: hardware muted |

### 5.2.2 Master volume register (addr 0x07)

|     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|
| D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |
| MV7 | MV6 | MV5 | MV4 | MV3 | MV2 | MV1 | MV0 |
| 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |

### 5.2.3 Channel volume (addr 0x08, 0x09)

|      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|
| D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
| C1V7 | C1V6 | C1V5 | C1V4 | C1V3 | C1V2 | C1V1 | C1V0 |
| 0    | 1    | 1    | 0    | 0    | 0    | 0    | 0    |

|      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|
| D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
| C2V7 | C2V6 | C2V5 | C2V4 | C2V3 | C2V2 | C2V1 | C2V0 |
| 0    | 1    | 1    | 0    | 0    | 0    | 0    | 0    |

#### Volume setting

The volume structure of the STA333IS consists of individual volume registers for each channel and a master volume register that provides an offset to each channel’s volume setting. The individual channel volumes are adjustable in 0.5-dB steps from +48 dB to -80 dB. As an example, if C3V = 0x00 or +48 dB and MV = 0x18 or -12 dB, then the total gain for channel 3 = +36 dB.

The master mute, when set to 1, will mute all channels at once, whereas the individual channel mutes (CxM) mute only that channel. Both the master mute and the channel mutes provide a “soft mute” with the volume ramping down to mute in 4096 samples from the maximum volume setting at the internal processing rate (about 96 kHz). A hard mute can be obtained by commanding a value of all 1’s (255) to any channel volume register or the master volume register. When volume offsets are provided via the master volume register, any channel whose total volume is less than -80 dB is muted.

All changes in volume take place at zero-crossings when ZCE = 1 (configuration register F) on a per-channel basis as this creates the smoothest possible volume transitions. When ZCE = 0, volume updates will occur immediately.

**Table 41. Master volume offset as a function of MV**

| MV[7:0]         | Volume offset from channel value |
|-----------------|----------------------------------|
| 00000000 (0x00) | 0 dB                             |
| 00000001 (0x01) | -0.5 dB                          |
| 00000010 (0x02) | -1 dB                            |
| ...             | ...                              |
| 01001100 (0x4C) | -38 dB                           |
| ...             | ...                              |
| 11111110 (0xFE) | -127.5 dB                        |
| 11111111 (0xFF) | Hard master mute                 |

**Table 42. Channel volume as a function of CxV**

| CxV[7:0]        | Volume            |
|-----------------|-------------------|
| 00000000 (0x00) | +48 dB            |
| 00000001 (0x01) | +47.5 dB          |
| 00000010 (0x02) | +47 dB            |
| ...             | ...               |
| 01011111 (0x5F) | +0.5 dB           |
| 01100000 (0x60) | 0 dB              |
| 01100001 (0x61) | -0.5 dB           |
| ...             | ...               |
| 11010111 (0xD7) | -59.5 dB          |
| 11011000 (0xD8) | -60 dB            |
| 11011001 (0xD9) | -61 dB            |
| 11011010 (0xDA) | -62 dB            |
| ...             | ...               |
| 11101100 (0xEC) | -80 dB            |
| 11101101 (0xED) | Hard channel mute |
| ...             | ...               |
| 11111111 (0xFF) | Hard channel mute |

### 5.3 Automodes™ register (0x0C)

| D7       | D6 | D5 | D4 | D3    | D2    | D1    | D0    |
|----------|----|----|----|-------|-------|-------|-------|
| Reserved |    |    |    | AMAM2 | AMAM1 | AMAM0 | AMAME |
| 0        | 0  | 0  | 0  | 0     | 0     | 0     | 0     |

#### AM interference frequency switching

**Table 43. AM interference frequency switching**

| Bit | R/W | RST | Name  | Description  |
|-----|-----|-----|-------|--|
| 0   | R/W | 0   | AMAME | 0: switching frequency determined by PWMS setting<br>1: switching frequency determined by AMAM setting |

#### AMAM bits

**Table 44. Automodes™ AM switching frequency selection**

| AMAM[2:0] | 48 kHz / 96 kHz input f <sub>S</sub> | 44.1 kHz / 88.2 kHz input f <sub>S</sub> |
|-----------|--------------------------------------|--|
| 000       | 0.535 MHz - 0.720 MHz                | 0.535 MHz - 0.670 MHz                    |
| 001       | 0.721 MHz - 0.900 MHz                | 0.671 MHz - 0.800 MHz                    |
| 010       | 0.901 MHz - 1.100 MHz                | 0.801 MHz - 1.000 MHz                    |
| 011       | 1.101 MHz - 1.300 MHz                | 1.001 MHz - 1.180 MHz                    |
| 100       | 1.301 MHz - 1.480 MHz                | 1.181 MHz - 1.340 MHz                    |
| 101       | 1.481 MHz - 1.600 MHz                | 1.341 MHz - 1.500 MHz                    |
| 110       | 1.601 MHz - 1.700 MHz                | 1.501 MHz - 1.700 MHz                    |



### 5.4 Channel configuration registers (addr 0x0E, 0x0F)

|          |    |    |    |    |       |          |    |
|----------|----|----|----|----|-------|----------|----|
| D7       | D6 | D5 | D4 | D3 | D2    | D1       | D0 |
| Reserved |    |    |    |    | C1VBP | Reserved |    |
| 0        | 0  | 0  | 0  | 0  | 0     | 0        | 0  |

|          |    |    |    |    |       |          |    |
|----------|----|----|----|----|-------|----------|----|
| D7       | D6 | D5 | D4 | D3 | D2    | D1       | D0 |
| Reserved |    |    |    |    | C2VBP | Reserved |    |
| 0        | 0  | 0  | 0  | 0  | 0     | 0        | 0  |

#### Volume bypass

Each channel contains an individual channel volume bypass. If a particular channel has volume bypassed via the CxVBP = 1 register, then only the channel volume setting for that particular channel affects the volume setting, the master volume setting will not affect that channel.

### 5.5 Variable max power correction registers (addr 0x27, 0x28)

The MPCC bits determine the 16 MSBs of the MPC compensation coefficient. This coefficient is used in place of the default coefficient when MPCV = 1.

|        |        |        |        |        |        |       |       |
|--------|--------|--------|--------|--------|--------|-------|-------|
| D7     | D6     | D5     | D4     | D3     | D2     | D1    | D0    |
| MPCC15 | MPCC14 | MPCC13 | MPCC12 | MPCC11 | MPCC10 | MPCC9 | MPCC8 |
| 0      | 0      | 0      | 1      | 1      | 0      | 1     | 0     |

|       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|
| D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
| MPCC7 | MPCC6 | MPCC5 | MPCC4 | MPCC3 | MPCC2 | MPCC1 | MPCC0 |
| 1     | 1     | 0     | 0     | 0     | 0     | 0     | 0     |

### 5.6 Variable distortion compensation registers (addr 0x29, 0x2A)

|       |       |       |       |       |       |      |      |
|-------|-------|-------|-------|-------|-------|------|------|
| D7    | D6    | D5    | D4    | D3    | D2    | D1   | D0   |
| DCC15 | DCC14 | DCC13 | DCC12 | DCC11 | DCC10 | DCC9 | DCC8 |
| 1     | 1     | 1     | 1     | 0     | 0     | 1    | 1    |

|      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|
| D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
| DCC7 | DCC6 | DCC5 | DCC4 | DCC3 | DCC2 | DCC1 | DCC0 |
| 0    | 0    | 1    | 1    | 0    | 0    | 1    | 1    |

The DCC bits determine the 16 MSBs of the distortion compensation coefficient. This coefficient is used in place of the default coefficient when DCCV = 1.

### 5.7 Fault-detect recovery constant registers (addr 0x2B, 0x2C)

|       |       |       |       |       |       |      |      |
|-------|-------|-------|-------|-------|-------|------|------|
| D7    | D6    | D5    | D4    | D3    | D2    | D1   | D0   |
| FDC15 | FDC14 | FDC13 | FDC12 | FDC11 | FDC10 | FDC9 | FDC8 |
| 0     | 0     | 0     | 0     | 0     | 0     | 0    | 0    |

|      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|
| D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   |
| FDC7 | FDC6 | FDC5 | FDC4 | FDC3 | FDC2 | FDC1 | FDC0 |
| 0    | 0    | 0    | 0    | 1    | 1    | 0    | 0    |

The FDC bits specify the 16-bit fault-detect recovery time delay. When status register bit FAULT is asserted, the tristate output is immediately asserted low and held low for the time period specified by this constant. A value of 0x0001 in this register is approximately 0.083 ms. The default value of 0x000C gives approximately 0.1 ms.

*Note:* 0x0000 is a reserved value for this register pair. This value must not be used.

### 5.8 Device status register (addr 0x2D)

|       |       |         |         |         |        |        |       |
|-------|-------|---------|---------|---------|--------|--------|-------|
| D7    | D6    | D5      | D4      | D3      | D2     | D1     | D0    |
| PLLUL | FAULT | UVFAULT | OVFAULT | OCFAULT | OCWARN | TFAULT | TWARN |

This read-only register provides the fault, warning and PLL status from the power control block.

**Table 45. Status bits description**

| Bit | R/W | RST | Name    | Description  |
|-----|-----|-----|---------|--|
| 0   | RO  | -   | TWARN   | Thermal warning:<br>0: junction temperature is close to the fault condition<br>1: normal operation |
| 1   | RO  | -   | TFAULT  | Thermal fault:<br>0: junction temperature limit detection<br>1: normal operation                   |
| 2   | RO  | -   | OCWARN  | Overcurrent warning:<br>0: warning<br>1: normal operation  |
| 3   | RO  | -   | OCFAULT | Overcurrent fault:<br>0: fault detected<br>1: normal operation                                     |
| 4   | -   | -   | -       | Reserved   |
| 5   | RO  | -   | UVFAULT | Undervoltage warning:<br>0: VCCx below lower voltage threshold<br>1: normal operation              |
| 6   | RO  | -   | FAULT   | Power bridge fault:<br>0: fault detected<br>1: normal operation                                    |
| 7   | RO  | -   | PLLUL   | PLL lock:<br>0: locked<br>1: not locked  |

## 5.9 Reserved registers (addr 0x2E, 0x2F, 0x30, 0x31)

These registers are not to be used.

## 5.10 Postscale registers (addr 0x32, 0x33)

| D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|-------|-------|-------|-------|-------|-------|-------|-------|
| C1PS7 | C1PS6 | C1PS5 | C1PS4 | C1PS3 | C1PS2 | C1PS1 | C1PS0 |
| 0     | 1     | 1     | 1     | 1     | 1     | 1     | 1     |

| D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|-------|-------|-------|-------|-------|-------|-------|-------|
| C2PS7 | C2PS6 | C2PS5 | C2PS4 | C2PS3 | C2PS2 | C2PS1 | C2PS0 |
| 0     | 1     | 1     | 1     | 1     | 1     | 1     | 1     |

### Postscale

The STA333IS provides one additional multiplication after the last interpolation stage and the distortion compensation on each channel, which can be used to limit the maximum modulation index and therefore the peak current through the power device. The register values represent an 8-bit signed fractional number. This number is extended to a 24-bit number, by adding zeros to the right, and then directly multiplied by the data on that channel. An independent postscale is provided for each channel but all channels can use channel 1 postscale factor by setting the postscale link bit. By default, all postscale factors are set to 0x7F (pass-through).

## 5.11 Output limit register (addr 0x34)

### 5.11.1 Thermal and overcurrent warning output limit register

| D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|-------|-------|-------|-------|-------|-------|-------|-------|
| OLIM7 | OLIM6 | OLIM5 | OLIM4 | OLIM3 | OLIM2 | OLIM1 | OLIM0 |
| 0     | 1     | 0     | 1     | 1     | 0     | 1     | 0     |

The STA333IS provides a simple mechanism for reacting to a thermal or overcurrent warning in the power device. When the TWARN or OCWARN status bit is asserted, the output is limited to the OLIM setting. The limit can be adjusted by modifying the thermal warning/overcurrent output limit value. As for the normal postscale, the register value represents an 8-bit signed fractional number. This number is extended to a 24-bit number, by adding zeros to the right, and then directly multiplied by the data on both channels. The scaling value range is from 0x80 = -1 to 0x7F = 0.992. To avoid phase changes in the output signal only the positive range is used (0x00 to 0x7F). The default setting of 0x5A provides a -3-dB limit.

If the cause of the limiting is a thermal warning, the output limiting is removed when the thermal warning situation disappears. If the cause of the limiting is an overcurrent warning, output limiting remains in effect until the device is reset.

Table 46. Output limit values for thermal and overcurrent warnings

| OLIM[7:0] | Attenuation (dB) |
|-----------|------------------|
| 0x7F      | 0.06             |
| 0x7E      | 0.13             |
| ....      | ....             |
| 0x5A      | 3.0              |
| ....      | ....             |
| 0x40      | 6.0              |
| ....      | ....             |
| 0x28      | 10               |
| ....      | ....             |
| 0x01      | 42               |
| 0x00      | Inf              |

### 5.12 Short-circuit protection registers SHOKx (addr 0x35, 0x37, 0x38)

| D7       | D6       | D5       | D4       | D3       | D2       | D1          | D0       |
|----------|----------|----------|----------|----------|----------|-------------|----------|
| reserved | reserved | reserved | reserved | reserved | reserved | ENABLE_SH   | reserved |
| 0        | 0        | 0        | 0        | 0        | 0        | 0 (default) | 1        |

| D7      | D6      | D5      | D4      | D3      | D2      | D1      | D0      |
|---------|---------|---------|---------|---------|---------|---------|---------|
| SHGND1A | SHGND1B | SHGND2A | SHGND2B | SHVCC1A | SHVCC1B | SHVCC2A | SHVCC2B |
| 1       | 1       | 1       | 1       | 1       | 1       | 1       | 1       |

| D7       | D6       | D5       | D4       | D3       | D2       | D1       | D0    |
|----------|----------|----------|----------|----------|----------|----------|-------|
| reserved | reserved | reserved | reserved | reserved | reserved | reserved | SHOUT |
| 0        | 0        | 0        | 0        | 0        | 1        | 0        | 1     |

The following power bridge pin short-circuit protections are implemented in the STA333IS:

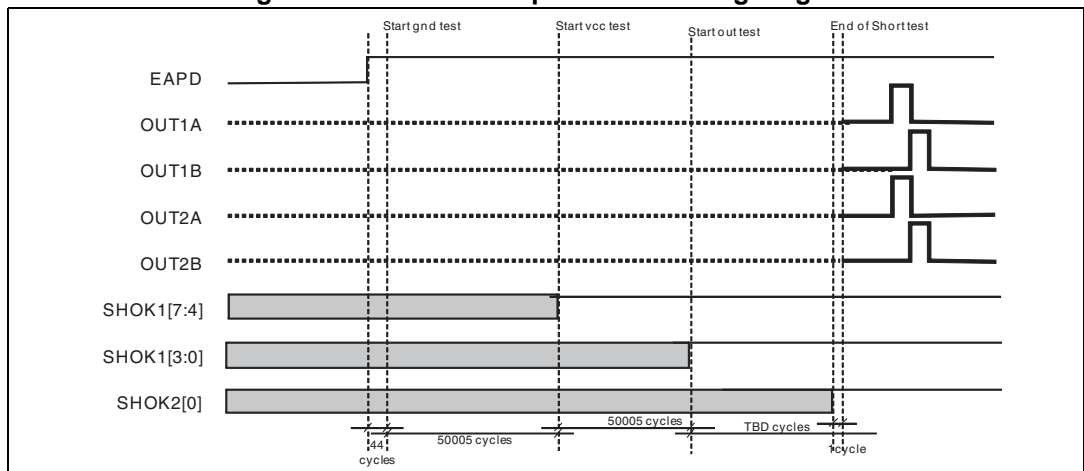
- OUTxx vs GNDx
- OUTxx vs VCCx
- OUT1B vs OUT2A

The protection is enabled when reg. 0x35 bit 1 (ENABLE\_SH) is set to '1'. The protection will check the short-circuit when the EAPD bit is toggled from '0' to '1' (i.e. the power bridge is switched on), and only if the test passes (no short) does the power bridge leave the tristate condition.

Register 0x37 and 0x38 (read-only registers) give more information about the detected short type. SHGNDxx equal to '0' means that OUTxx is shorted to ground, while the same value on SHVCCxx means that OUTxx is shorted to Vcc, and finally SHOUT='0' means that OUT1B is shorted to OUT2A. To be noted that once the check is performed and the tristate released, the short protection is no longer active until the next EAPD 0->1 toggling, which means that shorts that occurred during normal operation cannot be detected. To be noted that registers 0x37 and 0x38 are meaningful only after the EAPD bit is set to '1' at least once.

The short-circuit protections implemented are effective only in BTL configuration, and they must not be activated if a single-ended application scheme is needed.

**Figure 10. Short-circuit protection timing diagram**



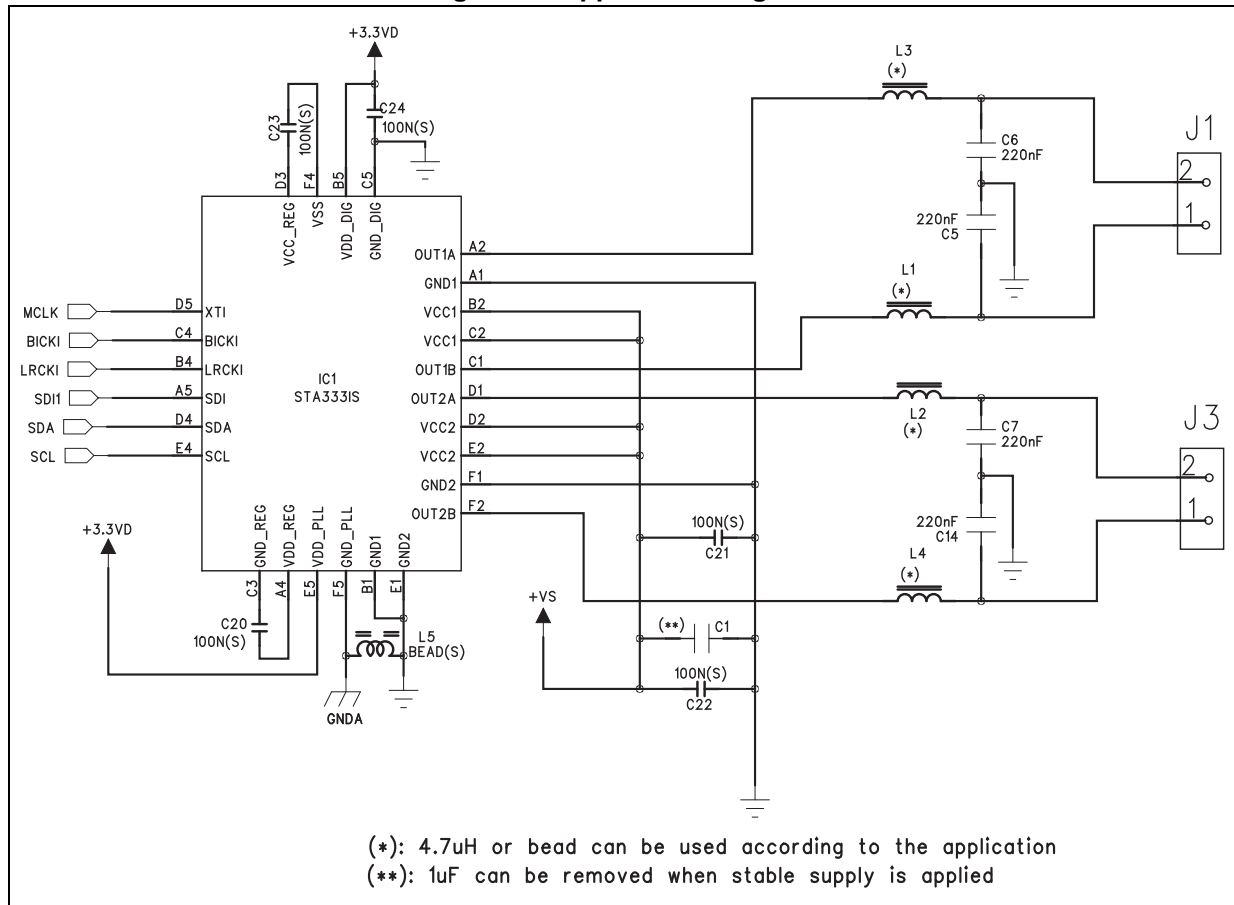
## 6 Application information

### 6.1 Application scheme for power supplies

Figure 11 below shows a typical application scheme for the STA333IS.

Special care has to be taken with regard to the power supplies when laying out the PCB. All decoupling capacitors should be placed as close as possible to the device in order to limit the effect of spikes on the supplies.

Figure 11. Application diagram



## 7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

The STA333IS comes in a CSP 5x6 array package.

### Soldering information

Figure 12. Recommended soldering reflow profile for mounting on PCB

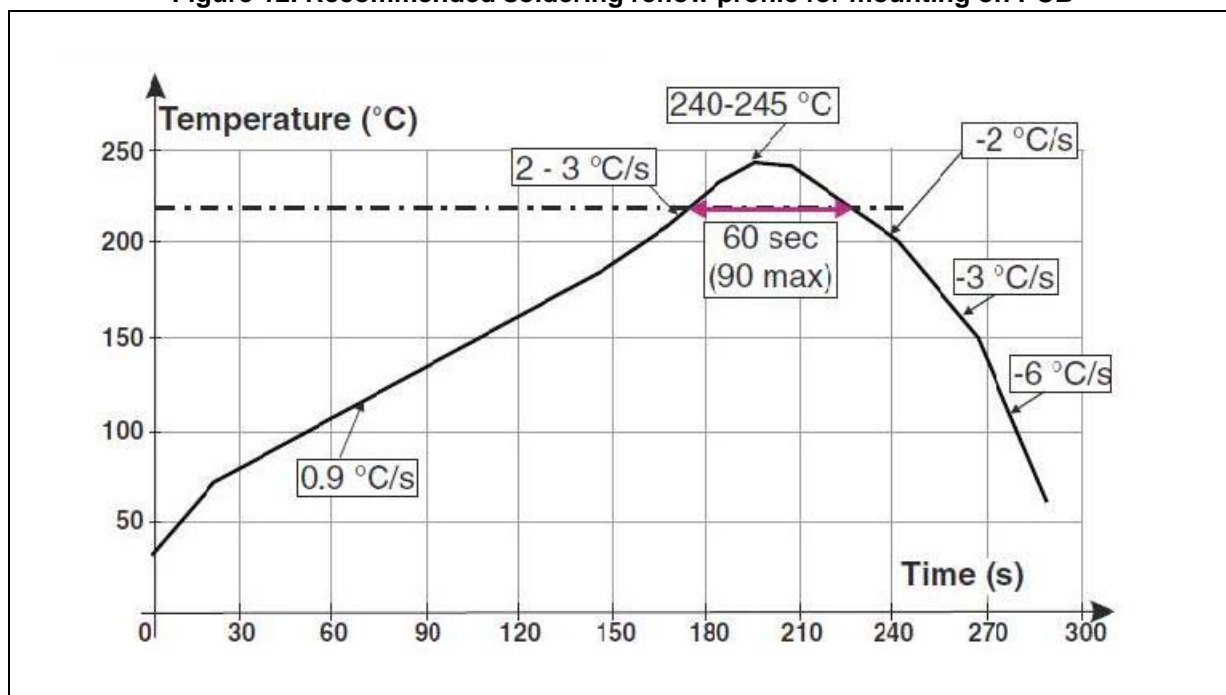
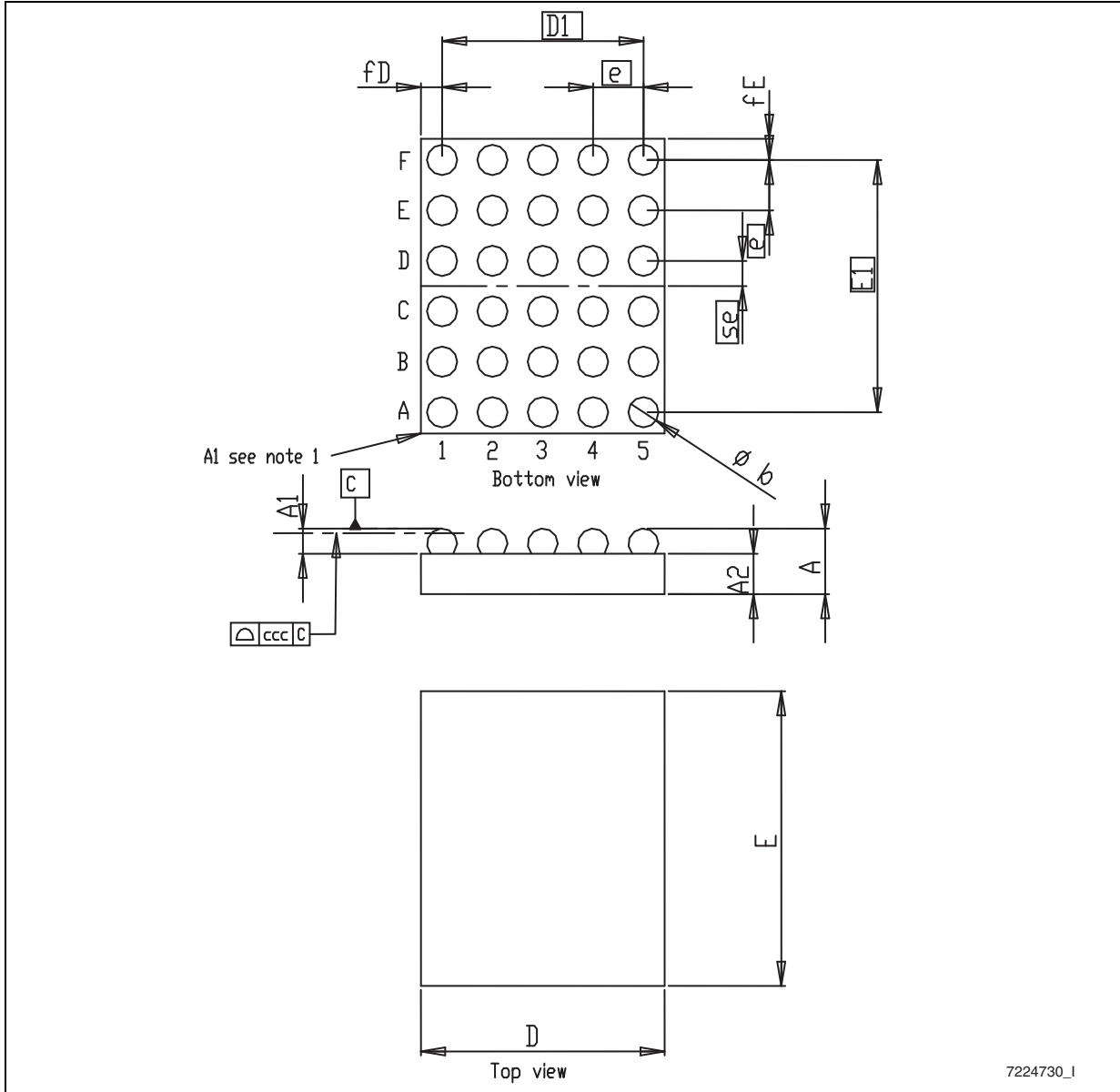


Table 47. Recommended soldering reflow values for mounting on PCB

| Profile                                     | Typ.         | Max.   |
|---|--------------|--------|
| Temp. gradient in preheat (T = 70 - 180 °C) | 0.9 °C/s     | 3 °C/s |
| Temp. gradient (T = 200 - 225 °C)           | 2 °C/s       | 3 °C/s |
| Peak temp. in reflow                        | 240 - 245 °C | 260 °C |
| Time above 220 °C                           | 60 s         | 90 s   |
| Temp. gradient in cooling                   | -2 to -3 °C  | -6 °C  |
| Time from 50 to 220 °C                      | 160 to 220 s |        |

Figure 13 below shows the package outline and Table 48 gives the dimensions.

Figure 13. CSP 5x6 array outline drawing



7224730\_1

Note 1: The terminal A1 on the backside of the product is identified by a distinguishing feature (for instance by a circular "clear area", typically 0.5 mm diameter).



Table 48. CSP 5x6 array package dimensions

| Symbol | mm    |       |       |
|--------|-------|-------|-------|
|        | Min   | Typ   | Max   |
| A      | 0.585 | 0.65  | 0.715 |
| A1     | 0.210 | 0.25  | 0.29  |
| A2     | 0.38  | 0.4   | 0.42  |
| b      | 0.265 | 0.315 | 0.365 |
| D      | 2.52  | 2.57  | 2.62  |
| D1     |       | 2     |       |
| E      | 3.19  | 3.24  | 3.29  |
| E1     |       | 2.5   |       |
| e      | 0.45  | 0.5   | 0.55  |
| se     | 0.2   | 0.25  | 0.3   |
| fD     | 0.277 | 0.285 | 0.293 |
| fE     | 0.362 | 0.370 | 0.378 |
| ccc    |       |       | 0.08  |

## 8 Revision history

**Table 49. Document revision history**

| Date        | Revision | Changes   |
|-------------|----------|---|
| 16-Jan-2013 | 1        | Initial release.  |
| 11-Mar-2013 | 2        | Document status promoted to "production data"<br>Updated Description on page 1<br>Updated Table 1: Device summary on page 1<br>Updated VCC (max) in Table 3: Absolute maximum ratings<br>Updated RTh(j-case) in Table 4: Thermal data<br>Updated Vol and Voh in Table 6: Electrical characteristics for digital section<br>Updated Table 7: Electrical specifications for power section<br>Updated Figure 6: I2S<br>Updated Figure 7: Left-justified<br>Updated Section 4.2: Device addressing<br>Updated Table 19: Supported serial audio input formats for LSB-first (SAIFB = 1)<br>Updated Figure 11 |
| 02-Apr-2013 | 3        | Textual update in Table 4: Thermal data<br>Added Figure 12: Recommended soldering reflow profile for mounting on PCB<br>Added Table 47: Recommended soldering reflow values for mounting on PCB   |
| 07-Mar-2019 | 4        | Updated <a href="#">Section 6.1: Application scheme for power supplies</a>  |

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