

IRS2053MPbF
 3 CH Digital Audio Amplifier

Features

- 3 channel integrated analog input Class D audio amplifier drivers
- Versatile protection control enabling latched, non-latched, or host controlled shutdown function
- DC offset detection input
- Clipping detection
- Thermal sensor inputs
- Fault output
- Programmable over current protection
- Programmable dead-time generation
- Startup click noise reduction
- Under voltage protection
- High noise immunity
- RoHS compliant

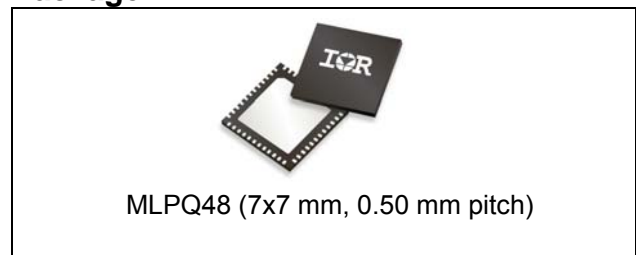
Note

The IRS2053M digital audio driver is a three channel Class D audio driver housed in a 48 pin MLPQ. The IRS2053M features clipping detection outputs, DC offset detection input, over temperature sensor inputs and a fault reporting output.

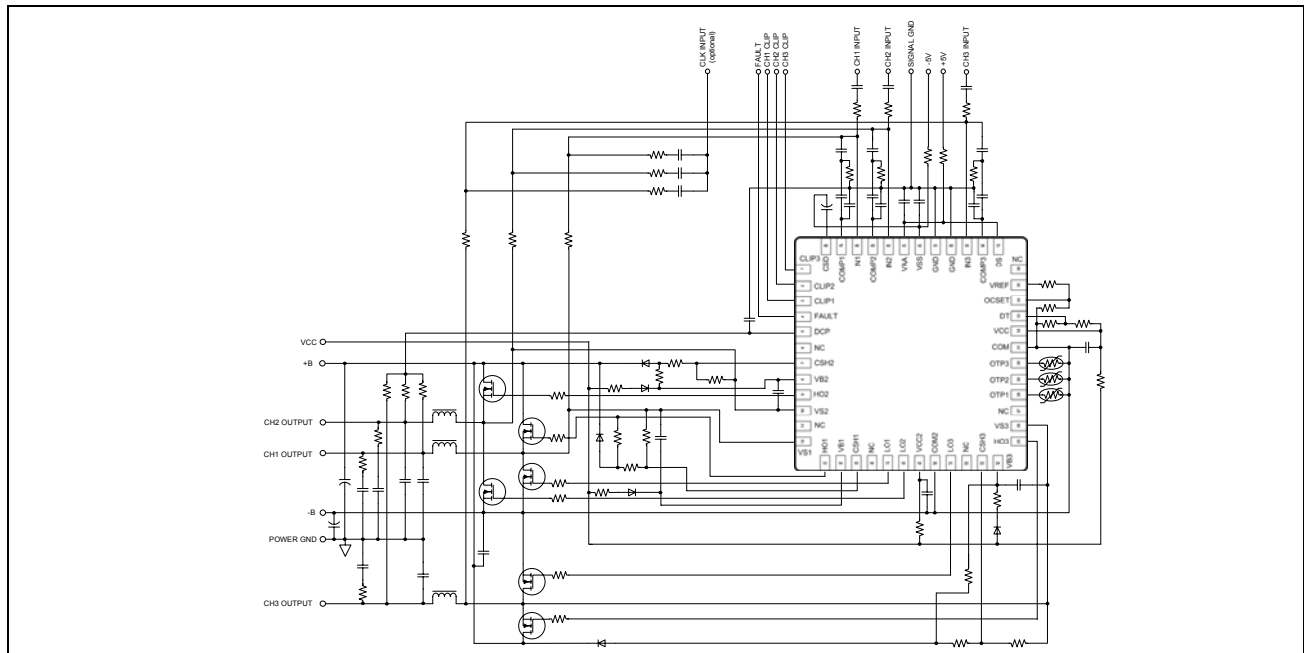
Product Summary

| | |
|--|-----------------|
| Topology | Half-Bridge |
| $V_{\text{OFFSET (max)}}$ | +/- 100 V |
| $I_{\text{O+}} \& I_{\text{O-}}$ (typical) | 0.5 A & 0.6 A |
| Selectable deadtime | 45/65/85/105 ns |
| DC offset | <20 mV |
| Error amplifier open loop gain | >60 dB |

Package



Typical Connection



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Description

The IRS2053 integrates three channels of high voltage, high performance Class D audio amplifier drivers with PWM modulators and protections. In conjunction with external MOSFET and external components, a complete 3 channel Class D audio amplifier can be realized. The IRS2053 is designed with floating analog inputs and protection control interface pin especially for half bridge topology. High and low side MOSFET are protected from over current conditions by a programmable bi-directional current sensing. Essential elements of PWM modulator section allow flexible system design. A small MLPQ48 package enhances the benefit of smaller size of Class D topology.

Qualification Information[†]

| | | |
|-----------------------------------|-------------------------|---|
| Qualification Level | | Industrial ^{††} |
| | | Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level. |
| Moisture Sensitivity Level | | MSL2 ^{†††} , 260°C (per IPC/JEDEC J-STD-020) |
| ESD | Machine Model | Class A (per JEDEC standard EIA/JESD22-A115) |
| | Human Body Model | Class 1C (per EIA/JEDEC standard JESD22-A114) |
| IC Latch-Up Test | | Class I, Level A (per JESD78A) |
| RoHS Compliant | | Yes |

- † Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>
- †† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.
- ††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM; all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

| Symbol | Definition | Min. | Max. | Units |
|--------------|--|------------------------------------|------------------------------------|-------|
| V_{Bn} | High side floating supply voltage | -0.3 | 215 | V |
| V_{Sn} | High side floating supply voltage ^{††} , n=1-3 | $V_{Bn} - 15$ | $V_{Bn} + 0.3$ | V |
| V_{Hon} | High side floating output voltage, n=1-3 | $V_{Sn} - 0.3$ | $V_{Bn} + 0.3$ | V |
| V_{CSHn} | CSH pin input voltage, n=1-3 | $V_{Sn} - 0.3$ | $V_{Bn} + 0.3$ | V |
| V_{CCn} | Low side fixed supply voltage ^{††} , n=1-2 | -0.3 | 20 | V |
| V_{LOn} | Low side output voltage, n=1-3 | -0.3 | VCC2 +0.3 | V |
| V_{AA} | Floating input positive supply voltage ^{††} | (See I_{AAZ}) | 210 | V |
| V_{SS} | Floating input negative supply voltage ^{††} | -1 (See I_{SSZ}) | GND +0.3 | V |
| V_{GND} | Floating input supply ground voltage | $V_{SS} - 0.3$ (See I_{SSZ}) | $V_{AA} + 0.3$ (See I_{AAZ}) | V |
| COM2 | Low side output supply return | -0.3 | +0.3 | V |
| I_{IN-n} | Inverting input current [†] , n=1-3 | - | ±3 | mA |
| V_{CSD} | SD pin input voltage | $V_{SS} - 0.3$ | $V_{AA} + 0.3$ | V |
| V_{COMPn} | COMP pin input voltage, n=1-3 | $V_{SS} - 0.3$ | $V_{AA} + 0.3$ | V |
| V_{DS} | DS pin input voltage | $V_{SS} - 0.3$ | $V_{AA} + 0.3$ | V |
| V_{CLIPn} | CLIP pin input voltage | $V_{SS} - 0.3$ | $V_{AA} + 0.3$ | V |
| I_{CLIPn} | CLIP pin sinking current | - | 5 | mA |
| V_{FAULT} | FAULT pin input voltage | $V_{SS} - 0.3$ | $V_{AA} + 0.3$ | V |
| I_{FAULT} | FAULT pin sinking current | - | 5 | mA |
| V_{DCP} | DCP pin input voltage | (See I_{DCP}) | (See I_{DCP}) | V |
| I_{DCP} | DCP pin sinking/sourcing current | -1 | 1 | mA |
| V_{DT} | DT pin input voltage | -0.3 | $V_{CC} + 0.3$ | V |
| V_{OCSET} | OCSET pin input voltage | -0.3 | $V_{CC} + 0.3$ | V |
| V_{OTPN} | OTP pin input voltage | -0.3 | $V_{CC} + 0.3$ | V |
| I_{AAZ} | Floating input positive supply zener clamp current | - | 20 | mA |
| I_{SSZ} | Floating input negative supply zener clamp current | - | 20 | mA |
| I_{CCZn} | Low side supply zener clamp current ^{†††} , n=1-2 | - | 10 | mA |
| I_{BSZn} | Floating supply zener clamp current ^{†††} , n=1-3 | - | 10 | mA |
| I_{OREF} | Reference output current | - | 5 | mA |
| dV_{Sn}/dt | Allowable V_s voltage slew rate, n=1-3 | - | 50 | V/ns |
| dV_{SS}/dt | Allowable V_{ss} voltage slew rate ^{†††} | - | 50 | V/ms |

Absolute Maximum Ratings (cont'd)

| Symbol | Definition | Min. | Max. | Units |
|--------|--|------|------|-------|
| Pd | Maximum power dissipation @ $T_A \leq +25^\circ\text{C}$ | - | 6.2 | W |
| RthJA | Thermal resistance, Junction to ambient ^{††††} | - | 20 | °C/W |
| RthJC | Thermal resistance, Junction to case | - | 3 | °C/W |
| Tj | Junction Temperature | - | 150 | °C |
| Ts | Storage Temperature | -55 | 150 | °C |
| Tl | Lead temperature (Soldering, 10 seconds) | - | 300 | °C |

† IN-1-3 contains clamping diode to GND.

†† VAA-VSS, Vcc1-COM, Vcc2-COM2, VB1-VS1, VB2-VS2 and VB3-VS3 contain internal shunt zener diodes. Please note that the voltage ratings of these can be limited by the clamping current.

††† For the rising and falling edges of step signal of 10V. Vss=15V to 200V.

†††† According to JESD51-5. JEDEC still air chamber.

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions below. The Vs and COM offset ratings are tested with supplies biased at $V_{AA}-V_{SS}=10V$, $V_{CC}=12V$ and $V_B-V_S=12V$. All voltage parameters are absolute voltages referenced to COM; all currents are defined positive into any lead.

| Symbol | Definition | Min. | Max. | Units |
|-------------|---|-----------------|-----------------|-------|
| V_{Bn} | High side floating supply absolute voltage, n=1-3 | $V_{Sn} + 10$ | $V_{Sn} + 14$ | V |
| V_{Sn} | High side floating supply offset voltage | † | 200 | V |
| I_{AAZ} | Floating input positive supply zener clamp current | 1 | 11 | mA |
| I_{SSZ} | Floating input negative supply zener clamp current | 1 | 11 | mA |
| V_{SS} | Floating input supply absolute voltage | 0 | 200 | V |
| V_{HOn} | High side floating output voltage, n=1-3 | V_S | V_B | V |
| V_{CC} | Low side fixed supply voltage | 10 | 15 | V |
| V_{LOn} | Low side output voltage, n=1-3 | 0 | $V_{CC}2$ | V |
| V_{GND} | GND pin input voltage | V_{SS}^{+++} | V_{AA}^{+++} | V |
| V_{IN-n} | Inverting input voltage, n=1-3 | $V_{GND} - 0.5$ | $V_{GND} + 0.5$ | V |
| V_{CSD} | CSD pin input voltage | V_{SS} | V_{AA} | V |
| V_{COMPn} | COMP pin input voltage, n=1-3 | V_{SS} | V_{AA} | V |
| C_{COMPn} | COMP pin phase compensation capacitor to GND, n=1-3 | 1 | - | nF |
| V_{DT} | DT pin input voltage | 0 | V_{CC} | V |
| I_{OREF} | Reference output current to COM ^{††} | 0.3 | 0.8 | mA |
| V_{OCSET} | OCSET pin input voltage | 0.5 | 5 | V |
| V_{CSHn} | CSH pin input voltage, n=1-3 | V_{Sn} | V_{Bn} | V |
| dVss/dt | Allowable Vss voltage slew rate upon power-up ⁺⁺⁺⁺ | - | 50 | V/ms |
| f_{SW} | Switching Frequency | - | 800 | kHz |
| T_A | Ambient Temperature | -40 | 125 | °C |

† Logic operational for Vsn equal to -5V to +200V. Logic state held for Vsn equal to -5V to - V_{BSn} .

†† Nominal voltage for V_{REF} is 5.1V. I_{OREF} of 0.3 – 0.8mA dictates total external resistor value on VREF to be 6.3k to 16.7k ohm.

+++ GND input voltage is limited by I_{IN-n} .

++++ Vss ramps up from 0V to 200V.

Electrical Characteristics

$V_{CC}=V_{CC2}=V_{BS1}=V_{BS2}=V_{BS3}=12V$, $V_{SS}=V_{S1}=V_{S2}=V_{S3}=COM=0V$, $V_{GND}=5V$, $V_{AA}=10V$, $C_L=1nF$ and $T_A=25^\circ C$ unless otherwise specified.

| Symbol | Definition | Min | Typ | Max | Units | Test Conditions |
|----------------------------------|---|------|------|------|---------|------------------------------------|
| Low Side Supply 1 | | | | | | |
| UV_{CC+} | Vcc supply UVLO positive threshold | 8.4 | 8.9 | 9.4 | V | |
| UV_{CC-} | Vcc supply UVLO negative threshold | 8.2 | 8.7 | 9.2 | V | |
| UV_{CCHYS} | UV_{CC} hysteresis | - | 0.2 | - | V | |
| I_{QCC} | Low side quiescent current | - | 5 | 8 | mA | $V_{DT}=V_{CC}$ |
| $V_{CLAMPL1}$ | Low side zener diode clamp voltage | 19.0 | 20.4 | 21.6 | V | $I_{CC1}=10mA$ |
| Low Side Supply 2 | | | | | | |
| I_{QCC2} | Low side quiescent current | - | 4.2 | 8 | mA | |
| $V_{CLAMPL2}$ | Low side zener diode clamp voltage | 19.6 | 20.4 | 21.6 | V | $I_{CC2}=10mA$ |
| High Side Floating Supply | | | | | | |
| UV_{BS+n} | High side well UVLO positive threshold, n=1-3 | 8.0 | 8.5 | 9.0 | V | |
| UV_{BS-n} | High side well UVLO negative threshold, n=1-3 | 7.8 | 8.3 | 8.8 | V | |
| UV_{BSHYSn} | UV_{BS} hysteresis, n=1-3 | - | 0.2 | - | V | |
| I_{QBSn} | High side quiescent current, n=1-3 | - | 0.5 | 1 | mA | |
| I_{LKHn} | High to Low side leakage current, n=1-3 | - | - | 50 | μA | $V_{Bn}=V_{Sn}=200V$ |
| V_{CLAMPn} | High side zener diode clamp voltage, n=1-3 | 14.7 | 15.3 | 16.2 | V | $I_{BSn}=5mA$ |
| Floating Input Supply | | | | | | |
| UV_{AA+} | $VA+$, $VA-$ floating supply UVLO positive threshold from V_{SS} | 8.2 | 8.7 | 9.2 | V | GND pin floating |
| UV_{AA-} | $VA+$, $VA-$ floating supply UVLO negative threshold from V_{SS} | 7.7 | 8.2 | 8.7 | V | GND pin floating |
| UV_{AAHYS} | UV_{AA} hysteresis | - | 0.5 | - | V | GND pin floating |
| I_{QAA0} | Floating Input positive quiescent supply current in shutdown mode | - | 1 | 3 | mA | $V_{CSD}=V_{SS}$ |
| I_{QAA10} | Floating Input positive quiescent supply current, positive input | - | 12 | 25 | mA | $V_{IN-}=V_{SS}+5.2V$ |
| I_{QAA11} | Floating Input positive quiescent supply current, negative input | - | 9 | 20 | mA | $V_{IN-}=V_{SS}+4.8V$ |
| I_{QAA2} | Floating Input positive quiescent supply current in start-up mode | - | 20 | 35 | mA | $V_{CSD}=V_{SS}+5.0V$ |
| I_{LKM} | Floating input side to Low side leakage current | - | - | 50 | μA | $V_{AA}=V_{SS}=V_{GND}=100V$ |
| V_{CLAMPM} | Floating supply zener diode clamp voltage | 19.6 | 20.4 | 21.6 | V | $I_{AA}=5mA$, $V_{CSD}=V_{SS}$ |

Electrical Characteristics (cont'd)

| Symbol | Definition | Min | Typ | Max | Units | Test Conditions |
|---|---|---------------|-----------------------|---------------|-------|---|
| Audio Input ($V_{GND}=0, V_{AA}=5V, V_{SS}=-5V, COM=COM2=VCC=VCC2=-5V, VS1=VS2=VS3=-5V, CSH1=CSH2=CHS3=-5V, DT=OCSET=-5V$) | | | | | | |
| V_{OSn} | CHn input offset voltage, n=1-3 | -18 | 0 | 18 | mV | |
| I_{BINn} | CHn input bias current, n=1-3 | - | - | 40 | nA | |
| GBWn | CHn small signal bandwidth | - | 9 | - | MHz | $C_{COMPn}=1nF, Rfn=0$ |
| V_{COMPn} | CHn OTA Output voltage, n=1-3 | $V_{AA}-1$ | - | $V_{SS}+1$ | V | |
| g_{mn} | CHn OTA transconductance, n=1-3 | - | 100 | - | mS | $V_{IN-n}=10mV$ |
| G_{Vn} | CHn OTA gain, n=1-3 | 60 | - | - | dB | |
| V_{Nrmsn} | CHn OTA input noise voltage, n=1-3 | - | 250 | - | mVrms | BW=20kHz, Resolution BW=22Hz Fig.5 |
| SRn | CHn slew rate, n=1-3 | - | ± 5 | - | V/us | $C_{COMPn}=1nF$ |
| CMRRn | CHn common-mode rejection ratio, n=1-3 | - | 60 | - | dB | |
| PSRRn | CHn supply voltage rejection ratio, n=1-3 | - | 65 | - | dB | |
| $V_{th+CLIPn}$ | CHn clip detection positive threshold, n=1-3 | $0.85xV_{AA}$ | $0.90xV_{AA}$ | $0.95xV_{AA}$ | V | |
| $V_{th-CLIPn}$ | CHn clip detection negative threshold, n=1-3 | $0.05xV_{AA}$ | $0.10xV_{AA}$ | $0.15xV_{AA}$ | V | |
| t_{CLIPn} | CHn clipping detection propagation delay, n=1-3 | - | 40 | - | ns | |
| $t_{CLIPmin}$ | CHn clipping detection minimum output duration | - | 3 | - | us | |
| PWM comparator | | | | | | |
| V_{thPVM} | PWM comparator threshold in COMP | - | $(V_{AA} - V_{SS})/2$ | - | V | |
| f_{OTAn} | CHn COMP pin star-up local oscillation frequency, n=1-3 | 0.6 | 1.0 | - | MHz | $V_{CSD} = V_{SS}+5V$ |

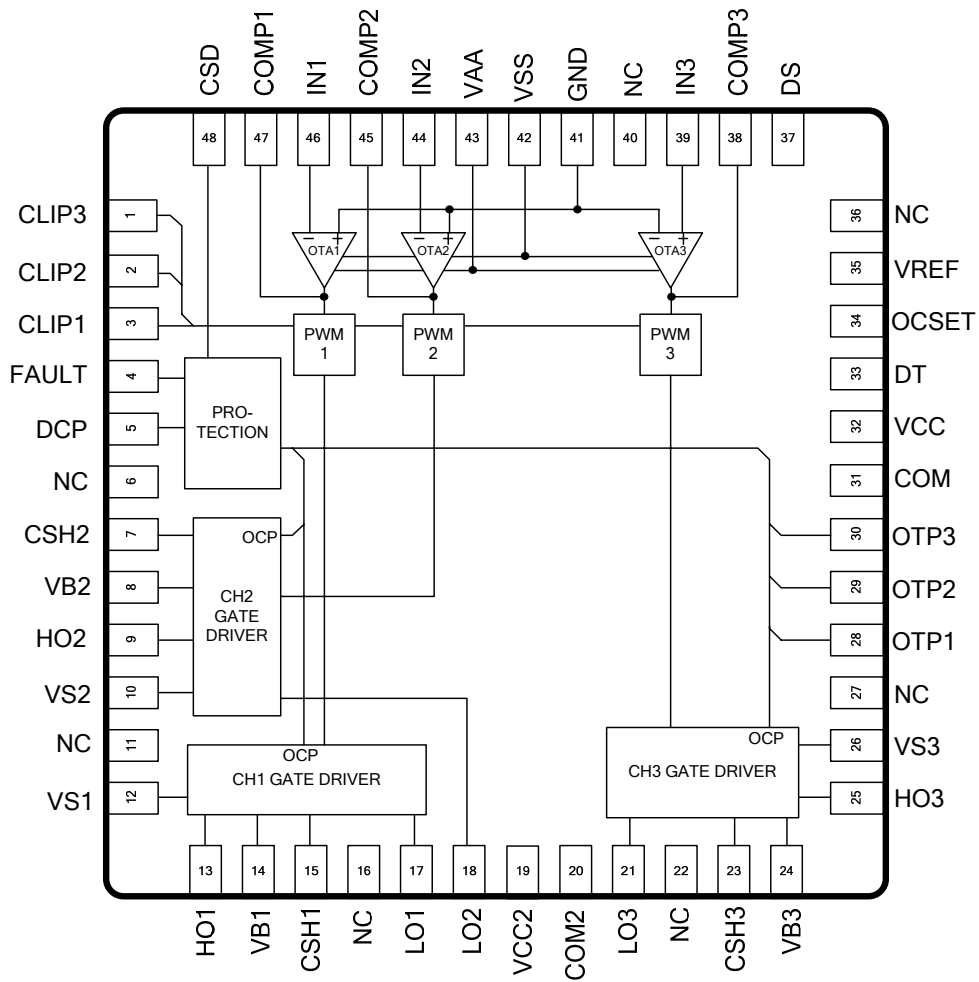
Electrical Characteristics (cont'd)

| Symbol | Definition | Min | Typ | Max | Units | Test Conditions |
|-------------------|---|---------------|---------------|---------------|---------|-------------------------|
| Protection | | | | | | |
| V_{REF} | Reference output voltage | 4.8 | 5.1 | 5.4 | V | $I_{OREF} = 0.5mA$ |
| $V_{th_{OCLn}}$ | CHn low side OC threshold in V_{sn} , n=1-3 | 1.1 | 1.2 | 1.3 | V | OCSET=1.2V |
| $V_{th_{OCHn}}$ | CHn high side OC threshold in V_{CSHn} , n=1-3 | 1.1+ Vs | 1.2+ Vs | 1.3+ Vs | V | Vs=200V |
| V_{DCP+} | DCP pin positive detecting threshold | | 1.3 | | V | |
| V_{DCP-} | DCP pin negative detecting threshold | | -1.3 | | V | |
| V_{DCPZ+} | DCP pin positive clamping voltage | | 3.0 | | V | |
| V_{DCPZ-} | DCP pin negative clamping voltage | | -2.5 | | V | |
| V_{OTPN} | CHn OTP pin threshold, n=1-3 | | 2.8 | | V | |
| I_{OTPN} | CHn OTP bias sourcing current, n=1-3 | | 0.6 | | mA | OTPN=0V |
| V_{CSDH} | CSD pin shutdown release threshold | $0.62xV_{AA}$ | $0.70xV_{AA}$ | $0.78xV_{AA}$ | V | |
| V_{CSDL} | CSD pin self reset threshold | $0.26xV_{AA}$ | $0.30xV_{AA}$ | $0.34xV_{AA}$ | V | |
| I_{CSD+} | CSD pin discharge current | 70 | 100 | 130 | μA | $V_{CSD} = V_{SS} + 5V$ |
| I_{CSD-} | CSD pin charge current | 70 | 100 | 130 | μA | $V_{CSD} = V_{SS} + 5V$ |
| t_{SDn} | CHn shutdown propagation delay from $V_{CSD} > V_{SS} + V_{th_{OCH}}$ to Shutdown | - | - | 250 | ns | |
| t_{OCHn} | CHn propagation delay time from $V_{CSHn} > V_{th_{OCHn}}$ to Shutdown, n=1-3 | - | - | 500 | ns | Fig.4 |
| t_{OCLn} | CHn propagation delay time from $V_{sn} > V_{th_{OCL}}$ to Shutdown, n=1-3 | - | - | 500 | ns | Fig.3 |
| $t_{OCLFAULT}$ | CH1 propagation delay time from $V_{s1} > V_{th_{OCL}}$ to FAULT | - | 285 | - | ns | |

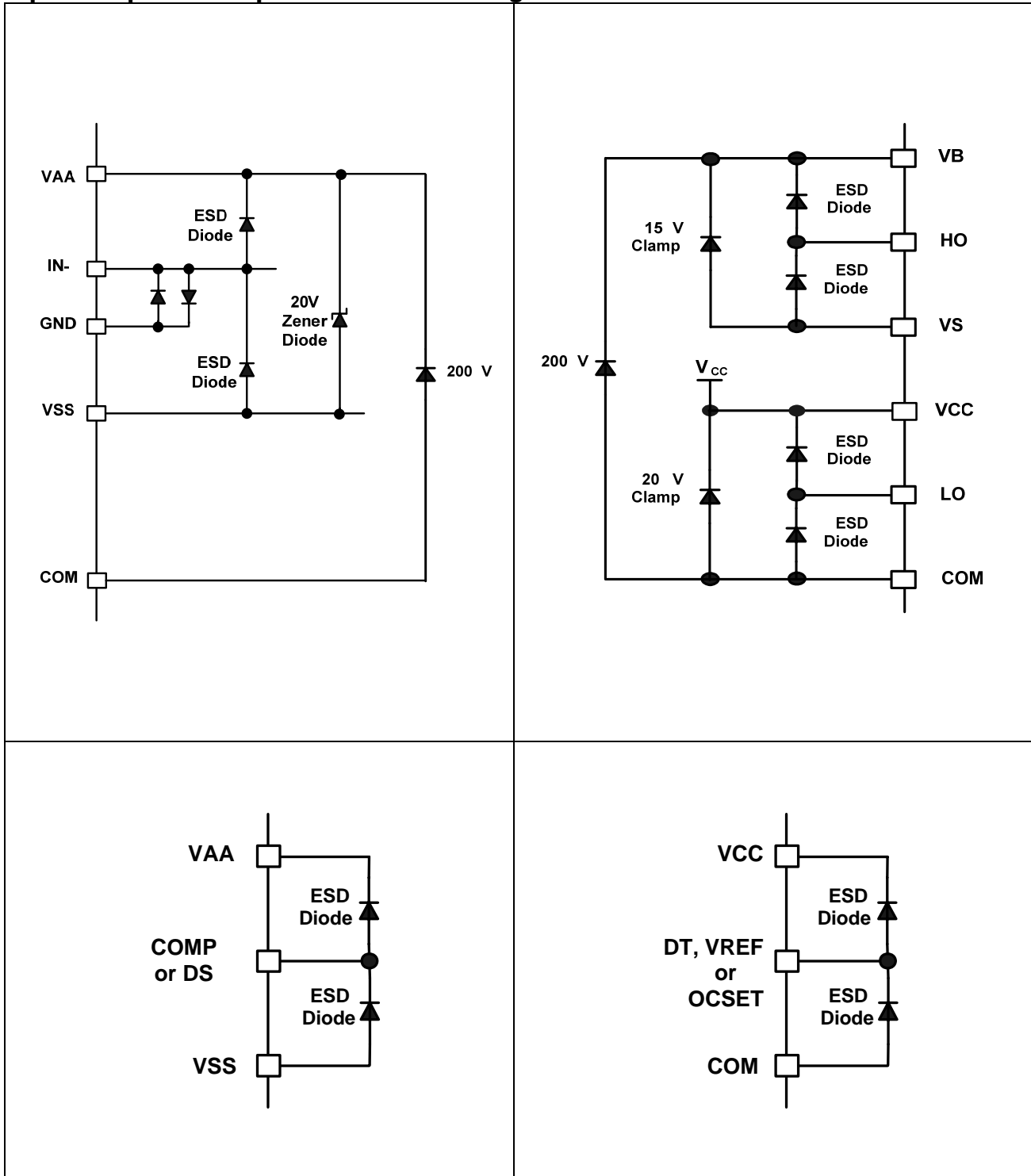
Electrical Characteristics (cont'd)

| Symbol | Definition | Min | Typ | Max | Units | Test Conditions |
|--------------------|--|----------------------|----------------------|----------------------|-------|----------------------------------|
| Gate Driver | | | | | | |
| I_{o+n} | CHn output high short circuit current (Source), n=1-3 | - | 0.5 | - | A | $V_o=0V$, $PW<10\mu S$ |
| I_{o-n} | CHn output low short circuit current (Sink), n=1-3 | - | 0.6 | - | A | $V_o=12V$, $PW<10\mu S$ |
| V_{OLn} | CHn low level out put voltage LO – COM, HO - VS, n=1-3 | - | - | 0.1 | V | $I_o=0A$ |
| V_{OHn} | CHn high level out put voltage VCC – LO, VB - HO, n=1-3 | - | - | 1.4 | V | |
| T_{on0n} | CHn high and low side turn-on propagation delay, n=1-3 | - | 350 | - | ns | $V_{DT} = V_{CC}, V_{DS}=V_{AA}$ |
| T_{off0n} | CHn high and low side turn-off propagation delay, n=1-3 | - | 325 | - | ns | |
| T_{on1n} | CHn high and low side turn-on propagation delay, n=1-3 | - | 145 | - | ns | $V_{DT} = V_{CC}, V_{DS}=V_{SS}$ |
| T_{off1n} | CHn high and low side turn-off propagation delay, n=1-3 | - | 100 | - | ns | |
| t_r | Turn-on rise time | - | 25 | 50 | ns | |
| t_f | Turn-off fall time | - | 20 | 40 | ns | |
| DT_{1n} | CHn deadtime: LOn turn-off to HOn turn-on (DT_{LO-HO}) & HOn turn-off to LnO turn-on (DT_{HO-LO}) | 30 | 45 | 60 | ns | $V_{DT}>V_{DT1}$, |
| DT_{2n} | CHn deadtime: LOn turn-off to HOn turn-on (DT_{LO-HO}) & HOn turn-off to LOn turn-on (DT_{HO-LO}) | 45 | 65 | 85 | ns | $V_{DT1}>V_{DT}>V_{DT2}$, |
| DT_{3n} | CHn deadtime: LOn turn-off to HOn turn-on (DT_{LO-HO}) & HOn turn-off to LOn turn-on (DT_{HO-LO}) | 60 | 85 | 110 | ns | $V_{DT2}>V_{DT}>V_{DT3}$, |
| DT_{4n} | CHn deadtime: LOn turn-off to HOn turn-on (DT_{LO-HO}) & HO turn-off to LOn turn-on (DT_{HO-LO}) $V_{DT}=V_{DT4}$ | 80 | 105 | 145 | ns | $V_{DT}<V_{DT3}$ |
| V_{DT1} | DT mode select threshold 1 | $0.51 \times V_{CC}$ | $0.57 \times V_{CC}$ | $0.63 \times V_{CC}$ | V | |
| V_{DT2} | DT mode select threshold 2 | $0.32 \times V_{CC}$ | $0.36 \times V_{CC}$ | $0.40 \times V_{CC}$ | V | |
| V_{DT3} | DT mode select threshold 3 | $0.21 \times V_{CC}$ | $0.23 \times V_{CC}$ | $0.25 \times V_{CC}$ | V | |
| $V_{th_{DS}}$ | DS pin input threshold | $0.4 \times V_{AA}$ | $0.5 \times V_{AA}$ | $0.6 \times V_{AA}$ | V | $V_{SS} = 0V$ |

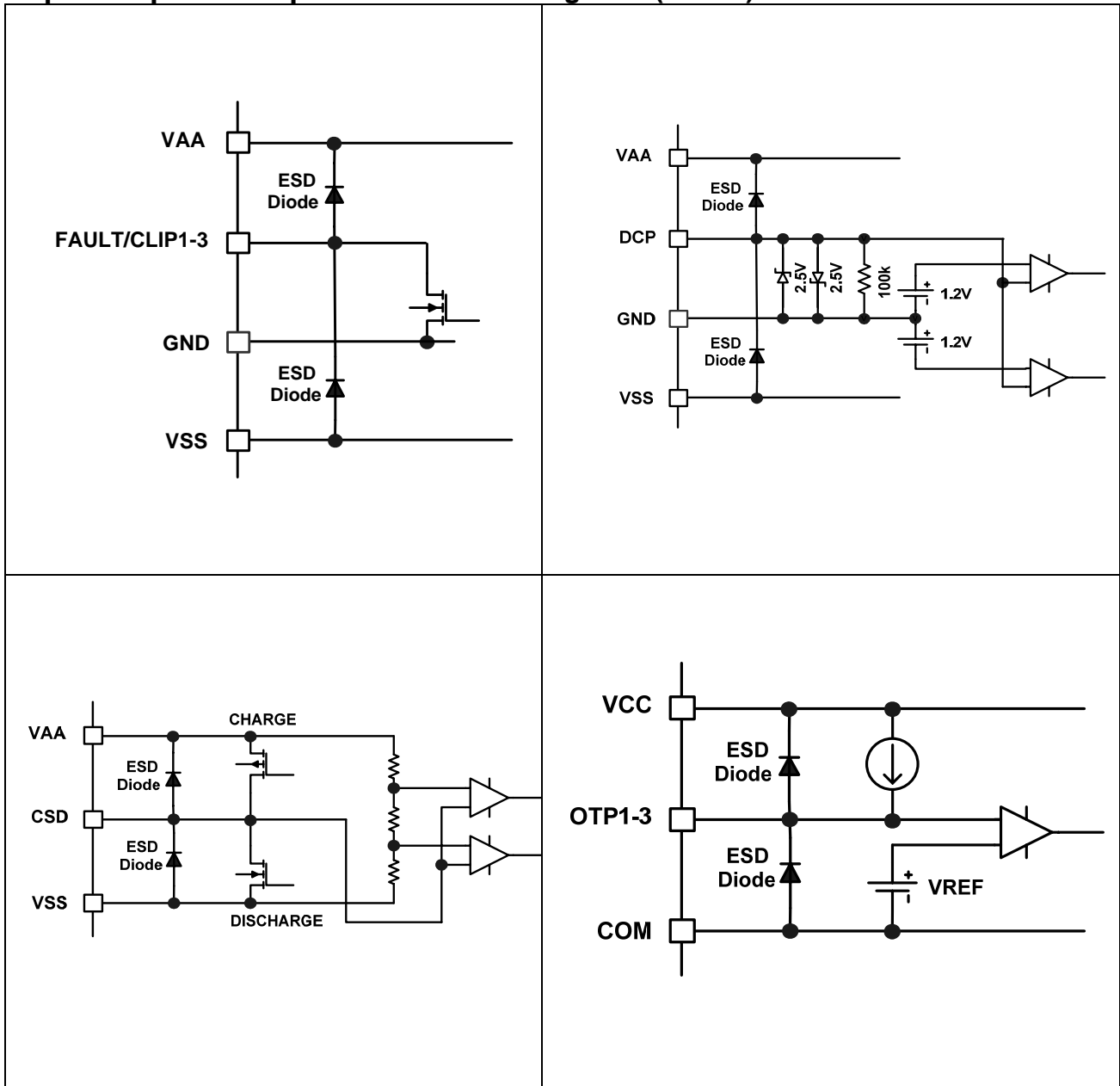
Functional Block Diagram



Input/Output Pin Equivalent Circuit Diagrams



Input/Output Pin Equivalent Circuit Diagrams (cont'd)

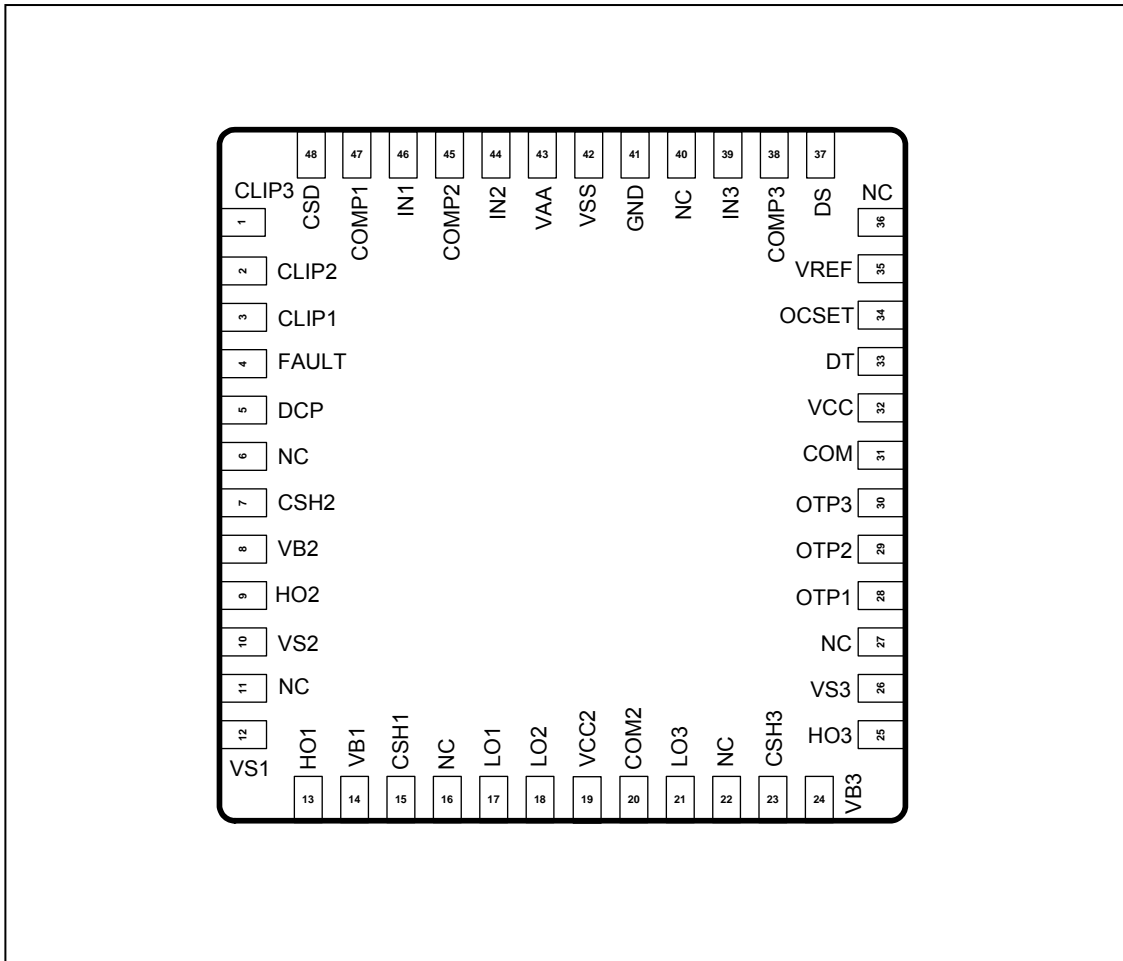


Lead Definitions

| Pin # | Symbol | Description |
|-------|--------|--|
| 1 | CLIP3 | Clipping detection output CH1, open drain, referenced to GND |
| 2 | CLIP2 | Clipping detection output CH2, open drain, referenced to GND |
| 3 | CLIP1 | Clipping detection output CH3, open drain, referenced to GND |
| 4 | FAULT | Fault output, open drain, referenced to GND |
| 5 | DCP | DC offset protection input |
| 6 | NC | |
| 7 | CSH2 | CH2 High side over current sensing input, referenced to VS2 |
| 8 | VB2 | CH2 High side floating supply |
| 9 | HO2 | CH2 High side output |
| 10 | VS2 | CH2 High side floating supply return |
| 11 | NC | |
| 12 | VS1 | CH1 High side floating supply return |
| 13 | HO1 | CH1 High side output |
| 14 | VB1 | CH1 High side floating supply |
| 15 | CSH1 | CH1 High side over current sensing input, referenced to VS1 |
| 16 | NC | |
| 17 | LO1 | CH1 Low side output |
| 18 | LO2 | CH2 Low side output |
| 19 | VCC2 | Low side gate drive supply |
| 20 | COM2 | Low side gate drive supply return |
| 21 | LO3 | CH3 Low side output |
| 22 | NC | |
| 23 | CSH3 | CH3 High side over current sensing input, referenced to VS3 |
| 24 | VB3 | CH3 High side floating supply |

| Pin # | Symbol | Description |
|-------|--------|--|
| 25 | HO3 | CH3 High side output |
| 26 | VS3 | CH3 High side floating supply return |
| 27 | NC | |
| 28 | OTP1 | Over temperature sensor input 1 |
| 29 | OTP2 | Over temperature sensor input 2 |
| 30 | OTP3 | Over temperature sensor input 3 |
| 31 | COM | Low side gate drive supply return |
| 32 | VCC | Low side gate drive supply |
| 33 | DT | Deadtime program, reference to COM |
| 34 | OCSET | Low side OCP threshold, referenced to COM |
| 35 | VREF | 5.1V reference voltage output for OCSET |
| 36 | NC | |
| 37 | DS | Propagation delay select (VAA: Normal, VSS: Shorter) |
| 38 | COMP3 | CH3 PWM comparator input |
| 39 | IN3 | CH3 inverting audio input |
| 40 | NC | |
| 41 | GND | Input reference GND |
| 42 | VSS | Floating input negative supply |
| 43 | VAA | Floating input positive supply |
| 44 | IN2 | CH2 inverting audio input |
| 45 | COMP2 | CH2 PWM comparator input |
| 46 | IN1 | CH1 inverting audio input |
| 47 | COMP1 | CH1 PWM comparator input |
| 48 | CSD | Protection timer capacitor |

Lead Assignments



Application Information and Additional Details

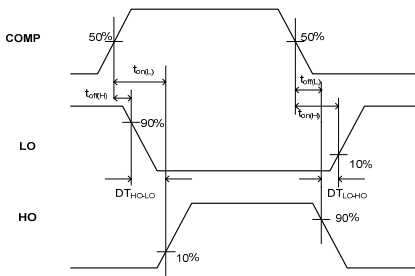


Figure 1 Switching Time Waveform Definitions

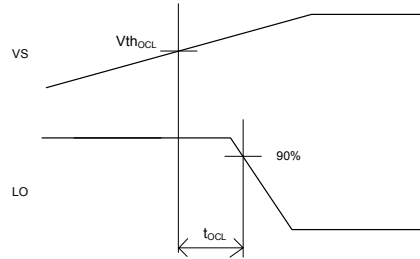


Figure 3 $V_s > V_{thOCL}$ to Shutdown Waveform

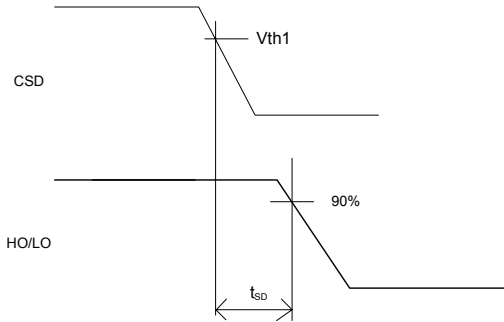


Figure 2 CSD to Shutdown Waveform Definitions

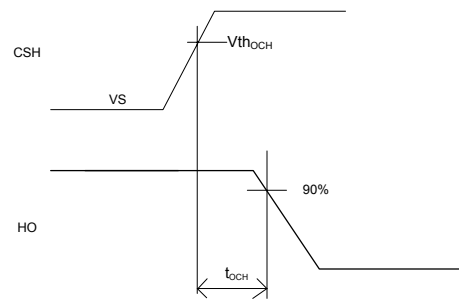


Figure 4 $V_{CSh} > V_{thOCH}$ to Shutdown Waveform

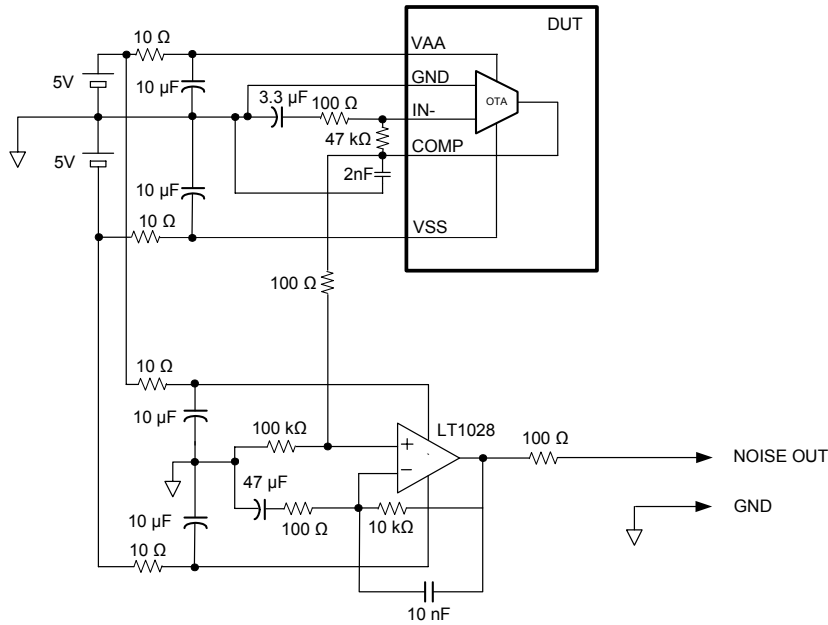
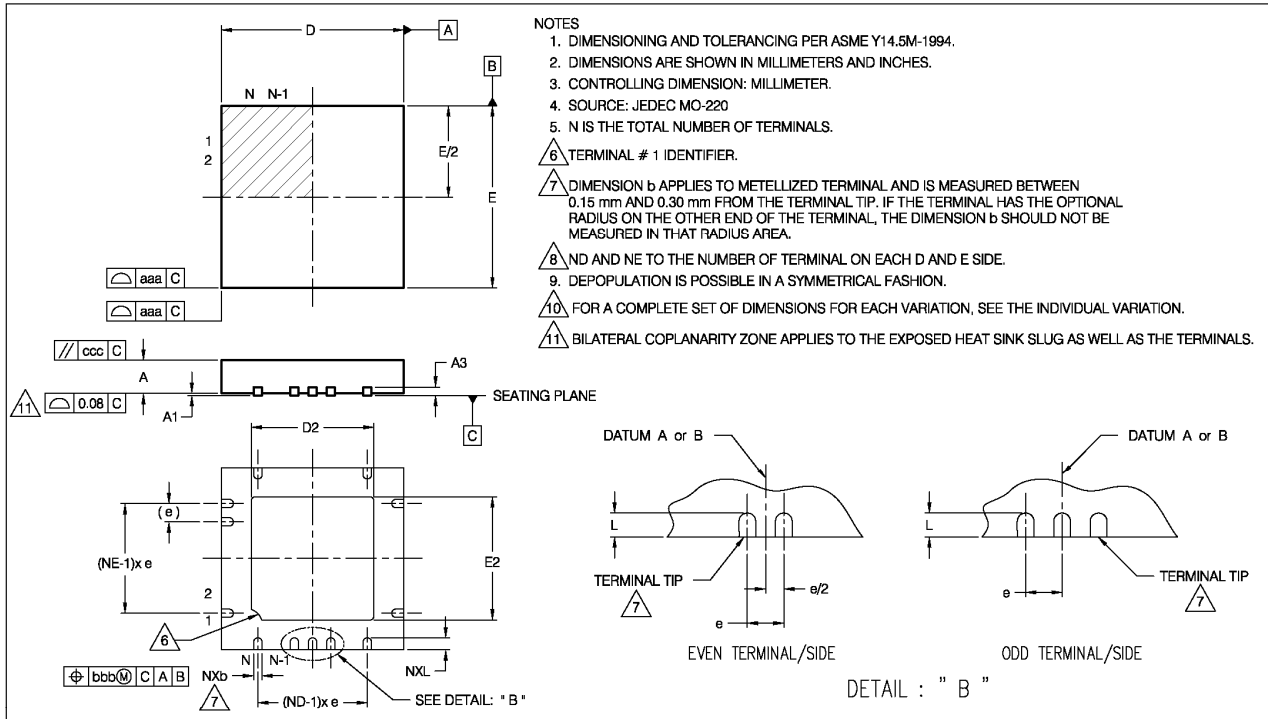


Figure 5: OTA input noise voltage measurement circuit

Package Details: MLPQ 7X7



| VER. | ESCN NUMBER | BY | DATE | APPROVAL INITIALS |
|------|--------------------------|-----|---------|-------------------|
| 7 | REVISED PER ESCN 0421-06 | GCR | 8/7/06 | |
| 8 | REVISED PER ESCN 37678 | GCR | 12/6/06 | |
| 9 | REVISED PER ESCN 37834 | GCR | 1/8/07 | |
| 10 | REVISED PER ESCN 38363 | GCR | 2/5/07 | |
| 11 | REVISED PER ESCN 45228 | GCR | 2/2/09 | |
| 12 | REVISED PER ESCN 45324 | GCR | 2/19/09 | A. B. |

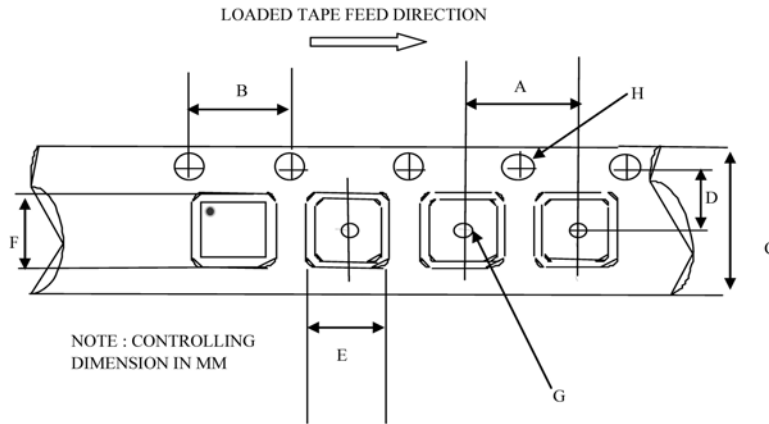
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE: IN INCHES
TOLERANCES ARE:
DECIMALS
.X = +/-
.XX = +/-
.XXX = +/-
.XXXX = +/-
.XXXXX = +/-
ANGLES
∠ = +/- .5°

QFN (MLPQ, MLF) PACKAGE OUTLINE

| | | | | |
|----------------------|---------------------|----------------------------|-------------|------|
| DRAWN BY | G. C. RAMOS 5/4/04 | IR INTERNATIONAL RECTIFIER | | |
| APPROVED BY | A. CALICDAN | EL SEGUNDO, CALIFORNIA | | |
| SIGNATURE & DATE | A. Calicdan 2/19/09 | CAD GENERATED | | |
| DO NOT SCALE DRAWING | SCALE ENLGMT | SHEET | DRAWING NO. | VER. |
| | | 1 / 3 | 01-3086 | 12 |

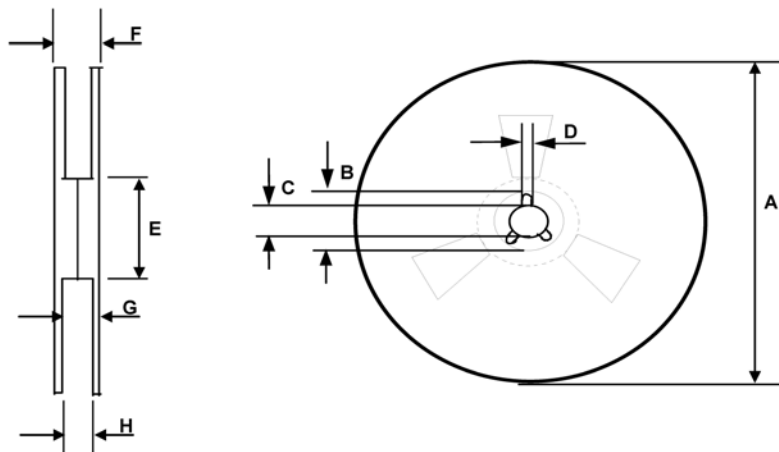
| VKKD-4NJ1 | | | | | |
|-------------|------|------|------------|-------|-------|
| MILLIMETERS | | | INCHES | | |
| MIN | NOM | MAX | MIN | NOM | MAX |
| 0.80 | 0.90 | 1.00 | .032 | .035 | .039 |
| 0.00 | 0.02 | 0.05 | .000 | .0008 | .0019 |
| 0.20 REF | | | .008 REF | | |
| 0.18 | 0.25 | 0.30 | .0071 | .0098 | .0118 |
| 5.40 | 5.55 | 5.65 | .213 | .219 | .222 |
| 7.00 BSC | | | .276 BSC | | |
| 7.00 BSC | | | .276 BSC | | |
| 5.40 | 5.55 | 5.65 | .213 | .219 | .222 |
| 0.30 | 0.40 | 0.50 | .012 | .016 | .020 |
| 0.50 PITCH | | | .020 PITCH | | |
| 48 | | | 48 | | |
| 12 | | | 12 | | |
| 12 | | | 12 | | |
| 0.15 | | | .0059 | | |
| 0.10 | | | .0039 | | |
| 0.10 | | | .0039 | | |
| 0.05 | | | .0019 | | |

Tape and Reel Details: MLPQ 7X7



CARRIER TAPE DIMENSION FOR 48MLPQ7X7

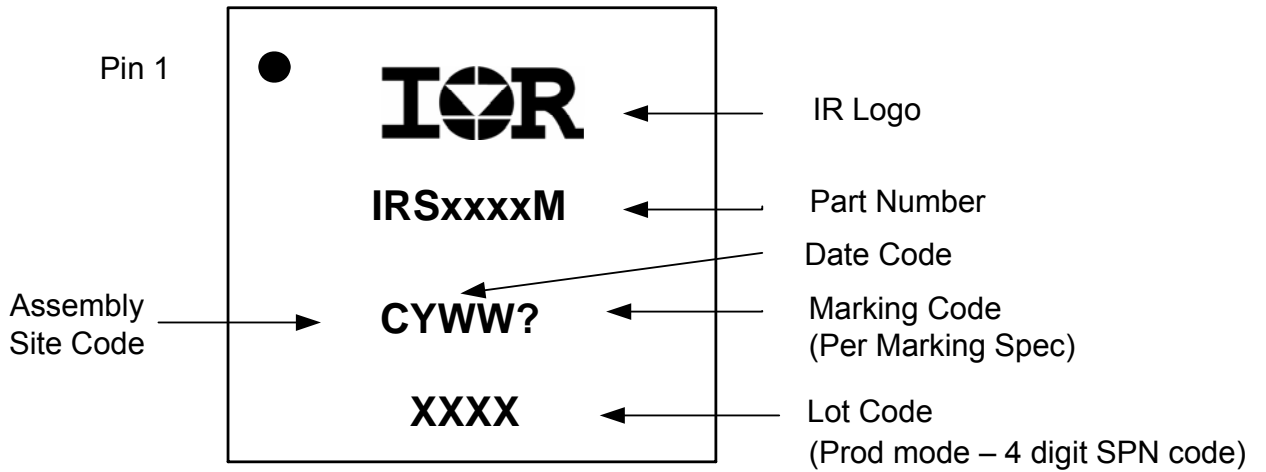
| Code | Metric | | Imperial | |
|------|--------|-------|----------|-------|
| | Min | Max | Min | Max |
| A | 11.90 | 12.10 | 0.474 | 0.476 |
| B | 3.90 | 4.10 | 0.153 | 0.161 |
| C | 15.70 | 16.30 | 0.618 | 0.641 |
| D | 7.40 | 7.60 | 0.291 | 0.299 |
| E | 7.15 | 7.35 | 0.281 | 0.289 |
| F | 7.15 | 7.35 | 0.281 | 0.289 |
| G | 1.50 | n/a | 0.059 | n/a |
| H | 1.50 | 1.60 | 0.059 | 0.062 |



REEL DIMENSIONS FOR 48MLPQ7X7

| Code | Metric | | Imperial | |
|------|--------|--------|----------|--------|
| | Min | Max | Min | Max |
| A | 329.60 | 330.25 | 12.976 | 13.001 |
| B | 20.95 | 21.45 | 0.824 | 0.844 |
| C | 12.80 | 13.20 | 0.503 | 0.519 |
| D | 1.95 | 2.45 | 0.767 | 0.096 |
| E | 98.00 | 102.00 | 3.858 | 4.015 |
| F | n/a | 22.4 | n/a | 0.881 |
| G | 18.5 | 21.1 | 0.728 | 0.83 |
| H | 16.4 | 18.4 | 0.645 | 0.724 |

Part Marking Information



Ordering Information

| Base Part Number | Package Type | Standard Pack | | Complete Part Number |
|------------------|--------------|---------------|----------|----------------------|
| | | Form | Quantity | |
| IRS2053M | MLPQ 48 7x7 | Tube / Bulk | 52 | IRS2053MPBF |
| | | Tape and Reel | 3000 | IRS2053MTRPBF |

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<http://www.irf.com/technical-info/>

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