SRC419x 192-kHz Stereo Asynchronous Sample-Rate Converters

1 Features

- Automatic Sensing of the Input-to-Output Sampling Ratio
- Wide Input-to-Output Sampling Range: 16:1 to 1:16
- Supports Input and Output Sampling Rates Up to 212 kHz
- Dynamic Range: 144 dB (–60-dbFS Input, BW = 20 Hz to f_S/2, A-Weighted)
- THD+N: –140 dB (0-dbFS Input, BW = 20 Hz to f_S/2)
- Attenuates Sampling and Reference Clock Jitter
- High-Performance, Linear-Phase Digital Filtering with Stop Band Attenuation Greater than 140 dB
- Flexible Audio Serial Ports:
  - Master or Slave-Mode Operation
  - Supports I^2S, Left-Justified, Right-Justified, and TDM Data Formats
  - Supports 16, 18, 20, or 24-Bit Audio Data
  - TDM Mode Allows Daisy-Chaining of up to Eight Devices
- Supports 24-, 20-, 18-, or 16-Bit Input and Output Data: All Output Data is Dithered from the Internal 28-Bit Data Path
- Low Group Delay Option for Interpolation Filter
- Direct Downsampling Option for Decimation Filter (SRC4193 Only)
- SPI Port Provides Access to Internal Control Registers (SRC4193 Only)
- Soft Mute Function
- Bypass Mode
- Programmable Digital Output Attenuation (SRC4193 Only); 256 Steps: 0 dB to –127.5 dB, 0.5-dB/step
- Power Down Mode
- Operates From a Single 3.3-V Power Supply
- Small 28-Pin SSOP Package
- Pin Compatible with the AD1896 (SRC4192 Only)

2 Applications

- Digital Mixing Consoles
- Digital Audio Workstations
- Audio Distribution Systems
- Broadcast Studio Equipment
- High-End A/V Receivers
- General Digital Audio Processing

3 Description

The SRC4192 and SRC4193 devices are asynchronous, sample-rate converters designed for professional and broadcast audio applications. The SRC4192 and SRC4193 devices combine a wide input-to-output sampling ratio with outstanding dynamic range and ultra-low distortion. Input and output serial ports support standard audio formats, as well as a Time Division Multiplexed (TDM) mode. Flexible audio interfaces allow the SRC4192 and SRC4193 devices to connect to a wide range of audio data converters, digital audio receivers and transmitters, and digital signal processors.

The SRC4192 device is a standalone, pin-programmed device, with control pins for mode, data format, mute, bypass, and low group-delay functions. The SRC4193 device is a software-controlled device featuring a serial peripheral interface (SPI) port, which is utilized to program all functions through the internal control registers.

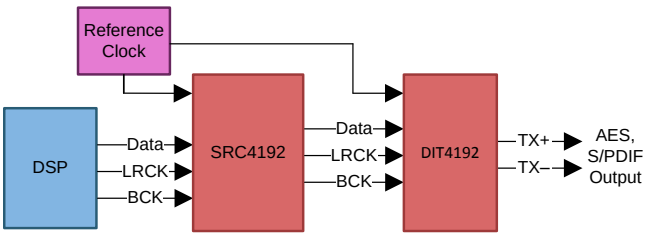
The SRC4192 and SRC4193 devices can operate from a single 3.3-V power supply. A separate digital I/O supply (V_{IO}) operates over the 1.65-V to 3.6-V supply range, allowing greater flexibility when interfacing to current and future generation signal processors and logic devices. Both devices are available in a 28-pin SSOP package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SRC4192	SSOP (28)	5.30 mm × 10.20 mm
SRC4193		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Application Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2007) to Revision C **Page**

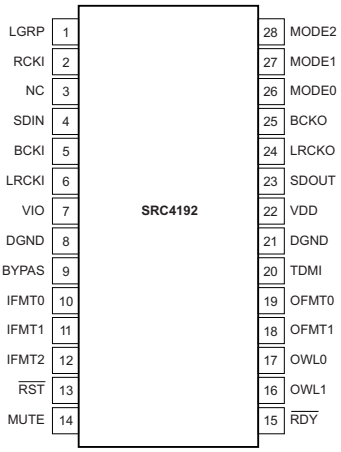
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision A (July 2003) to Revision B **Page**

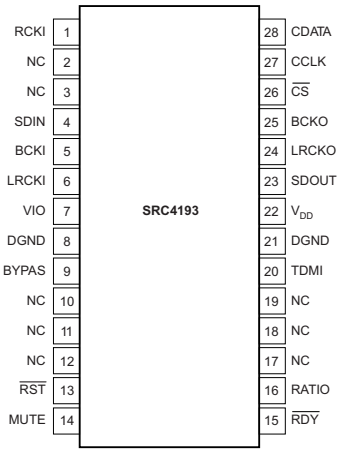
- Added U.S. patent number to note (1) U.S. Patent No. 7,262,716. ... 1

5 Pin Configuration and Functions

SRC4192 DB Package
28-Pin SSOP
Top View



SRC4193 DB Package
28-Pin SSOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SRC4192	SRC4193		
BCKI	5	5	I	Input port bit clock I/O
BCKO	25	25	O	Output port bit clock I/O
BYPAS	9	9	I	ASRC bypass control input (Active High)
CCLK	—	27	I	SPI port data clock input
CDATA	—	28	I	SPI port serial data input
$\overline{CS}$	—	26	I	SPI port chip select input (Active Low)
DGND	8, 21	8, 21	–	Digital ground
IFMT0	10	—	I	Input port data format control input
IFMT1	11	—	I	Input port data format control input
IFMT2	12	—	I	Input port data format control input
LGRP	1	—	I	Low group delay control input (active high)
LRCKI	6	6	I	Input port left/right word clock I/O
LRCKO	24	24	O	Output port left/right word clock I/O
MODE0	26	—	I	Serial port mode control input
MODE1	27	—	I	Serial port mode control input
MODE2	28	—	I	Serial port mode control input
MUTE	14	14	I	Output mute control input (active high)
NC	3	2,3,10,11,12, 17,18,19	–	No connection
OFMT0	19	—	I	Output port data format control input
OFMT1	18	—	I	Output port data format control input
OWL0	17	—	I	Output port data word length control input
OWL1	16	—	I	Output port data word length control input
RATIO	—	16	O	Input-to-output ratio flag output Low output denotes output rate lower than input rate. High output denotes output rate higher than input rate.
RCKI	2	1	I	Reference Clock Input
$\overline{RDY}$	15	15	O	ASRC Ready Status Output (Active Low)

Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	SRC4192	SRC4193		
$\overline{RST}$	13	13	I	Reset Input (Active Low)
SDIN	4	4	I	Audio Serial Data Input
SDOUT	23	23	O	Audio Serial Data Output
TDMI	20	20	I	TDM Data Input (Connect to DGND when not in use)
V_{DD}	22	22	I	Digital Core Supply, 3.3 V
V_{IO}	7	7	I	Digital I/O Supply, 1.65 V to V_{DD}

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply Voltage	V_{DD}	–0.3	4	V
	V_{IO}	–0.3	4	
Digital Input Voltage		–0.3	4	
Operating Temperature		–45	85	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±3000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	V_{DD}	3	3.3	3.6	V
	V_{IO} 1.8 V	1.65	1.8	1.95	
	V_{IO} 3.3 V	3	3.3	3.6	
Operating temperature		–45		85	°C

6.4 Thermal Information

THERMAL METRIC[1]		SRC4192 SRC4193 DB (SSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

All parameters specified with T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE[1]							
	Resolution				24		Bits
f_{SIN}	Input sampling frequency			4		212	kHz
f_{SOUT}	Output sampling frequency			4		212	kHz
	Input: output sampling ratio	Upsampling				1:16	
		Downsampling				16:1	
	Dynamic range	44.1 kHz; 48 kHz	BW = 20 Hz to f_{SOUT}/2, –60-dBFS Input f_{IN} = 1 kHz, Unweighted (add 3 dB to spec for A-weighted result)		140		dB
		48 kHz; 44.1 kHz			140		
		48 kHz; 96 kHz			140		
		44.1 kHz; 192 kHz			138		
		96 kHz; 48 kHz			141		
		192 kHz; 12 kHz			141		
		192 kHz; 32 kHz			141		
		192 kHz; 48 kHz			141		
		32 kHz; 48 kHz			140		
		12 kHz; 192 kHz			138		
	Total harmonic distortion + noise	44.1 kHz; 48 kHz	BW = 20 Hz to f_{SOUT}/2, 0-dBFS Input f_{IN} = 1 kHz, Unweighted		–140		dB
		48 kHz; 44.1 kHz			–140		
		48 kHz; 96 kHz			–140		
		44.1 kHz; 192 kHz			–137		
		96 kHz; 48 kHz			–140		
		192 kHz; 12 kHz			–140		
		192 kHz; 32 kHz			–141		
		192 kHz; 48 kHz			–141		
		32 kHz; 48 kHz			–140		
		12 kHz; 192 kHz			–137		
	Interchannel gain mismatch				0		dB
	Interchannel phase deviation				0		°
	Digital attenuation	Minimum	SRC4193 Only		0		dB
		Maximum			–127.5		
		Step Size			0.5		
	Mute attenuation		24-Bit Word Length, A-weighted		–144		dB
DIGITAL INTERPOLATION FILTER CHARACTERISTICS							
	Passband					0.4535 × f_{SIN}	Hz
	Passband ripple					±0.007	dB
	Transition band			0.4535 × f_{SIN}		0.5465 × f_{SIN}	Hz
	Stop band			0.5465 × f_{SIN}			Hz
	Stop band attenuation			–144			dB

(1) Dynamic performance measured with an Audio Precision System Two Cascade or Cascade Plus.

Electrical Characteristics (continued)

All parameters specified with T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Normal group delay (LGRP = 0)	Decimation Filter On (DFLT = 0)		102.53125/f_{SIN}		s
		Decimation Filter Off (DFLT = 1)		102/f_{SIN}		
	Low group delay (LGRP = 1)	Decimation Filter On (DFLT = 0)		70.53125/f_{SIN}		s
		Decimation Filter Off (DFLT = 1)		70/f_{SIN}		
DIGITAL DECIMATION FILTER CHARACTERISTICS						
	Passband				0.4535 × f_{SOUT}	Hz
	Passband ripple				±0.008	dB
	Transition band		0.4535 × f_{SOUT}		0.5465 × f_{SOUT}	Hz
	Stop band		0.5465 × f_{SOUT}			Hz
	Stop band attenuation		–143			dB
	Group delay – decimation filter	DFLT = 0 for SRC4193		36.46875/f_{SOUT}		s
	Direct downsampling	SRC4193 only, DFLT = 1		0		s
DIGITAL I/O CHARACTERISTICS						
V_{IH}	High-level input voltage		0.7 × V_{IO}		V_{IO}	V
V_{IL}	Low-level input voltage		0		0.3 × V_{IO}	V
I_{IH}	High-level input current			0.5	10	µA
I_{IL}	Low-level input current			0.5	10	µA
V_{OH}	High-level output voltage	I_O = –4 mA	0.8 × V_{IO}		V_{IO}	V
V_{OL}	Low-level output voltage	I_O = +4 mA	0		0.2 × V_{IO}	V
C_{IN}	Input Capacitance			3		pF
POWER SUPPLIES						
	Operating voltage, V_{DD}		3	3.3	3.6	V
	Operating voltage, V_{IO}		1.65	3.3	3.6	
	Supply current, I_{DD}, power down	V_{DD} = 3.3 V, V_{IO} = 3.3 V, $\overline{RST}$ = 0, No Clocks			100	µA
		SRC4193 only, V_{DD} = 3.3 V, V_{IO} = 3.3 V, $\overline{PDN}$ Bit = 0, No Clocks		5		mA
	Supply current, I_{DD}, dynamic	V_{DD} = 3.3 V, V_{IO} = 3.3 V, f_{SIN} = f_{SOUT} = 192 kHz		66		mA
	Supply current, I_{IO}, power down	V_{DD} = 3.3 V, V_{IO} = 3.3 V, $\overline{RST}$ = 0, No Clocks			100	µA
		SRC4193 only, V_{DD} = 3.3 V, V_{IO} = 3.3 V, $\overline{PDN}$ Bit = 0, No Clocks		21		
	Supply current, I_{IO}, dynamic	V_{DD} = 3.3 V, V_{IO} = 3.3 V, f_{SIN} = f_{SOUT} = 192 kHz		2		mA
	Total power dissipation, P_D, power down	V_{DD} = 3.3 V, V_{IO} = 3.3 V, $\overline{RST}$ = 0, No Clocks			660	µW
		SRC4193 only, V_{DD} = 3.3 V, V_{IO} = 3.3 V, $\overline{PDN}$ Bit = 0, No Clocks		16.6		mW
	Total power dissipation, P_D, dynamic	V_{DD} = 3.3 V, V_{IO} = 3.3 V, f_{SIN} = f_{SOUT} = 192 kHz		225		mW

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE CLOCK TIMING						
	RCKI frequency	f_{SMIN} = min (f_{SIN}, f_{SOUT}), f_{SMAX} = max (f_{SIN}, f_{SOUT})	128 × f_{SMIN}		50	MHz
t_{RCKIP}	RCKI period		20		1/(128 × f_{SMIN})	ns
t_{RCKIH}	RCKI pulsewidth high		0.4 × t_{RCKIP}			ns
t_{RCKIL}	RCKI pulsewidth low		0.4 × t_{RCKIP}			ns
RESET TIMING						
t_{RSTL}	$\overline{RST}$ pulse width low		500			ns
	Delay following $\overline{RST}$ rising edge	SRC4193 only	500			µs
INPUT SERIAL PORT TIMING						
t_{LRIS}	LRCKI to BCKI setup time		10			ns
t_{SIH}	BCKI pulsewidth high		10			ns

Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SIL}	BCKI pulsewidth low		10			ns
t_{LDIS}	SDIN data setup time		10			ns
t_{LDIH}	SDIN data hold time		10			ns
OUTPUT SERIAL PORT TIMING						
t_{DOPD}	SDOUT data delay time				10	ns
t_{DOH}	SDOUT data hold time		2			ns
t_{SOH}	BCKO pulsewidth high		10			ns
t_{SOL}	BCKO pulsewidth low		5			ns
TDM MODE TIMING						
t_{LROS}	LRCKO setup time		10			ns
t_{LROH}	LRCKO hold time		10			ns
t_{TDMS}	TDMI data setup time		10			ns
t_{TDMH}	TDMI data hold time		10			ns
SPI TIMING						
	CCLK frequency				25	MHz
t_{CDS}	CDATA setup time		12			ns
t_{CDH}	CDATA hold time		8			ns
t_{CSCR}	$\overline{CS}$ falling to CCLK rising		15			ns
t_{CFCS}	CCLK falling to $\overline{CS}$ rising		12			ns

6.7 Typical Characteristics

At T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.

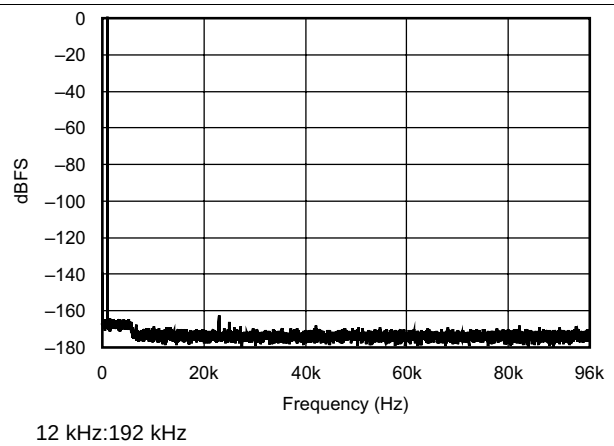


Figure 1. FFT With 1-kHz Input Tone at 0 dBFS

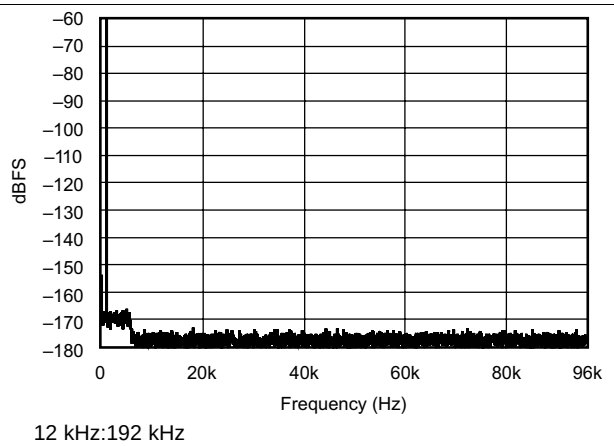
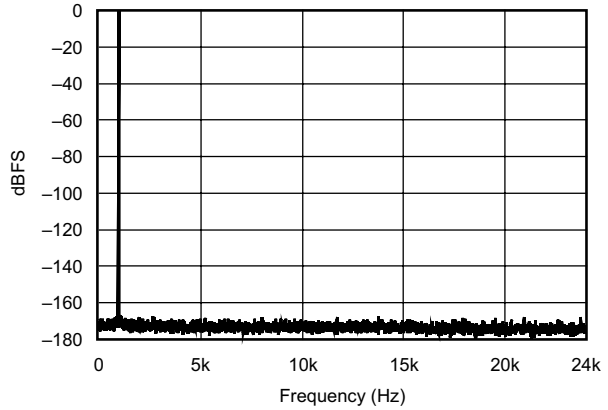


Figure 2. FFT With 1-kHz Input Tone at –60 dBFS

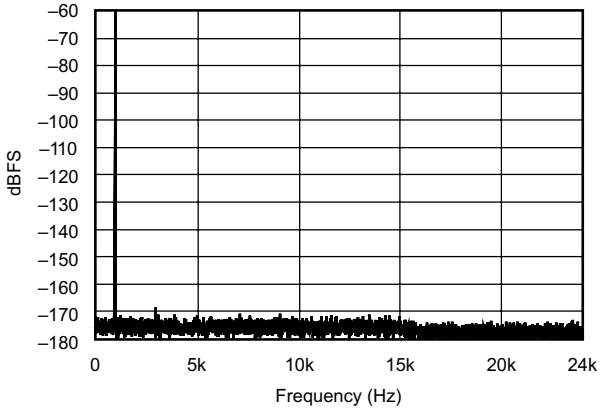
Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.



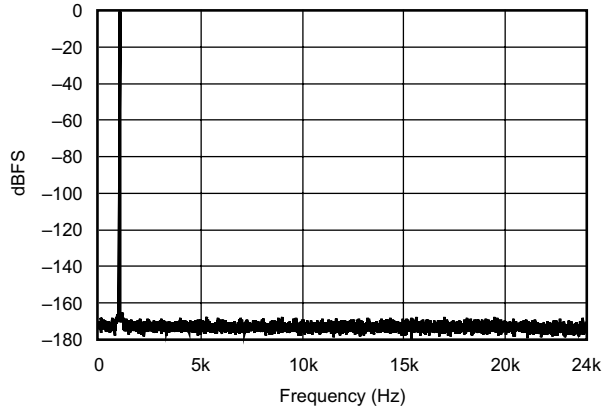
32 kHz:48 kHz

Figure 3. FFT With 1-kHz Input Tone at 0 dBFS



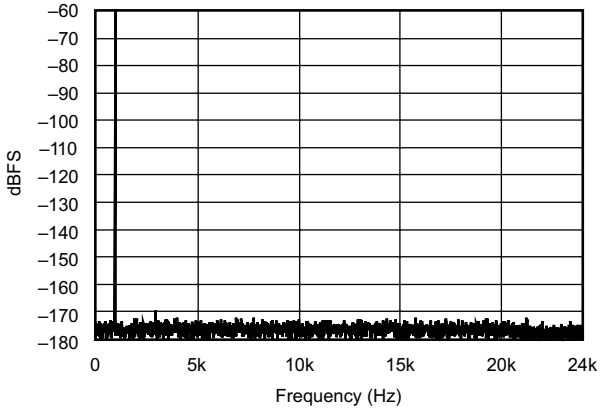
32 kHz:48 kHz

Figure 4. FFT With 1-kHz Input Tone at –60 dBFS



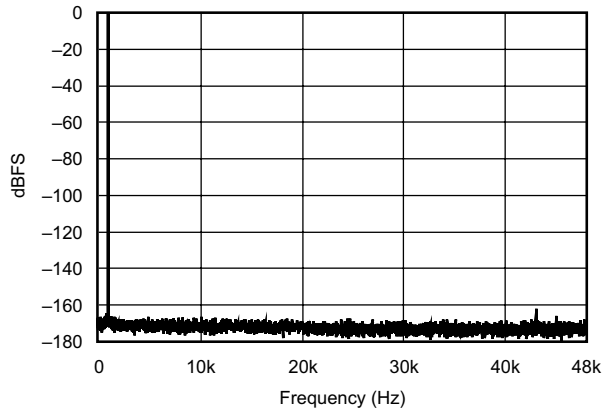
44.1 kHz:48 kHz

Figure 5. FFT With 1-kHz Input Tone at 0 dBFS



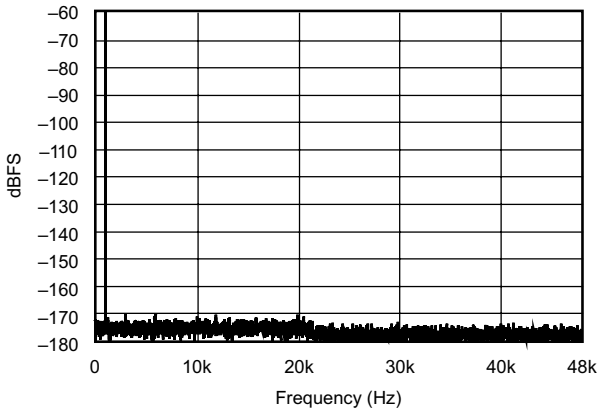
44.1 kHz:48 kHz

Figure 6. FFT With 1-kHz Input Tone at –60 dBFS



44.1 kHz:96 kHz

Figure 7. FFT With 1-kHz Input Tone at 0 dBFS

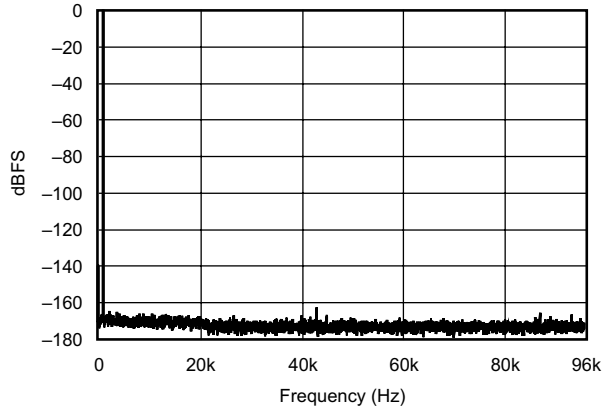


44.1 kHz:96 kHz

Figure 8. FFT With 1-kHz Input Tone at –60 dBFS

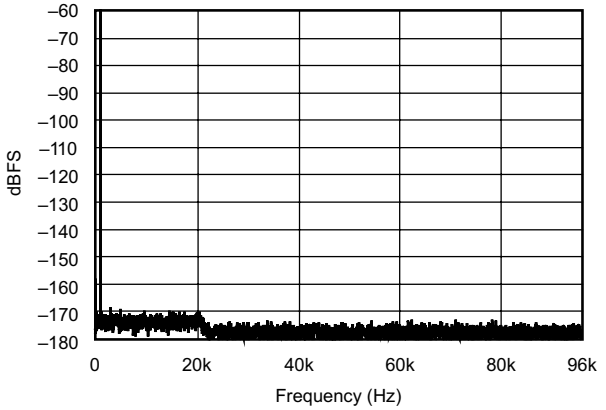
Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.



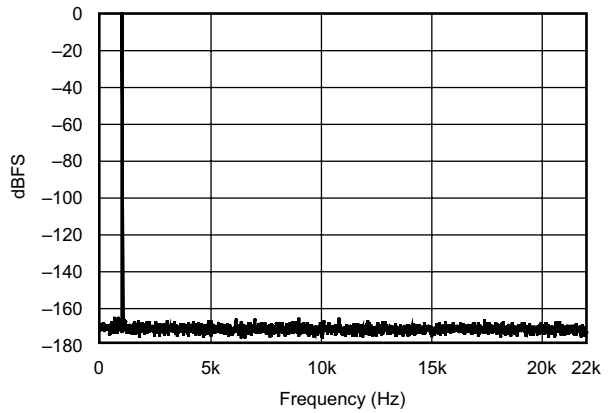
44.1 kHz:192 kHz

Figure 9. FFT With 1-kHz Input Tone at 0 dBFS



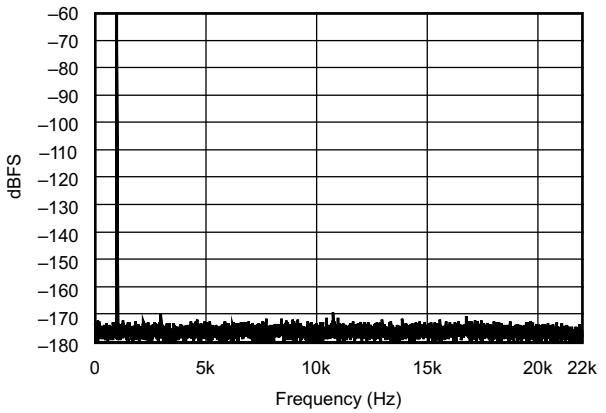
44.1 kHz:192 kHz

Figure 10. FFT With 1-kHz Input Tone at –60 dBFS



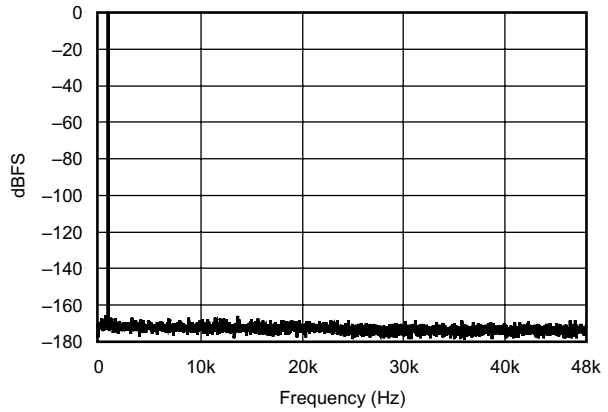
48 kHz:44.1 kHz

Figure 11. FFT With 1-kHz Input Tone at 0 dBFS



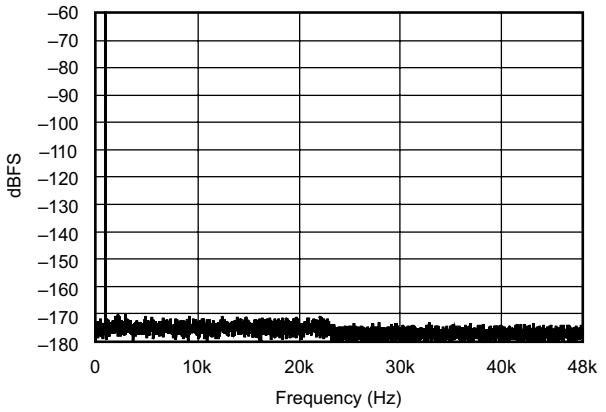
48 kHz:44.1 kHz

Figure 12. FFT With 1-kHz Input Tone at –60 dBFS



48 kHz:96 kHz

Figure 13. FFT With 1-kHz Input Tone at 0 dBFS

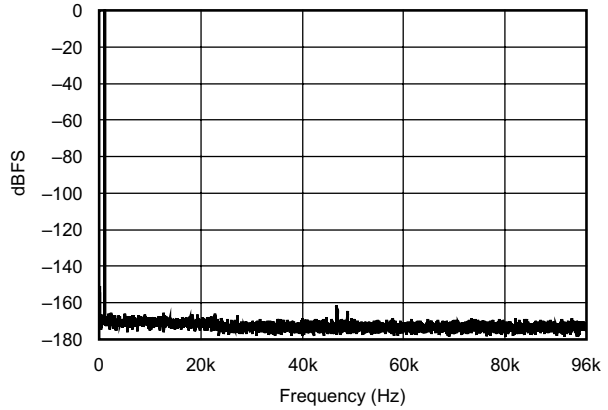


48 kHz:96 kHz

Figure 14. FFT With 1-kHz Input Tone at –60 dBFS

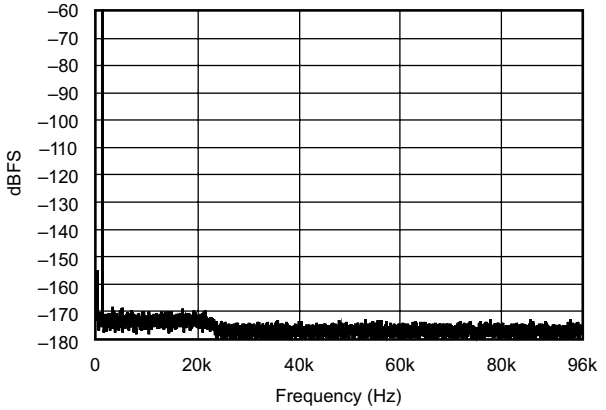
Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.



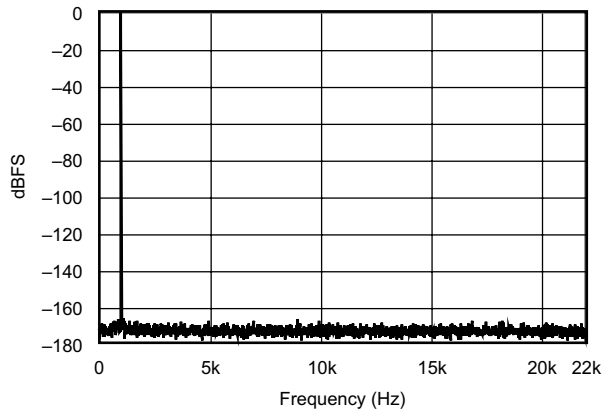
48 kHz:192 kHz

Figure 15. FFT With 1-kHz Input Tone at 0 dBFS



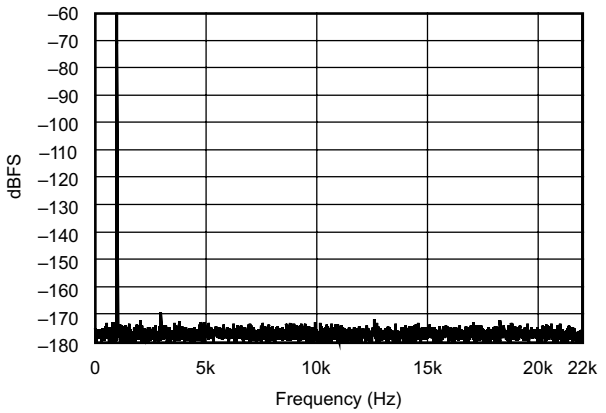
48 kHz:192 kHz

Figure 16. FFT With 1-kHz Input Tone at –60 dBFS



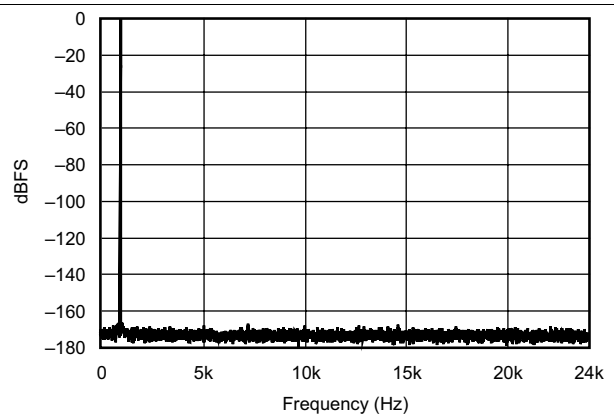
96 kHz:44.1 kHz

Figure 17. FFT With 1-kHz Input Tone at 0 dBFS



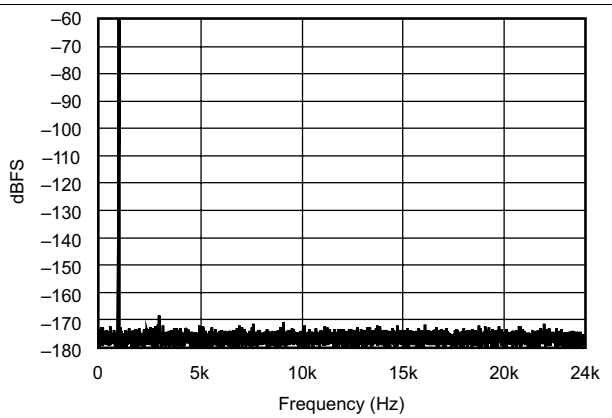
96 kHz:44.1 kHz

Figure 18. FFT With 1-kHz Input Tone at –60 dBFS



96 kHz:48 kHz

Figure 19. FFT With 1-kHz Input Tone at 0 dBFS

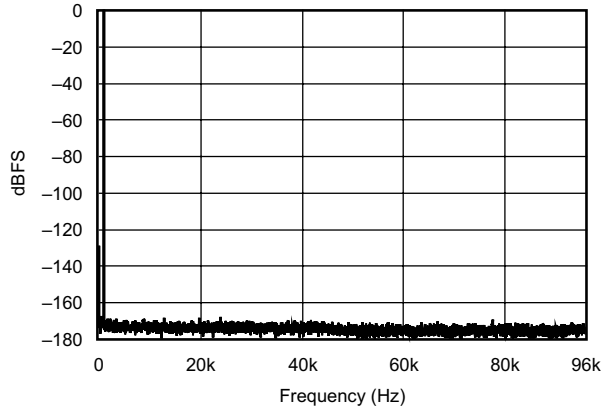


96 kHz:48 kHz

Figure 20. FFT With 1-kHz Input Tone at –60 dBFS

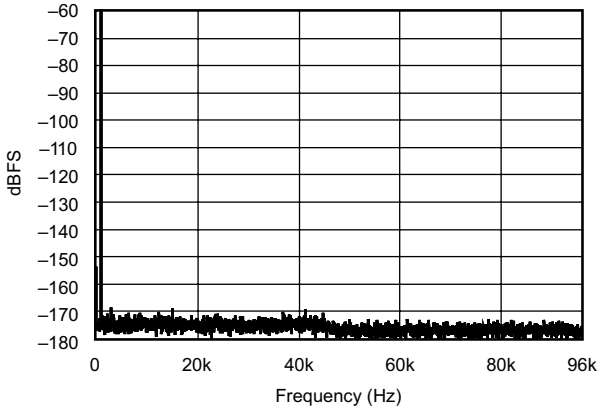
Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.



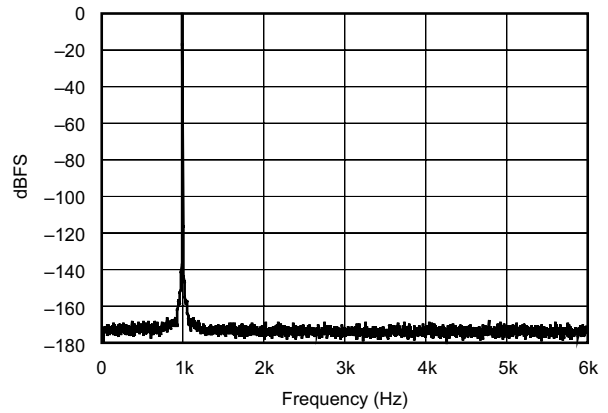
96 kHz:192 kHz

Figure 21. FFT With 1-kHz Input Tone at 0 dBFS



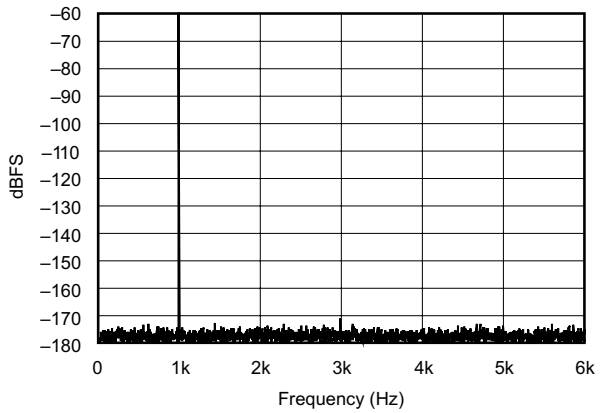
96 kHz:192 kHz

Figure 22. FFT With 1-kHz Input Tone at –60 dBFS



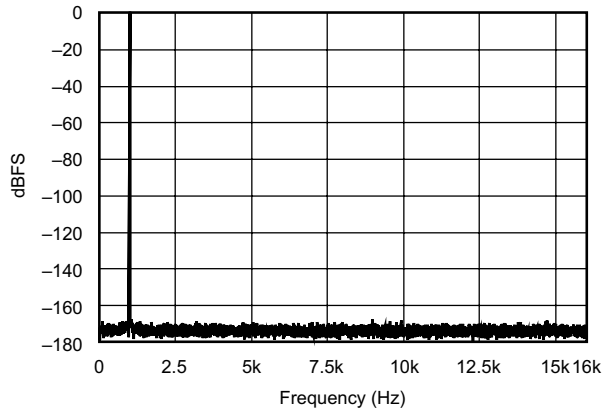
192 kHz:12 kHz

Figure 23. FFT With 1-kHz Input Tone at 0 dBFS



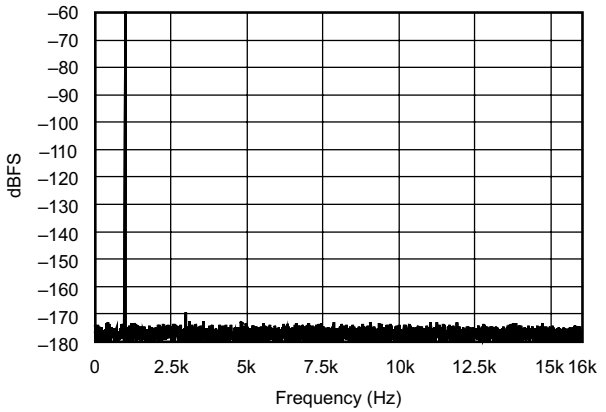
192 kHz:12 kHz

Figure 24. FFT With 1-kHz Input Tone at –60 dBFS



192 kHz:32 kHz

Figure 25. FFT With 1-kHz Input Tone at 0 dBFS

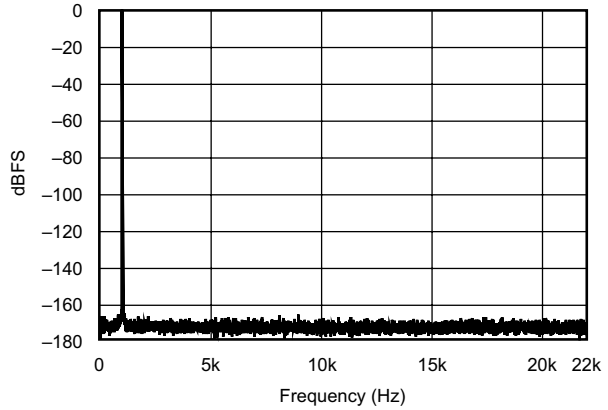


192 kHz:32 kHz

Figure 26. FFT With 1-kHz Input Tone at –60 dBFS

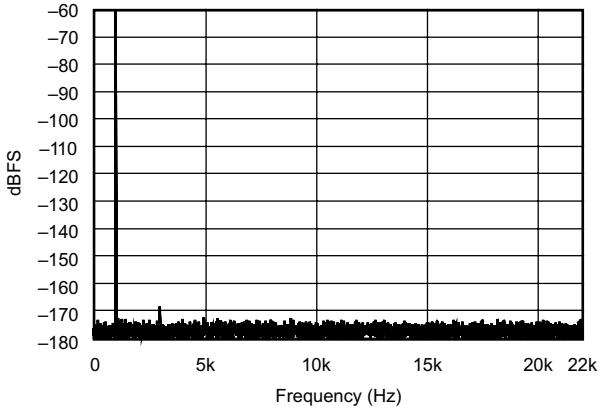
Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.



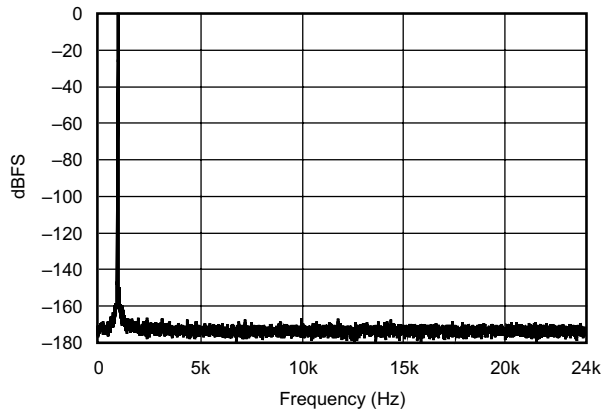
192 kHz:44.1 kHz

Figure 27. FFT With 1-kHz Input Tone at 0 dBFS



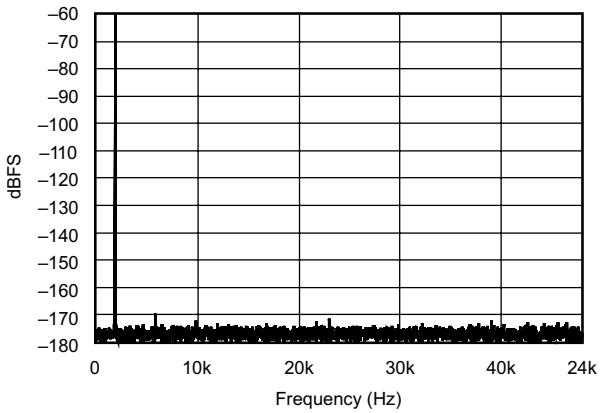
192 kHz:44.1 kHz

Figure 28. FFT With 1-kHz Input Tone at –60 dBFS



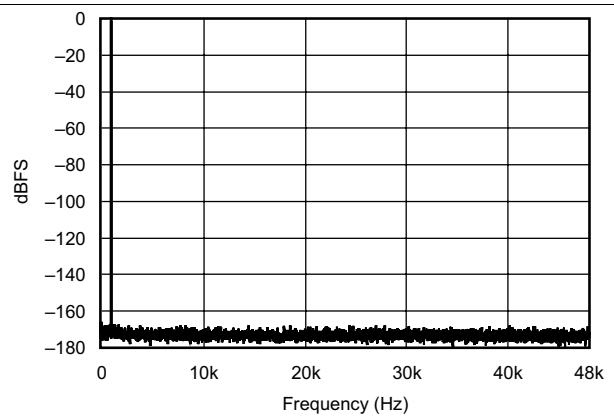
192 kHz:48 kHz

Figure 29. FFT With 1-kHz Input Tone at 0 dBFS



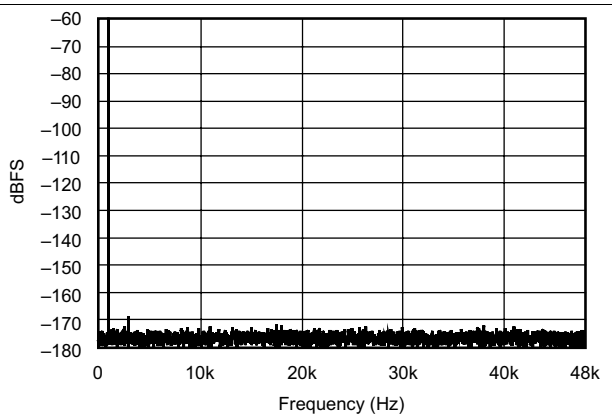
192 kHz:48 kHz

Figure 30. FFT With 1-kHz Input Tone at –60 dBFS



192 kHz:96 kHz

Figure 31. FFT With 1-kHz Input Tone at 0 dBFS

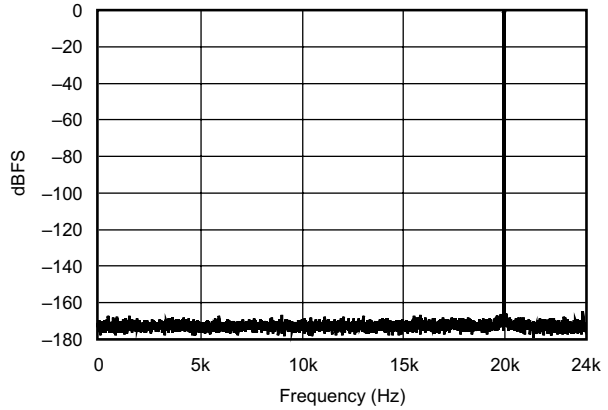


192 kHz:96 kHz

Figure 32. FFT With 1-kHz Input Tone at –60 dBFS

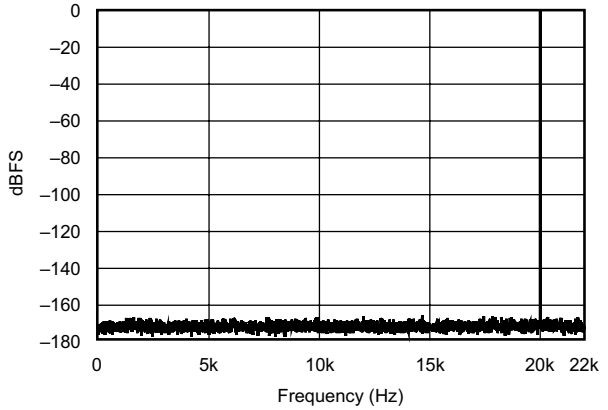
Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.



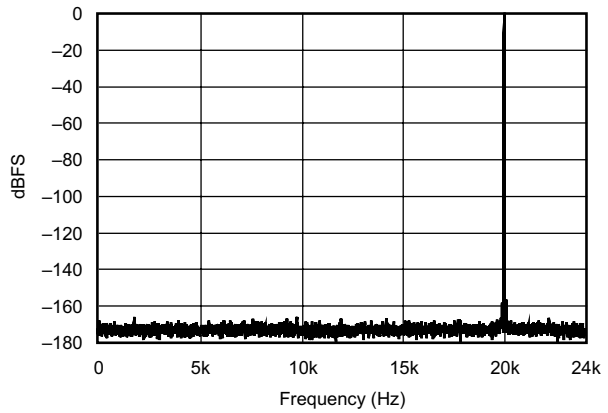
44.1 kHz:48 kHz

Figure 33. FFT With 20-kHz Input Tone at 0 dBFS



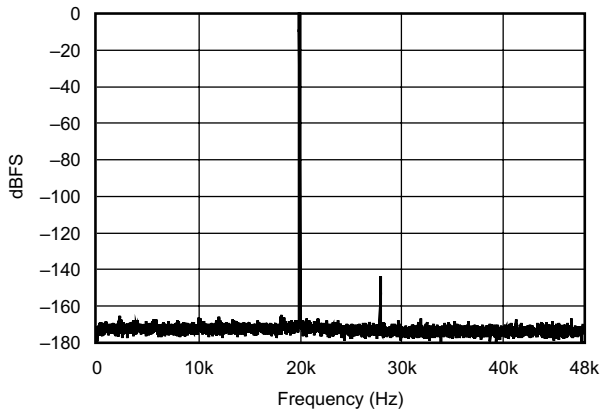
48 kHz:44.1 kHz

Figure 34. FFT With 20-kHz Input Tone at 0 dBFS



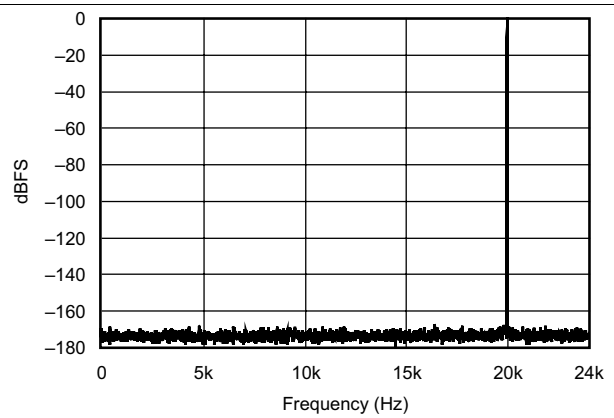
48 kHz:48 kHz

Figure 35. FFT With 20-kHz Input Tone at 0 dBFS



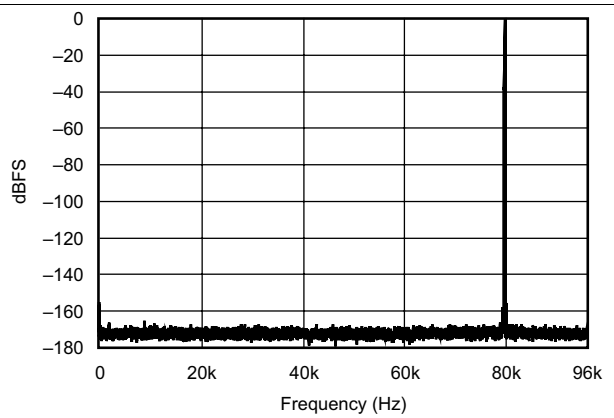
48 kHz:96 kHz

Figure 36. FFT With 20-kHz Input Tone at 0 dBFS



96 kHz:48 kHz

Figure 37. FFT With 20-kHz Input Tone at 0 dBFS

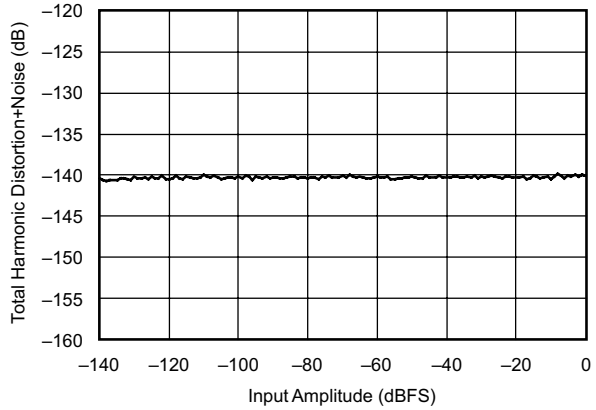


192 kHz:192 kHz

Figure 38. FFT With 80-kHz Input Tone at 0 dBFS

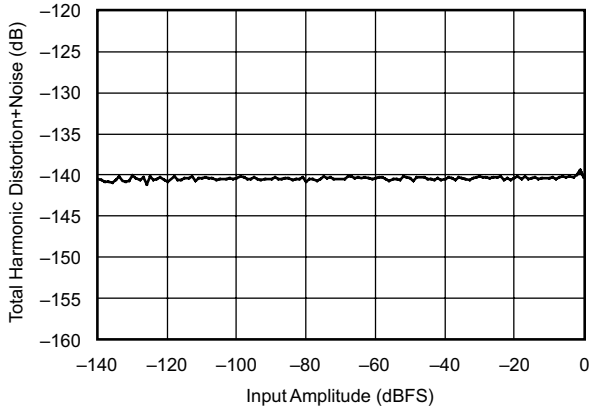
Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.



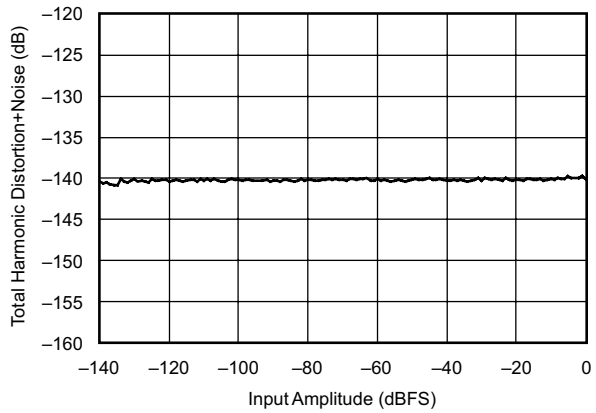
44.1 kHz:48 kHz

Figure 39. THD+N vs Input Amplitude f_{IN} = 1 kHz



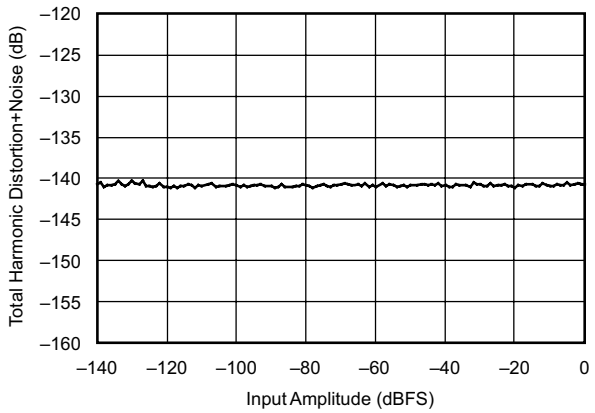
48 kHz:44.1 kHz

Figure 40. THD+N vs Input Amplitude f_{IN} = 1 kHz



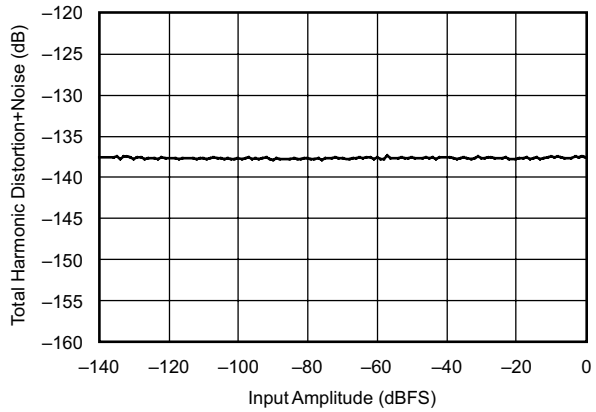
48 kHz:96 kHz

Figure 41. THD+N vs Input Amplitude f_{IN} = 1 kHz



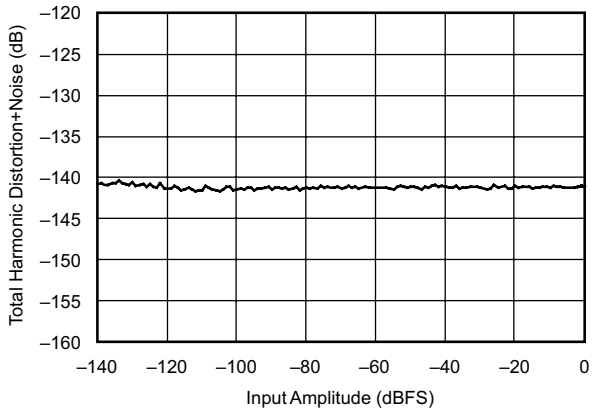
96 kHz:48 kHz

Figure 42. THD+N vs Input Amplitude f_{IN} = 1 kHz



44.1 kHz:192 kHz

Figure 43. THD+N vs Input Amplitude f_{IN} = 1 kHz

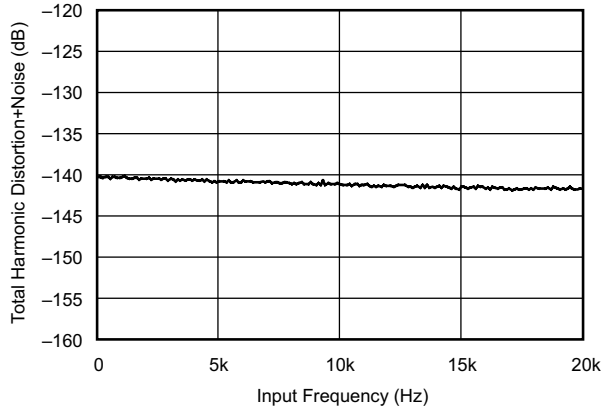


192 kHz:48 kHz

Figure 44. THD+N vs Input Amplitude f_{IN} = 1 kHz

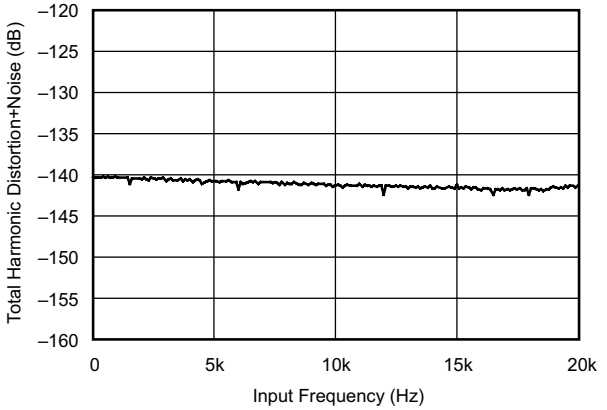
Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.



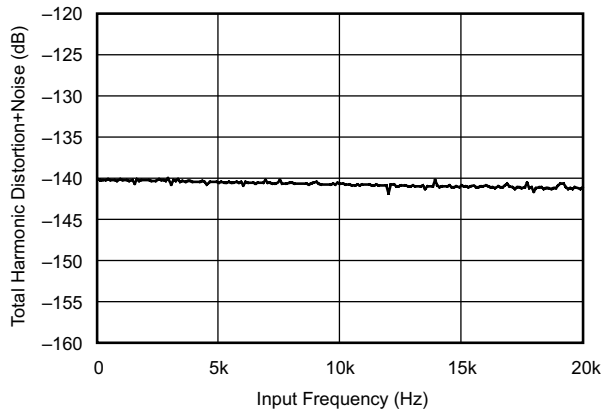
44.1 kHz:48 kHz

Figure 45. THD+N vs Input Frequency, 0-dBFS Input



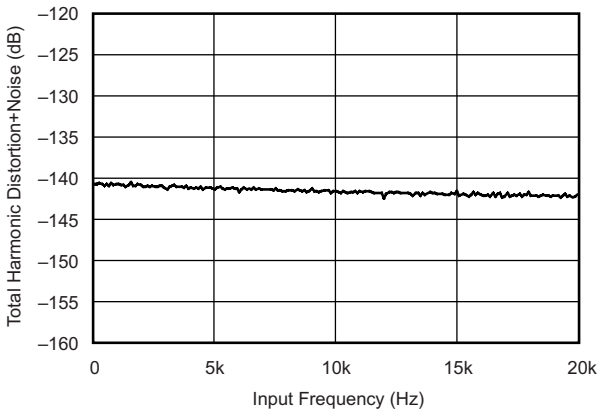
48 kHz:44.1 kHz

Figure 46. THD+N vs Input Frequency, 0-dBFS Input



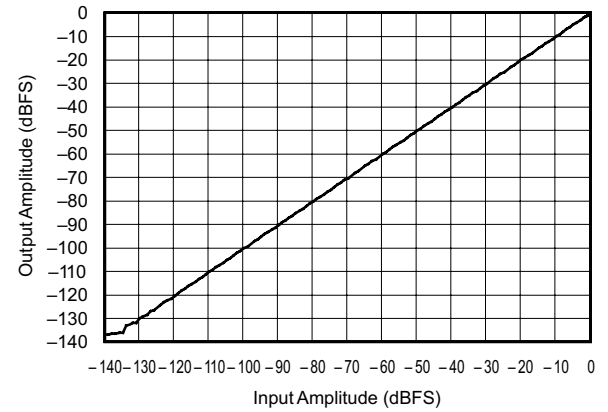
48 kHz:96 kHz

Figure 47. THD+N vs Input Frequency, 0-dBFS Input



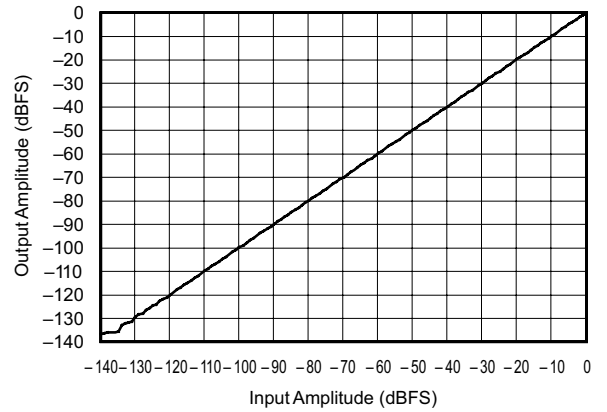
96 kHz:48 kHz

Figure 48. THD+N vs Input Frequency, 0-dBFS Input



44.1 kHz:48 kHz

Figure 49. Linearity With f_{IN} = 200 Hz

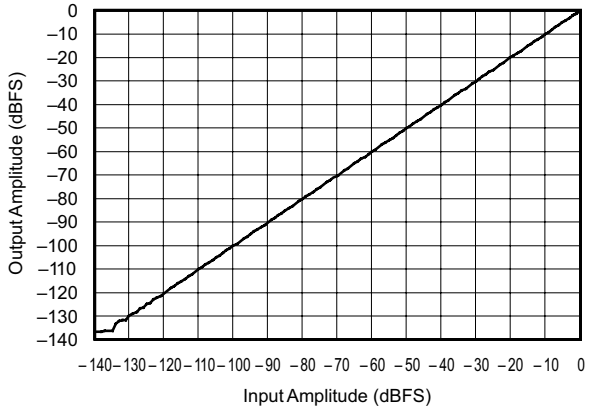


48 kHz:44.1 kHz

Figure 50. Linearity With f_{IN} = 200 Hz

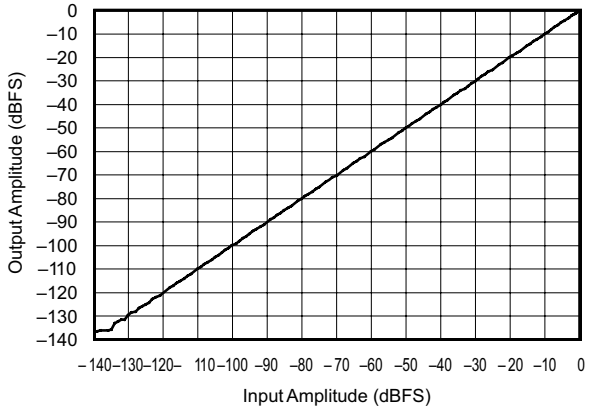
Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.



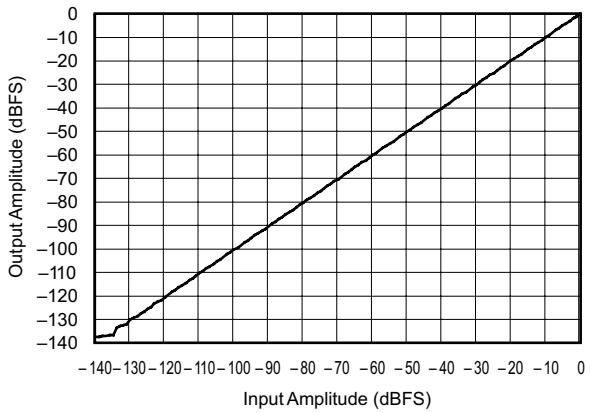
48 kHz:48 kHz

Figure 51. Linearity With f_{IN} = 200 Hz



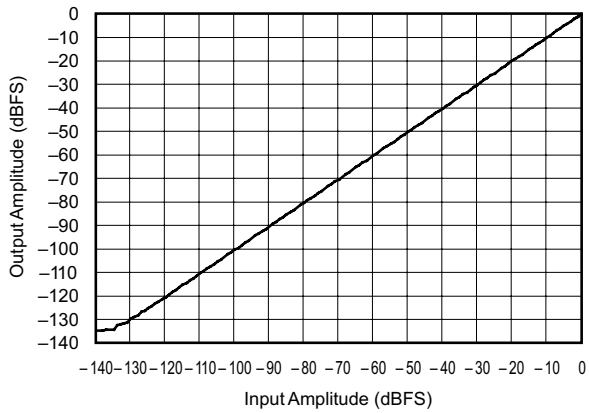
48 kHz:96 kHz

Figure 52. Linearity With f_{IN} = 200 Hz



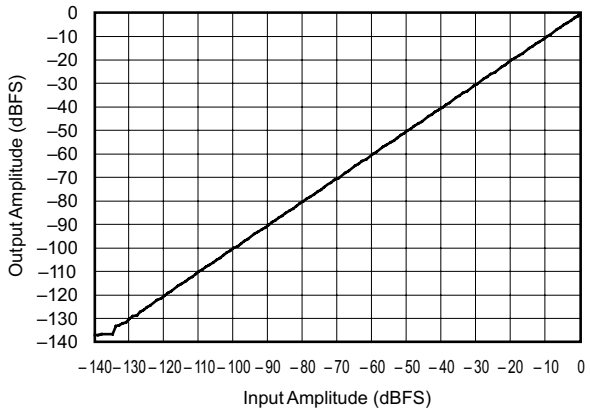
96 kHz:48 kHz

Figure 53. Linearity With f_{IN} = 200 Hz



44.1 kHz:192 kHz

Figure 54. Linearity With f_{IN} = 200 Hz



192 kHz:44.1 kHz

Figure 55. Linearity With f_{IN} = 200 Hz

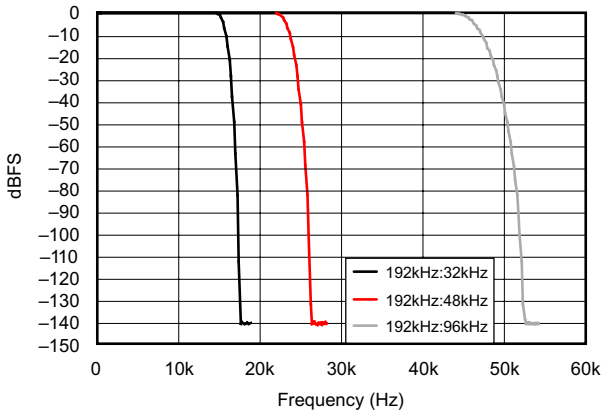


Figure 56. Frequency Response With 0-dBFS Input

Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, and V_{IO} = 3.3 V, unless otherwise noted.

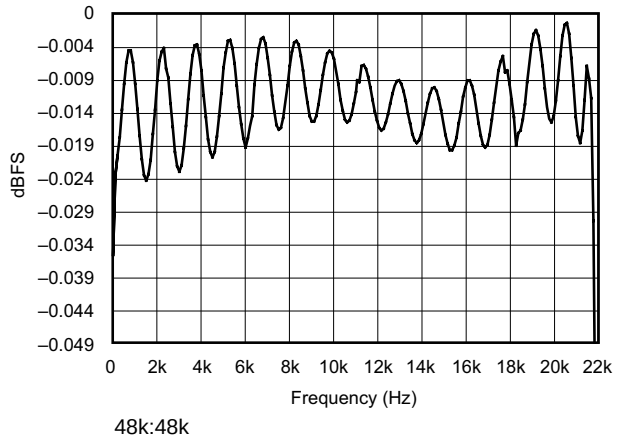


Figure 57. Pass Band Ripple

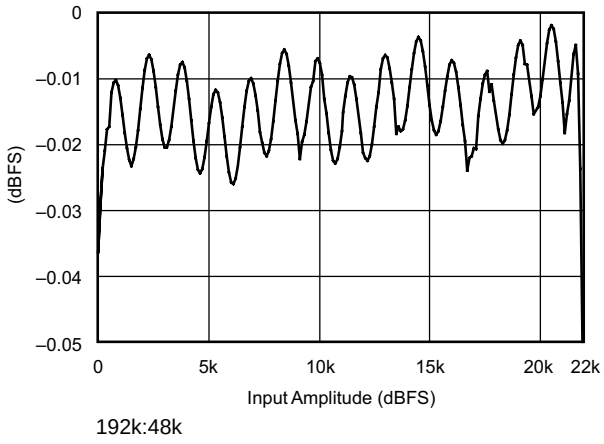


Figure 58. Pass Band Ripple

7 Detailed Description

7.1 Overview

The SRC4192 and SRC4193 devices are asynchronous, sample-rate converters (ASRC) designed for professional audio applications. Operation at input and output sampling frequencies up to 212 kHz is supported, with an input and output sampling ratio range of 16:1 to 1:16. Excellent dynamic range and Total Harmonic Distortion + Noise (THD+N) are achieved by employing high-performance, linear-phase digital filtering with image rejection better than 140 dB. Digital filtering options allow for lower group-delay processing. These include a low group-delay option for the interpolation and resampler function, as well as a direct down-sampling option for the decimation function (SRC4193 device only).

The audio input and output ports support standard audio data formats, as well as a TDM interface mode. Word lengths of 24-, 20-, 18-, and 16-bits are supported. Both ports may operate in slave mode, deriving their word and bit clocks from external input and output devices. Alternatively, one port may operate in master mode while the other remains in slave mode. In master mode, the LRCK and BCK clocks are derived from the reference clock input, RCKI. The flexible configuration of the input and output ports allows connection to a wide variety of audio data converters, interface devices, digital signal processors, and programmable logic.

A bypass mode is included, which allows audio data to be passed directly from the input port to the output port, bypassing the ASRC function. The bypass option is useful for passing through encoded or compressed audio data, or nonaudio control or status data.

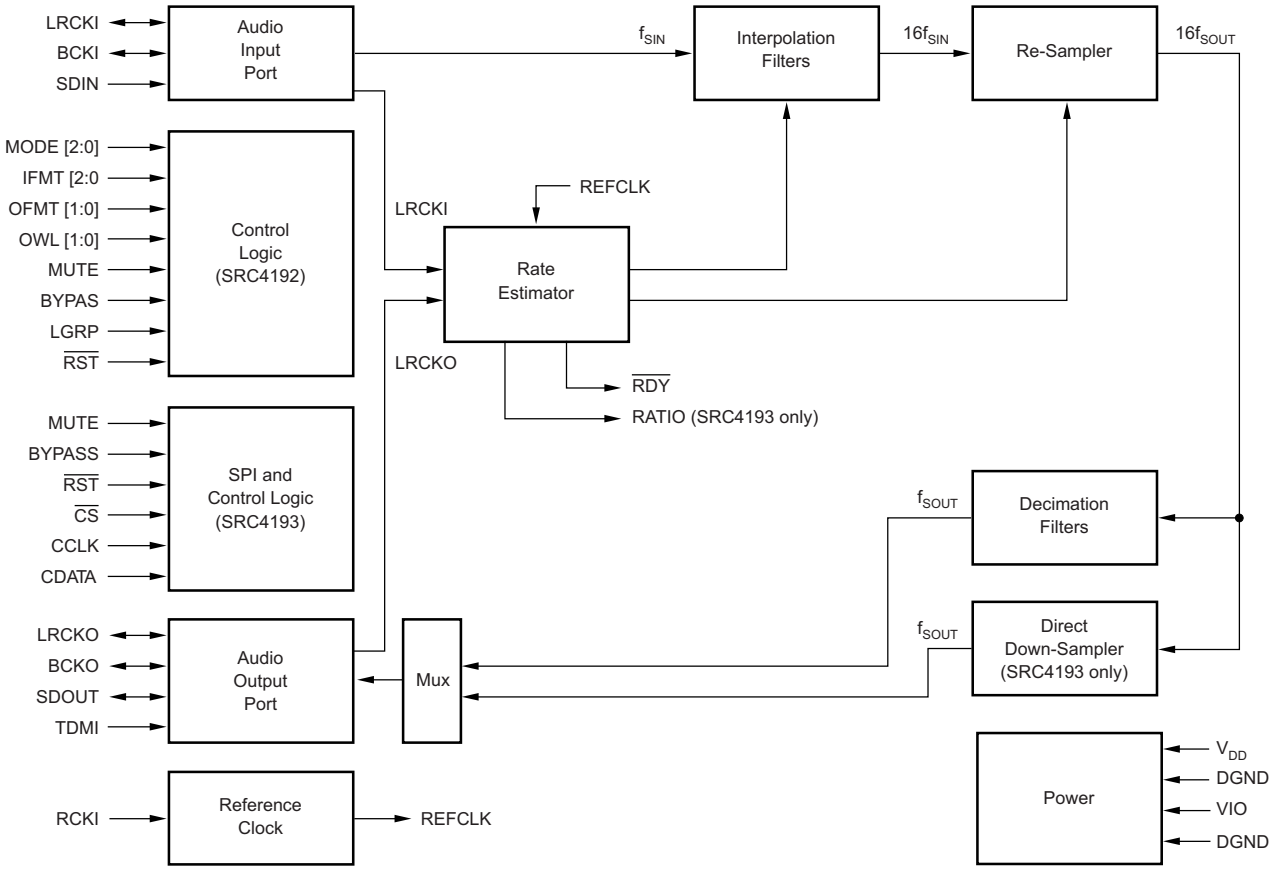
A soft mute function is available on both the SRC4192 and SRC4193 devices. Digital output attenuation is available only for the SRC4193 device. Both soft mute and digital attenuation functions provide artifact-free operation, while allowing muting or level adjustment of the audio output signal. The mute attenuation is typically –144 dB, while the digital attenuation control is adjustable from 0 dB to –127.5 dB in 0.5-dB steps.

The SRC4193 device includes a three-wire SPI port to access on-chip control registers for configuration of internal functions. The port can be easily interfaced to microprocessors or digital signal processors with synchronous serial port peripherals.

Functional Block Diagram shows a functional block diagram of the SRC4192 and SRC4193 devices. Audio data is received at the input port, clocked by either the audio data source in slave mode, or by the SRC419x in master mode. The output-port data is clocked by either the audio data source in slave mode, or by the SRC419x in master mode. The input data is passed through interpolation filters which up-sample the data, which is then passed on to the resampler. The rate estimator compares the input and output sampling frequencies by comparing LRCKI, LRCKO, and a reference clock. The results include an offset for the FIFO pointer and the coefficients needed for re-sampling function.

The output of the resampler is passed on to either the decimation filter or direct down-sampler function. The decimation filter performs down-sampling and anti-alias filtering functions, and is required when the output sampling frequency is lower than the input-sampling frequency. The direct down-sampler function does not provide any filtering, and may be used in cases when aliasing is not an issue. This includes the case when the output sampling frequency is equal to or greater than the input sampling frequency. The advantage of direct down-sampling is a significant reduction in the group delay associated with the decimation filter, allowing lower latency sample rate conversion. The direct down-sampler function is available only for the SRC4193 device.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Port Operation

The audio input port is a three-wire synchronous serial interface that can operate in either slave or master mode. The SDIN input (pin 4) is the serial audio data input. Audio data is input at this pin in one of three standard audio data formats: Philips I^2S, Left-Justified, or Right-Justified. The audio data word length may be up to 24-bits for I^2S and Left-Justified formats, while the Right-Justified format supports 16-, 18-, 20-, or 24-bit data. The data formats are shown in Figure 59, while critical timing parameters are shown in Figure 60 and listed in *Electrical Characteristics*.

Feature Description (continued)

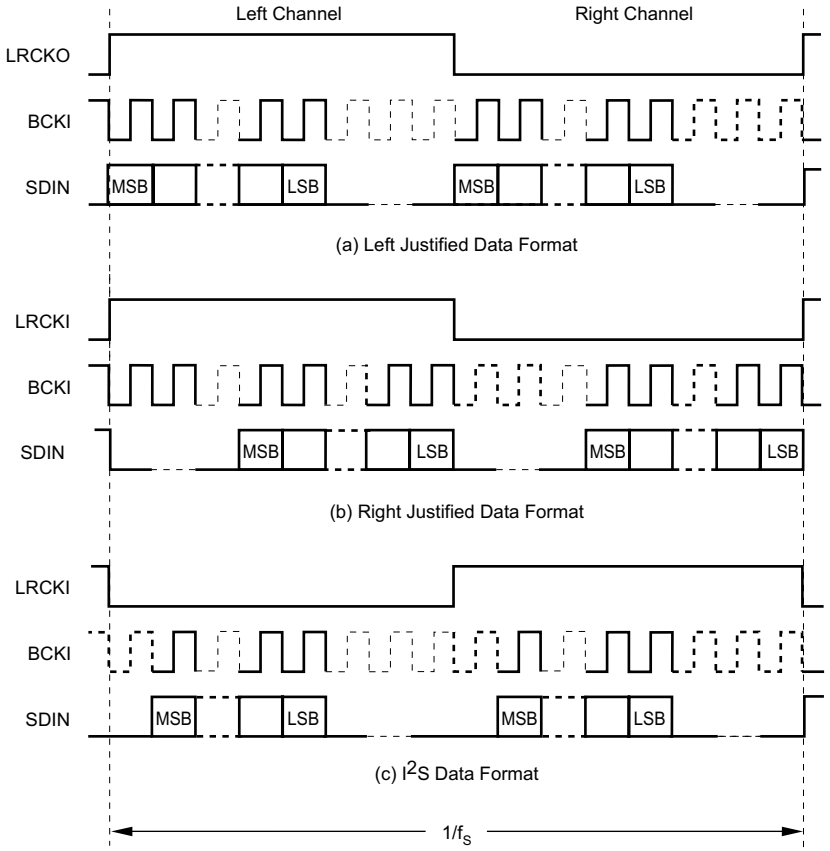


Figure 59. Input Data Formats

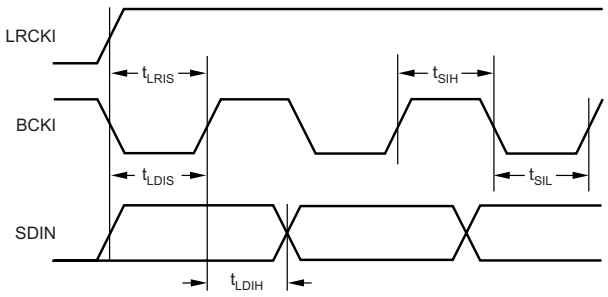


Figure 60. Input Port Timing

The bit clock is either an input or output at BCKI (pin 5). In slave mode, BCKI is configured as an input pin, and may operate at rates from $32f_S$ to $128f_S$,with a minimum of one clock cycle per data bit. In master mode, BCKI operates at a fixed rate of $64f_S$.

The left/right word clock, LRCKI (pin 6), may be configured as an input or output pin. In slave mode, LRCKI is an input pin, while in master mode LRCKI is an output pin. In either case, the clock rate is equal to f_S, the input sampling frequency. The LRCKI duty cycle is fixed to 50% for master mode operation.

Table 1 shows data format selection for the input port. For the SRC4192, the IFMT0 (pin 10), IFMT1 (pin 11), and IFMT2 (pin 12) inputs are used to set the input port data format. For the SRC4193, the IFMT[2:0] bits in Control Register 3 are used to select the data format.

Feature Description (continued)

Table 1. Input Port Data Format Selection

IFMT2	IFMT1	IFMT0	INPUT PORT DATA FORMAT
0	0	0	24-Bit Left Justified
0	0	1	24-Bit I^2S
0	1	0	Unused
0	1	1	Unused
1	0	0	16-Bit Right Justified
1	0	1	18-Bit Right Justified
1	1	0	20-Bit Right Justified
1	1	1	24-Bit Right Justified

7.3.2 Output Port Operation

The audio output port is a four-wire synchronous serial interface that can operate in either Slave or Master mode. The SDOUT output (pin 23) is the serial audio data output. Audio data is output at this pin in one of four data formats: Philips I^2S, Left-Justified, Right-Justified, or TDM. The audio data word length may be 16-, 18-, 20-, or 24-bits. For all word lengths, the data is triangular PDF dithered from the internal 28-bit data path. The data formats (with the exception of TDM mode) are shown in Figure 61, while critical timing parameters are shown in Figure 62 and listed in *Electrical Characteristics*. The TDM format and timing are shown in Figure 72 and Figure 73, respectively, while examples of standard TDM configurations are shown in Figure 74 and Figure 75

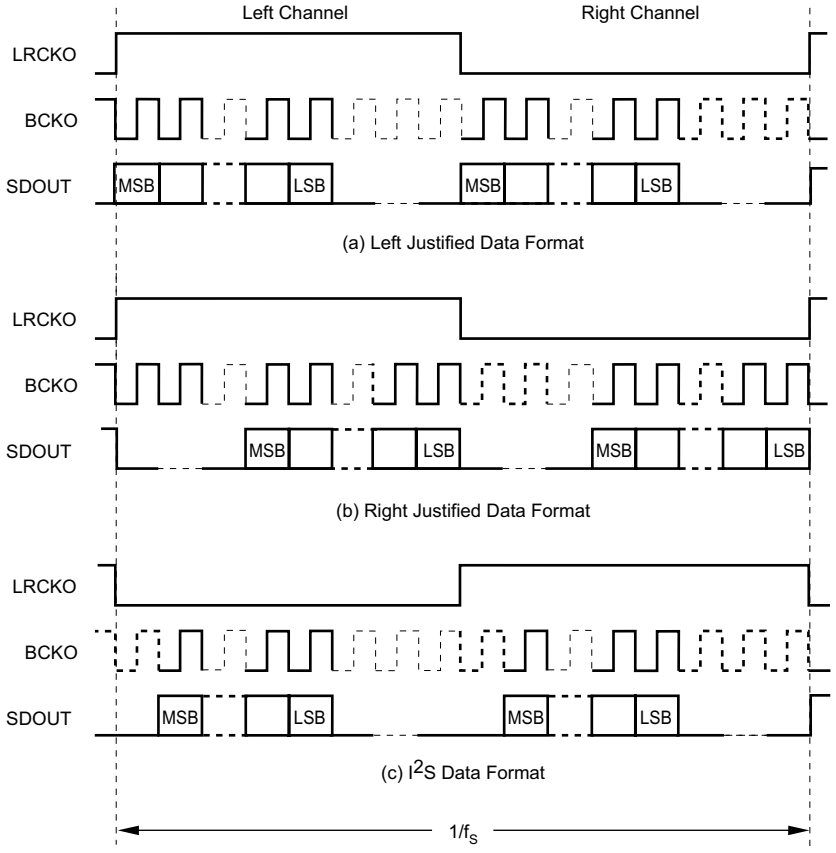


Figure 61. Output Data Formats

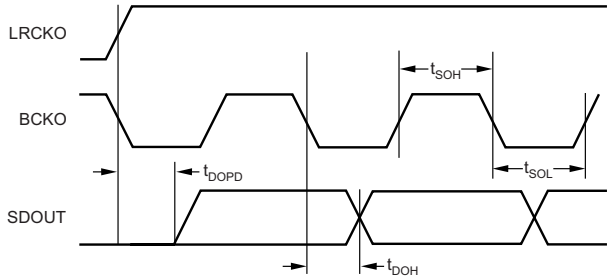


Figure 62. Output Port Timing

The bit clock is either input or output at BCKO (pin 25). In Slave mode, BCKO is configured as an input pin, and can operate at rates from $32f_S$ to $128f_S$, with a minimum of one clock cycle for each data bit. The exception is the TDM mode, where the BCKO must operate at $N \times 64f_S$, where N is equal to the number of SRC4192 or SRC4193 devices included on the TDM interface. In master mode, BCKO operates at a fixed rate of $64f_S$ for all data formats except TDM, where BCKO operates at the reference clock (RCKI) frequency. Additional information regarding TDM mode operation is included in *Application and Implementation*.

The left/right word clock, LRCKO (pin 24), can be configured as an input or output pin. In slave mode, LRCKO is an input pin, while in master mode it is an output pin. In either case, the clock rate is equal to f_S, the output sampling frequency. The clock duty cycle is fixed to 50% for I^2S, Left-Justified, and Right-Justified formats in master mode. The LRCKO pulse width is fixed to 32 BCKO cycles for the TDM format in master mode.

Table 2 illustrates data format selection for the output port. For the SRC4192, the OFMT0 (pin 19), OFMT1 (pin 18), OWL0 (pin 17), and OWL1 (pin 16) inputs are used to set the output port data format and word length. For the SRC4193, the OFMT[1:0] and OWL[1:0] bits in Control Register 3 are used to select the data format and word length.

Table 2. Output Port Data Format Selection

OFMT1	OFMT0	OUTPUT PORT DATA FORMAT
0	0	Left-Justified
0	1	I^2S
1	0	TDM
1	1	Right-Justified
OWL1	**OWL0**	**OUTPUT PORT DATA WORD LENGTH**
0	0	24-Bits
0	1	20-Bits
1	0	18-Bits
1	1	16-Bits

7.3.3 Soft Mute Function

The soft mute function of the SRC419x device is invoked by forcing the MUTE input (pin 14) high. For the SRC4193 device, the mute function may also be accessed using the MUTE bit in Control Register 1. The soft mute function slowly attenuates the output signal level down to all zeroes plus ±1LSB of dither. This provides an artifact-free muting of the audio output port.

7.3.4 Digital Attenuation (SRC4193 Only)

The SRC4193 device includes independent digital attenuation for the left and right audio channels. The attenuation ranges from 0 dB (or unity) to –127.5 dB in 0.5-dB steps. The attenuation settings are programmed using Control Registers 4 and 5, corresponding to the left and right channels, respectively.

The TRACK bit in Control Register 1 selects independent or tracking attenuation modes. When TRACK = 0, the left and right channels are controlled independently. When TRACK = 1, the attenuation setting for the left channel is also used for the right channel, and the right channel is said to track the left channel attenuation setting.

7.3.5 Ready Output

The SRC419x device includes an active low ready output named $\overline{\text{RDY}}$ (pin 15). This is an output from the rate estimator block, which indicates that the input-to-output sampling frequency ratio has been determined. The ready signal can be used as a flag or indicator output. The ready signal can also be connected to the active high MUTE input (pin 14) to provide an auto-mute function, so that the output port is muted when the rate estimator is in transition.

7.3.6 Ratio Output (SRC4193 Only)

The SRC4193 device includes a simple ratio flag output named RATIO (pin 16). When RATIO is low, it indicates that the output sampling frequency is lower than the input sampling frequency. When RATIO is high, it indicates that the output sampling frequency is higher than the input sampling frequency. The ratio output can be used as an indicator or flag output for an LED or host device.

7.3.7 Serial Peripheral Interface (SPI) Port: SRC4193 Only

The SPI port is a three-wire synchronous serial interface used to access the on-chip control registers of the SRC4193 device. The interface is comprised of a serial data clock input, CCLK (pin 27), a serial data input, CDATA (pin 28), and an active low chip-select input, $\overline{\text{CS}}$ (pin 26). Figure 63 shows the protocol for writing control registers using the serial control port. Figure 64 shows the critical timing parameters for the SPI port interface, which are also listed in *Electrical Characteristics*.

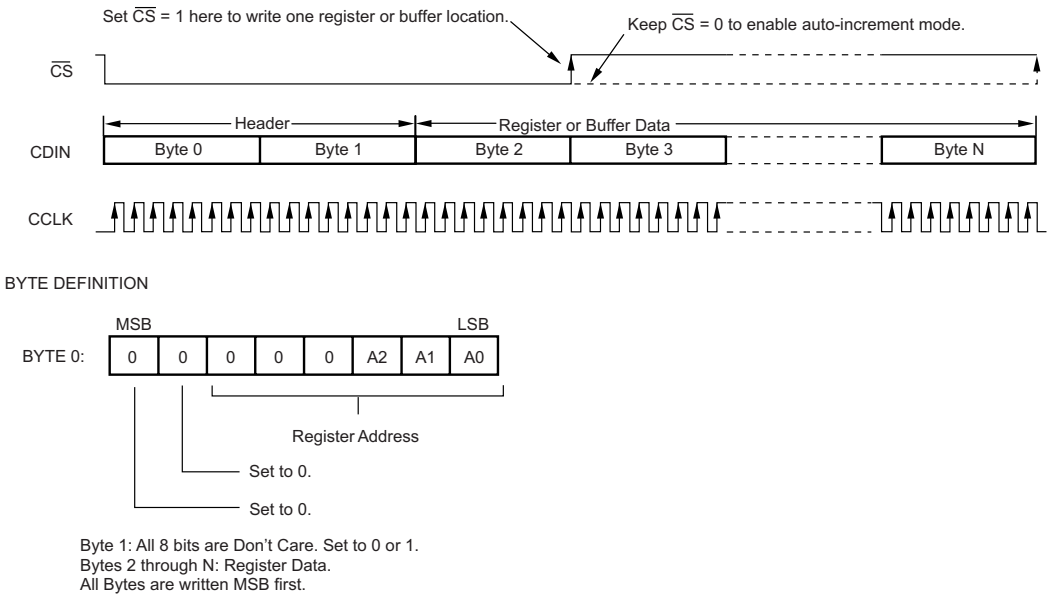


Figure 63. SPI Port Protocol

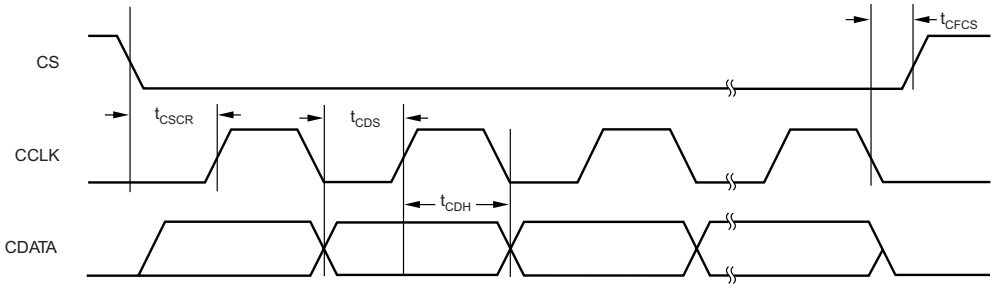


Figure 64. SPI Port Timing

Byte 0 indicates the address of the control register to be written. The two most significant bits are set to 0, while the six least significant bits contain the control register address. Byte 1 is a don't care byte. This byte is included in the protocol to maintain compatibility with current and future Texas Instruments digital audio products, including the DIT4096 and DIT4192 digital audio transmitters. Byte 2 contains the 8-bit data for the control register addressed in Byte 0.

As shown in Figure 63, a write sequence starts by bringing the $\overline{CS}$ input low. Bytes 0, 1, and 2 are then written to program a single control register. Bringing the $\overline{CS}$ input high after the third byte will write just one register. However, if $\overline{CS}$ remains low after writing the first control byte, the port will autoincrement the address by 1, allowing successive addresses to be written. The address is automatically incremented by 1 after each byte is written, as long as the $\overline{CS}$ input remains low. This is referred to as auto-increment operation, and is always enabled for the SPI port.

7.4 Device Functional Modes

7.4.1 Reset and Power Down Operation

The SRC419x device can be reset using the $\overline{RST}$ input (pin 13). There is no internal power-on reset, so the user should force a reset sequence after power up to initialize the device. To force a reset, the reference clock input must be active, with an external clock source supplying a valid reference clock signal (refer to Figure 80). The user must assert $\overline{RST}$ low for a minimum of 500 ns, and then bring $\overline{RST}$ high again to force a reset. Figure 65 shows the reset timing for the SRC419x device.

For the SRC4193, there is an additional 500 µs delay after the $\overline{RST}$ rising edge, due to internal logic requirements. The customer should wait at least 500 µs after the $\overline{RST}$ rising edge before attempting to write to the SPI port of the SRC4193 device.

The SRC419x device also supports a power-down mode. Power-down mode may be set by either holding the $\overline{RST}$ input low (SRC4192 and SRC4193 devices), or by setting the PDN bit in Control Register 1 to zero (SRC4193 device only). The SRC4193 device will be in power-down mode by default after an external reset has been issued. To enable normal operation for the SRC4193, disable power down mode by writing a 1 to the PDN bit in Control Register 1.

When using the PDN bit in Control Register 1 to enable power-down mode for the SRC4193, the current state of the control registers is maintained through the power-down and power-up transition.

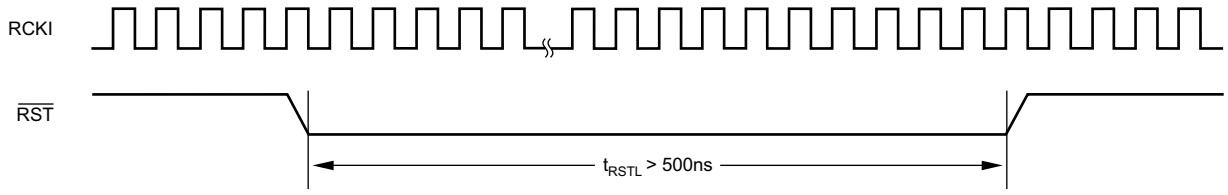


Figure 65. Reset Pulse Width Requirement

7.4.2 Audio Port Modes

The SRC4192 and SRC4193 devices both support seven serial-port modes, shown in Table 3. For the SRC4192 device, the audio port mode is selected using the MODE0 (pin 26), MODE1 (pin 27), and MODE2 (pin 28) inputs. For the SRC4193 device, the mode is selected using the MODE[2:0] bits in Control Register 1. The default mode setting for the SRC4193 device is both input and output ports set to slave mode.

In slave mode, the port LRCK and BCK clocks are configured as inputs, and receive their clocks from an external audio device. In master mode, the LRCK and BCK clocks are configured as outputs, being derived from the reference clock input (RCKI). Only one port can be set to master mode at any given time, as indicated in Table 3.

Table 3. Setting the Serial Port Modes

MODE2	MODE1	MODE0	SERIAL PORT MODE
0	0	0	Both Input and Output Ports are Slave mode
0	0	1	Output Port is Master mode with RCKI = 128 f_S
0	1	0	Output Port is Master mode with RCKI = 512 f_S

Device Functional Modes (continued)

Table 3. Setting the Serial Port Modes (continued)

MODE2	MODE1	MODE0	SERIAL PORT MODE
0	1	1	Output Port is Master mode with RCKI = 256 f_S
1	0	0	Both Input and Output Ports are Slave mode
1	0	1	Input Port is Master mode with RCKI = 128 f_S
1	1	0	Input Port is Master mode with RCKI = 512 f_S
1	1	1	Input Port is Master mode with RCKI = 256 f_S

7.4.3 Bypass Mode

The SRC419x device includes a bypass function, which routes the input port data directly to the output port bypassing the ASRC function. Bypass mode may be invoked by forcing the BYPAS input (pin 9) high for the devices. The bypass mode may also be accessed for the SRC4193 device using the BYPAS bit in Control Register 1. The BYPAS pin and control bit should be set to 0 for normal operation.

No dithering is applied to the output data in bypass mode, and the digital attenuation and mute functions are also unavailable.

7.5 Register Maps

7.5.1 Control Register Map (SRC4193 Device Only)

The control register map for the SRC4193 device is shown in Table 4. Register 0 is reserved for factory use and defaults to all zeros upon reset. Avoid writing this register, as unexpected operation may result if Register 0 is programmed to an arbitrary value. Registers 1 through 5 contain control bits used to configure the internal functions of the SRC4193. All other register addresses are reserved and should not be used in customer applications.

Table 4. SRC4193 Device Control Register Map

Register Address (Dec/Hex)	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
0	0	0	0	0	0	0	0	0
1	$\overline{\text{PDN}}$	TRACK	0	MUTE	BYPAS	MODE2	MODE1	MODE0
2	0	0	0	0	0	0	DFLT	LGRP
3	OWL1	OWL0	OFMT1	OFMT0	0	IFMT2	IFMT1	IFMT0
4	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
5	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0

7.5.1.1 System Control Register

Table 5. System Control Register Field Descriptions

Bit	Field	Description
7	$\overline{\text{PDN}}$	Power Down Setting this bit to 0 sets the SRC4193 to the power-down state. All other register settings are preserved and the SPI port remains active. (Default) Setting this bit to 1 powers up the SRC4193 using the current register settings.
6	TRACK	Digital Attenuation Tracking 0 = Tracking Off: Attenuation for the Left and Right channels is controlled independently. (Default) 1 = Tracking On: Left channel attenuation setting is used for both channels.
5	Reserved	
4	MUTE	Output Soft Mute This bit is logically OR'd with the MUTE input (pin 14) 0 = Soft mute disabled (Default) 1 = Soft mute enabled with data attenuated to all 0s
3	BYPAS	Bypass Mode This bit is logically OR'd with the BYPAS input (pin 9) 0 = Bypass Mode disabled with normal ASRC operation. (Default) 1 = Bypass Mode enabled with data routed directly from the input port to the output port, bypassing the ARSC function.
2-0	MODEx	Audio Serial Port Mode See Table 3.

7.5.1.2 Filter Control Register

Figure 66. Filter Control Register

7	6	5	4	3	2	1	0
Reserved						DFLT	LGRP

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. Filter Control Register Field Descriptions

Bit	Field	Description
7-2	Reserved	
1	DFLT	Decimation Filtering / Direct Down-Sampling The DFLT bit enables or disables the direct down-sampling function. 0 = Decimation filter enabled (default) (Must be used when f_{SOUT} is less than f_{SIN}) 1 = Direct down-sampling enabled without filtering. (May be enabled when f_{SOUT} is equal to or greater than f_{SIN})
0	LGRP	Low Group Delay This bit selects the number of input audio samples to be stored in the data buffer before the ASRC starts processing the audio data. 0 = Normal delay, 64 samples (default) 1 = Low delay, 32 samples

7.5.1.3 Audio Data Format Register

Figure 67. Audio Data Format Register

7	6	5	4	3	2	1	0
OWL1	OWL0	OFMT1	OFMT0	Reserved	IFMT2	IFMT1	IFMT0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. Audio Data Format Register Field Descriptions

Bit	Field	Description
7-6	OWLx	Output Port Data Word Length See Table 2.
5-4	OFMTx	Output Port Data Format See Table 2.
3	Reserved	
2-0	IFMTx	Input Port Data Format See Table 1.

7.5.1.4 Digital Attenuation Register – Left Channel

Figure 68. Digital Attenuation Register – Left Channel

7	6	5	4	3	2	1	0
AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. Digital Attenuation Register – Left Channel Field Descriptions

Bit	Field	Description
7-0	ALx	Register defaults to 00_{HEX}, or 0 dB (unity gain). Output Attenuation (dB) = (–N × 0.5), where N = $AL[7:0]_{DEC}$

7.5.1.5 Digital Attenuation Register – Right Channel

Figure 69. Digital Attenuation Register – Right Channel

7	6	5	4	3	2	1	0
AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. Digital Attenuation Register – Right Channel Field Descriptions

Bit	Field	Description
7-0	ARx	Register defaults to 00_{HEX}, or 0 dB (unity gain). Output Attenuation (dB) = (–N × 0.5), where N = $AR[7:0]_{DEC}$ When the TRACK bit in Control Register 1 is set to 1, the Left Channel attenuation setting will be used for the Right Channel attenuation.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

This section of the data sheet provides practical applications information for hardware and systems engineers designing the SRC4192 and SRC4193 devices into the end equipment.

8.1.1 Interfacing to Digital Audio Receivers and Transmitters

The input and output ports of the SRC4192 and SRC4193 devices are designed to interface to a variety of audio devices, including receivers and transmitters commonly used for AES/EBU, S/PDIF, and CP1201 communications.

Texas Instruments manufactures the DIR1703 digital audio interface receiver and DIT4096/4192 digital audio transmitters to address these applications.

Figure 70 shows interfacing the DIR1703 device to the input port of the SRC4192 or SRC4193 device. The DIR1703 device operates from a single 3.3-V supply, which requires the V_{IO} supply (pin 7) for the SRC4192 or SRC4193 device to be set to 3.3 V for interface compatibility.

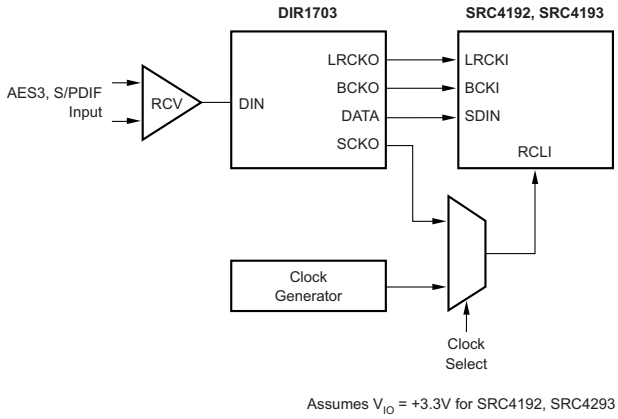
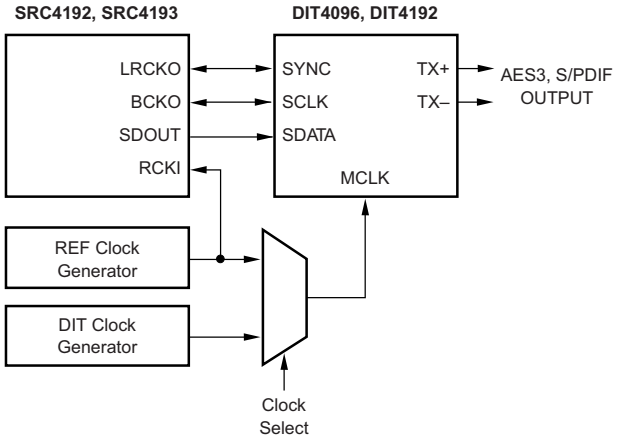


Figure 70. Interfacing the SRC4193 to the DIR1703 Digital Audio Interface Receiver

Figure 71 shows the interface between the output port of the SRC4192 or SRC4193 device and the audio serial port of the DIT4096 or DIT4192 device. Again, the V_{IO} supplies for both the SRC419x device and DIT4096/4192 device are set to 3.3 V for compatibility.

Application Information (continued)



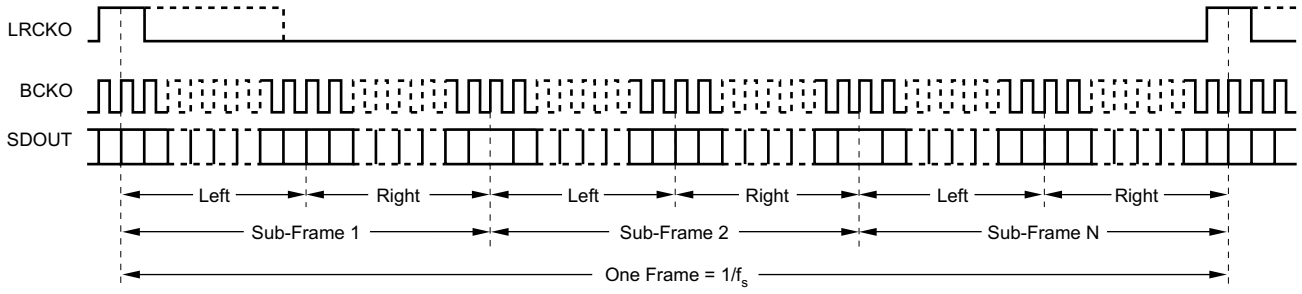
Assumes V_{IO} = +3.3V for SRC4192, SRC4293 and DIT4096, DIT4192

Figure 71. Interfacing the SRC4193 to the DIT4096/4192 Digital Audio Interface Transmitter

Like the output port of the SRC4192 or SRC4193 device, the audio serial port of the DIT4096 and DIT4192 device can be configured as a master or slave. In cases where the output port of the SRC419x device is set to master mode, use the reference clock source (RCKI) as the master clock source (MCLK) for the DIT4096/4192 device, to ensure that the transmitter is synchronized to the output port data of the SRC419x device.

8.1.2 TDM Applications

The SRC4192 and SRC4193 devices support a TDM output mode, which allows multiple devices to be daisy-chained together to create a serial frame. Each device occupies one subframe within a frame, and each sub-frame carries two channels (Left followed by Right). Each sub-frame is 64 bits long, with 32 bits allotted for each channel. The audio data for each channel is left justified within the allotted 32 bits. Figure 72 shows the TDM frame format, while Figure 73 shows TDM input timing parameters, which are listed in *Electrical Characteristics*.



N = Number of Daisy-Chained Devices
One Sub-Frame contains 64 bits, with 32 bits per channel.
For each channel, the audio data is left justified, MSB first format, with the word length determined by the OWL[1:0] pins/bits.

Figure 72. TDM Frame Format

Application Information (continued)

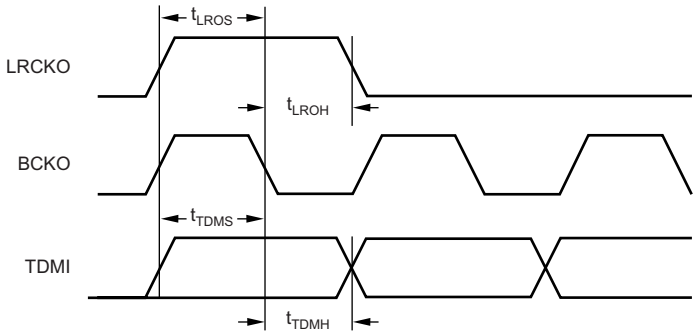


Figure 73. Input Timing for TDM Mode

The frame rate is equal to the output sampling frequency, f_s. The BCKO frequency for the TDM interface is N × 64f_s, where *N* is the number of devices included in the daisy chain. For Master mode, the output BCKO frequency is fixed to the reference clock (RCKI) input frequency. The number of devices that can be daisy-chained in TDM mode is dependent upon the output sampling frequency and the BCKO frequency, leading to the following numerical relationship:

Number of Daisy-Chained Devices = (f_{BCKO} / f_s) / 64 (1)

where

- f_{BCKO} = Output Port Bit Clock (BCKO), 27.648-MHz maximum
- f_s = Output Port Sampling (or LRCKO) Frequency, 216-kHz maximum.

This relationship holds true for both slave and master modes.

Figure 74 and Figure 75 show typical connection schemes for TDM mode. Although the TMS320C671x DSP device family is shown as the audio processing engine in these figures, other TI digital signal processors with a multi-channel buffered serial port (McBSPTM) may also function with this arrangement. Interfacing to processors from other manufacturers is also possible. Refer to Figure 62 in this data sheet, along with the equivalent serial port timing diagrams shown in the DSP data sheet, to determine compatibility.

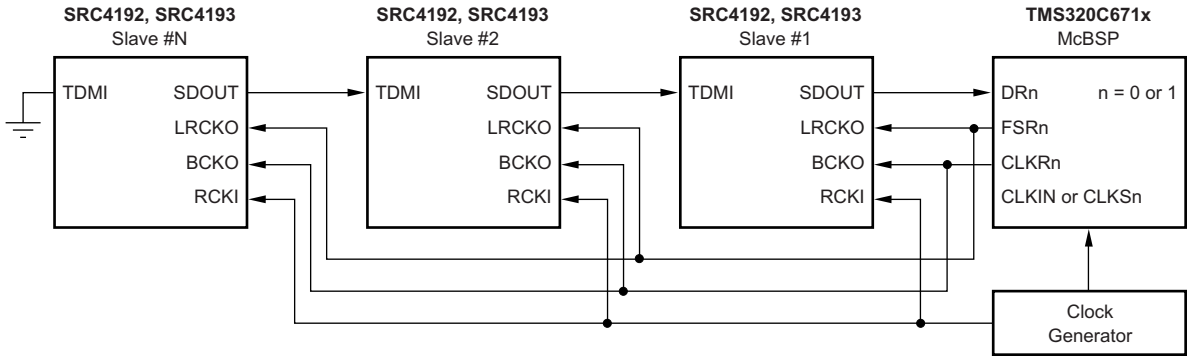


Figure 74. TDM Interface where all Devices are Slaves

Application Information (continued)

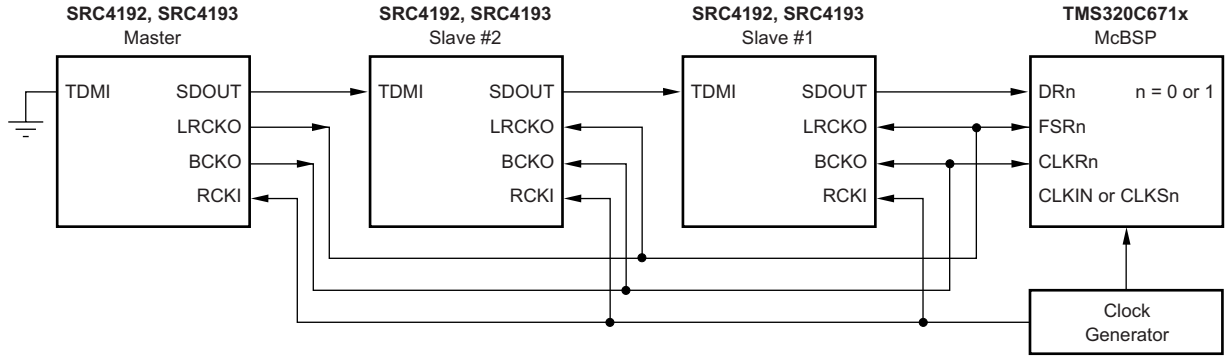


Figure 75. TDM Interface where one Device is Master to Multiple Slaves

8.2 Typical Application

Figure 76 and Figure 77 show typical connection diagrams for the SRC4192 and SRC4193 devices (respectively). Recommended values for power supply bypass capacitors are included. These capacitors should be placed as close to the IC package as possible.

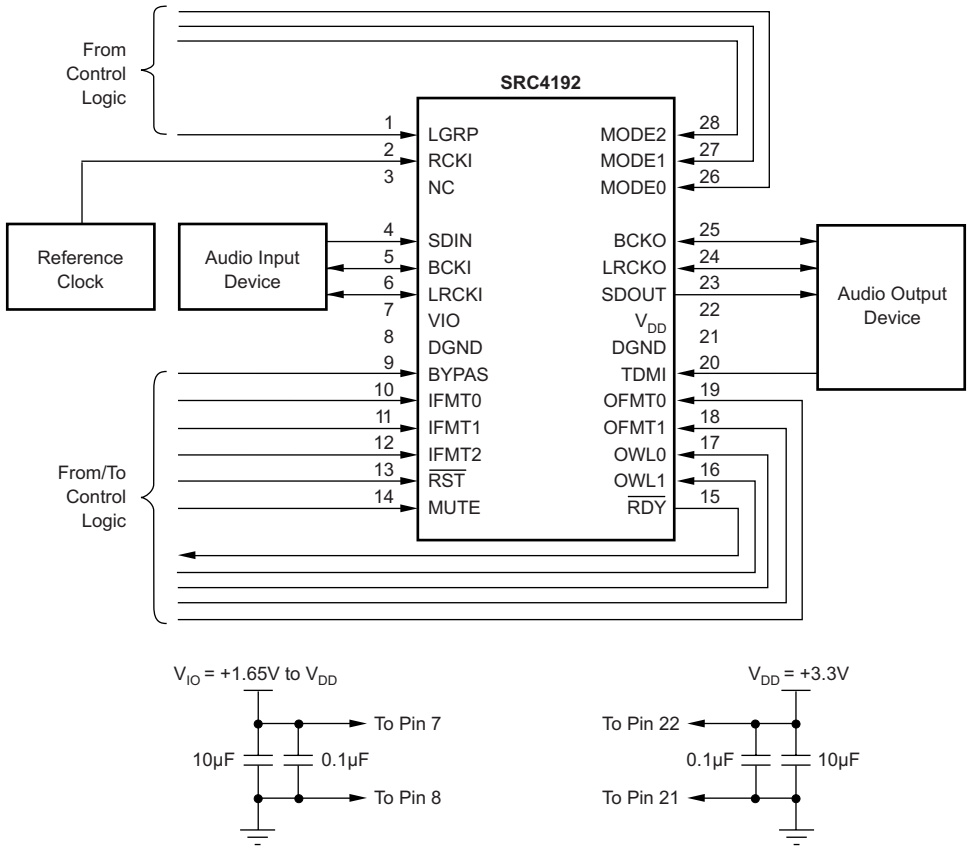


Figure 76. Typical Connection Diagram for the SRC4192

Typical Application (continued)

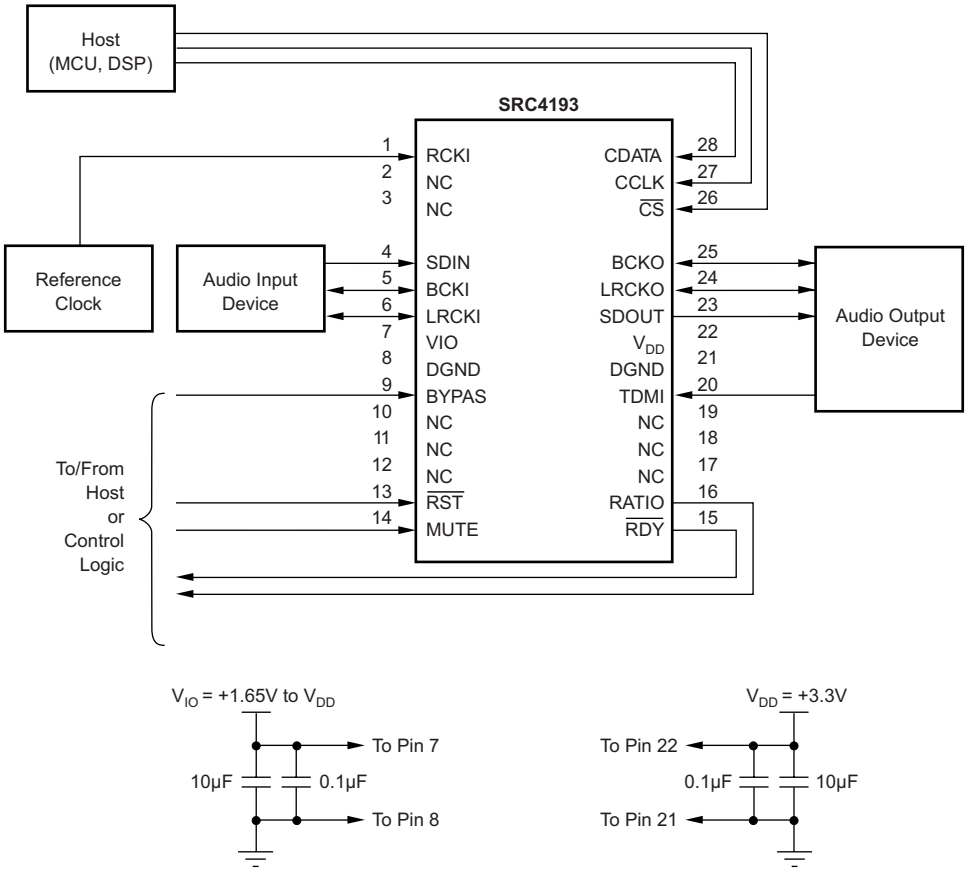


Figure 77. Typical Connection Diagram for the SRC4193

8.2.1 Design Requirements

The following lists design requirements:

- Control: Hardware, I^2C, or SPI
- Audio input: PCM serial data
- Audio output: PCM serial data
- Reference clock

8.2.2 Detailed Design Procedure

8.2.2.1 Control Method

The SRC4192 is a hardware controlled device while the SRC4193 is a software controlled device. The SRC4192 control pins can be connected to V_{DD} or GND directly or by the GPIO of a host controller. The SRC4193 can communicate over a 3 wire SPI.

8.2.2.2 Audio Input and Output

The Audio input and output ports can handle 16, 18, 20, or 24 bit right justified PCM serial data as well as 24 bit I2S or left justified PCM serial data at up to a 212-kHz sampling rate. A TDM format is also available. Both input and output can operate in slave mode, or one can operate as master while the other operates as a slave. A 16:1 or 1:16 is the max ratio supported between the input and output audio sampling rates.

Typical Application (continued)

8.2.3 Application Curves

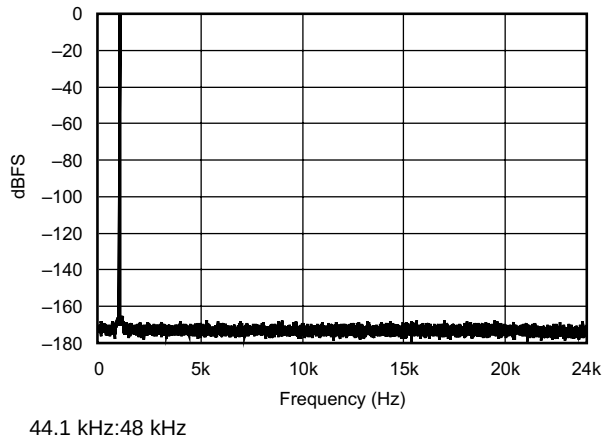


Figure 78. FFT With 1-kHz Input Tone at 0 dBFS

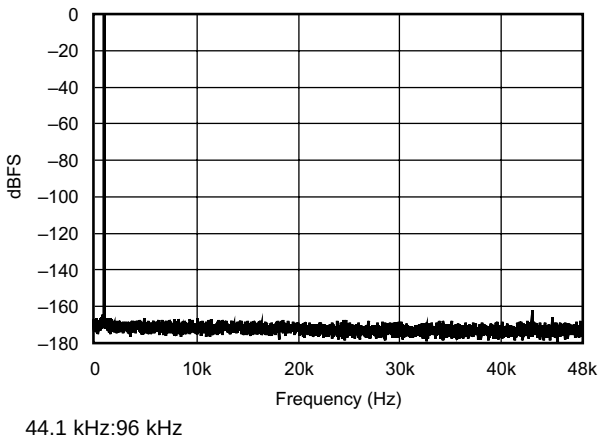


Figure 79. FFT With 1-kHz Input Tone at 0 dBFS

9 Power Supply Recommendations

To ensure compatibility, the VDD_IO and VDD_CORE supplies of the AD1896 device must be set to 3.3 V, while the V_{IO} and V_{DD} supplies of the SRC4192 device must be set to 3.3 V.

10 Layout

10.1 Layout Guidelines

10.1.1 Reference Clock

The SRC4192 and SRC4193 devices require a reference clock for operation. The reference clock is applied at the RCKI input (pin 1 for the SRC4193 device, pin 2 for the SRC4192 device). Figure 80 shows the reference clock connections and requirements for the SRC4192 and SRC4193 devices. The reference clock may operate at $128f_S$, $256f_S$, or $512f_S$, where f_S are the input or output sampling frequency. The maximum external reference clock input frequency is 50 MHz.

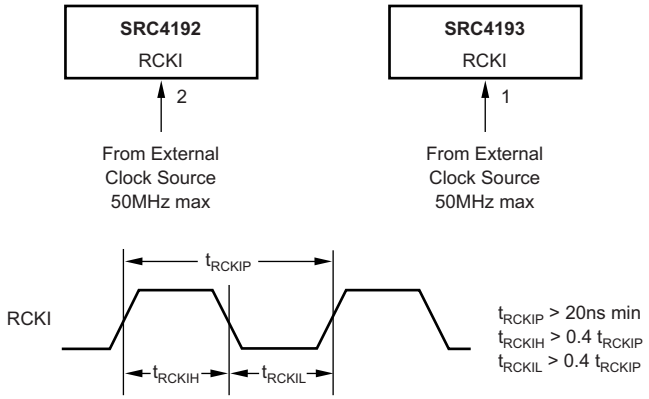


Figure 80. Reference Clock Input Connections and Timing Requirements

Layout Guidelines (continued)

10.1.2 Pin Compatibility With the Analog Devices AD1896 (SRC4192 Only)

The SRC4192 device is pin-and function-compatible with the AD1896 device when observing the guidelines indicated in the following paragraphs.

10.1.2.1 Crystal Oscillator

The SRC4192 does not have an on-chip crystal oscillator. An external reference clock is required at the RCKI input (pin 2).

10.1.2.2 Reference Clock Frequency

The reference clock input frequency for the SRC4192 must be no higher than 30 MHz, to match the master clock frequency specification of the AD1896 device. In addition, the SRC4192 device does not support the $768f_S$ reference clock rate.

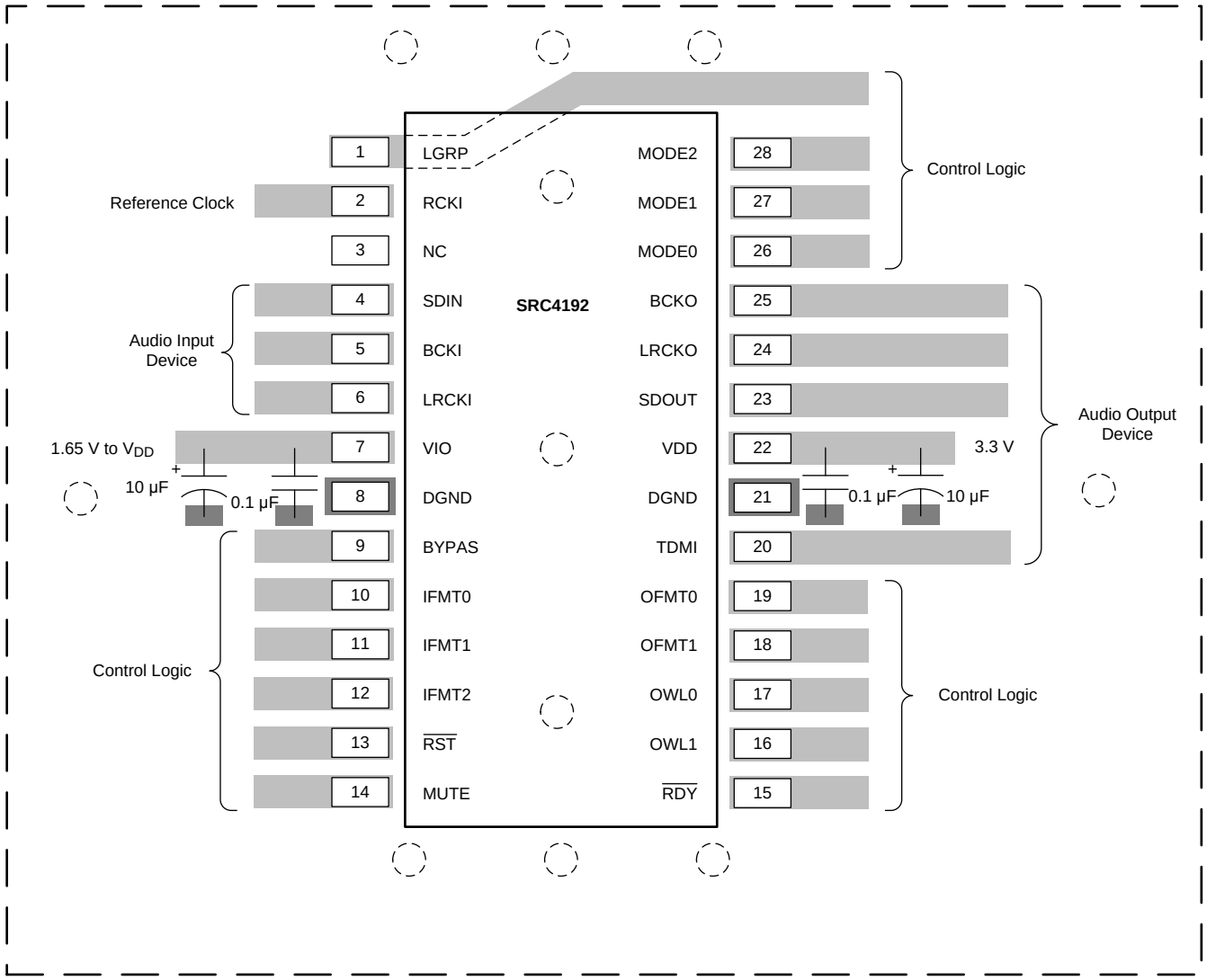
10.1.2.3 Master Mode Maximum Sampling Frequency

When the input or output ports are set to master mode, the maximum sampling frequency must be limited to 96 kHz to support the AD1896 device specification. This is despite the fact that the SRC4192 device supports a maximum sampling frequency of 212 kHz in master mode. The user should consider building an option into their design to support the higher sampling frequency of the SRC4192 device.

10.1.2.4 Matched Phase Mode

Because of the internal architecture of the SRC4192 device, it does not require or support the matched phase mode of the AD1896 device. Given multiple SRC4192 devices, if all reference clock (RCKI) inputs are driven from the same clock source, the devices will be phase-matched.

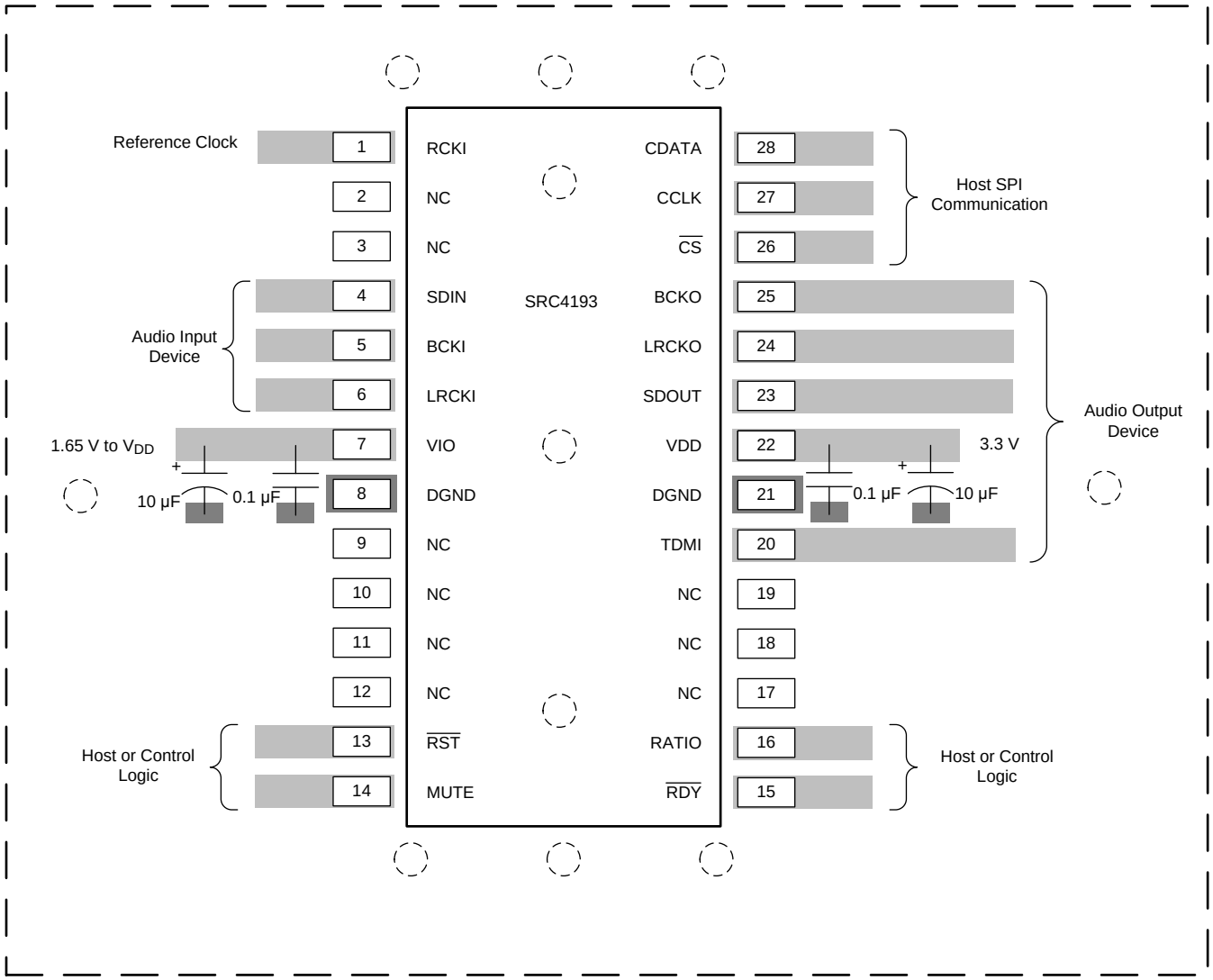
10.2 Layout Example



(1) TI recommends placing a top-layer ground pour for shielding around the SRC4192 device and connecting it to the lower main PCB-ground plane with multiple vias.

Figure 81. SRC4192 Layout Example

Layout Example (continued)



(1) TI recommends placing a top-layer ground pour for shielding around the SRC4193 device and connecting it to the lower main PCB-ground plane with multiple vias.

Figure 82. SRC4193 Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following: *SRC4192EVM Evaluation Module,* SBAU088

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 10. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SRC4192	Click here	Click here	Click here	Click here	Click here
SRC4193	Click here	Click here	Click here	Click here	Click here

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SRC4192IDB	ACTIVE	SSOP	DB	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SRC4192I	Samples
SRC4192IDBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SRC4192I	Samples
SRC4192IDBRG4	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SRC4192I	Samples
SRC4193IDB	ACTIVE	SSOP	DB	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SRC4193I	Samples
SRC4193IDBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SRC4193I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

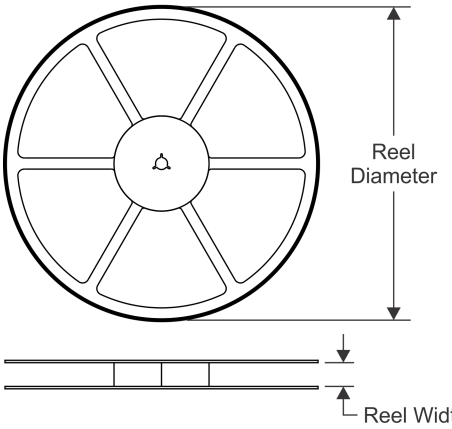
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

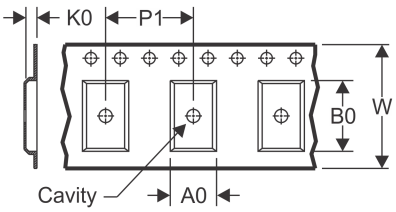
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

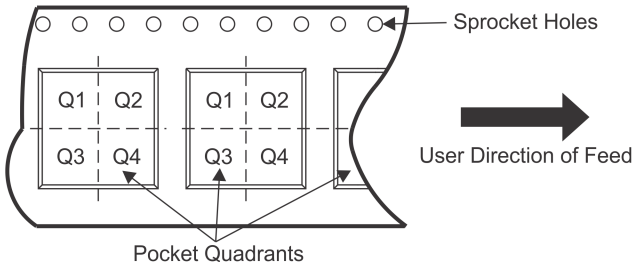


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

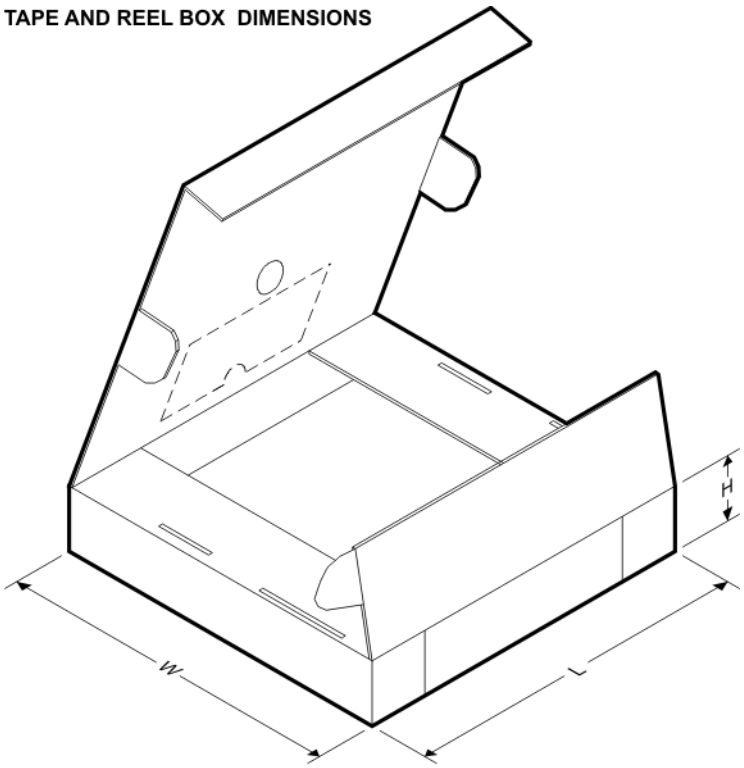
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SRC4192IDBR	SSOP	DB	28	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SRC4193IDBR	SSOP	DB	28	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

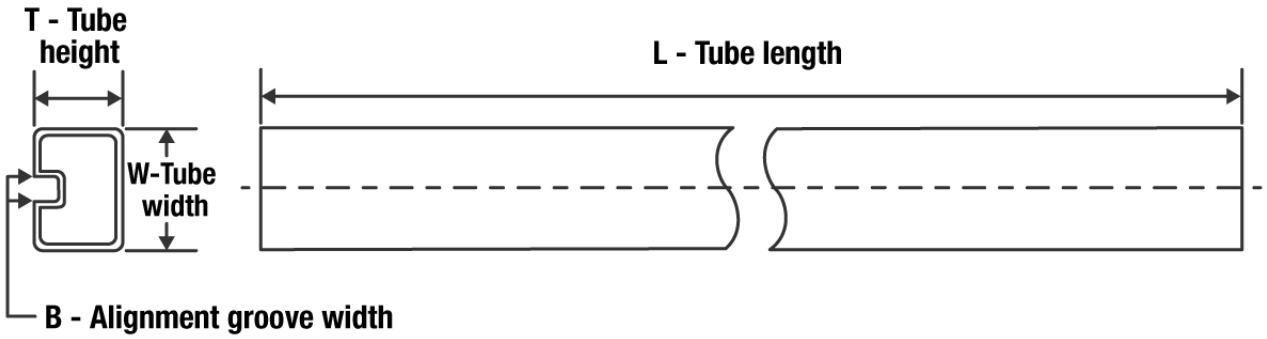
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SRC4192IDBR	SSOP	DB	28	2000	350.0	350.0	43.0
SRC4193IDBR	SSOP	DB	28	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

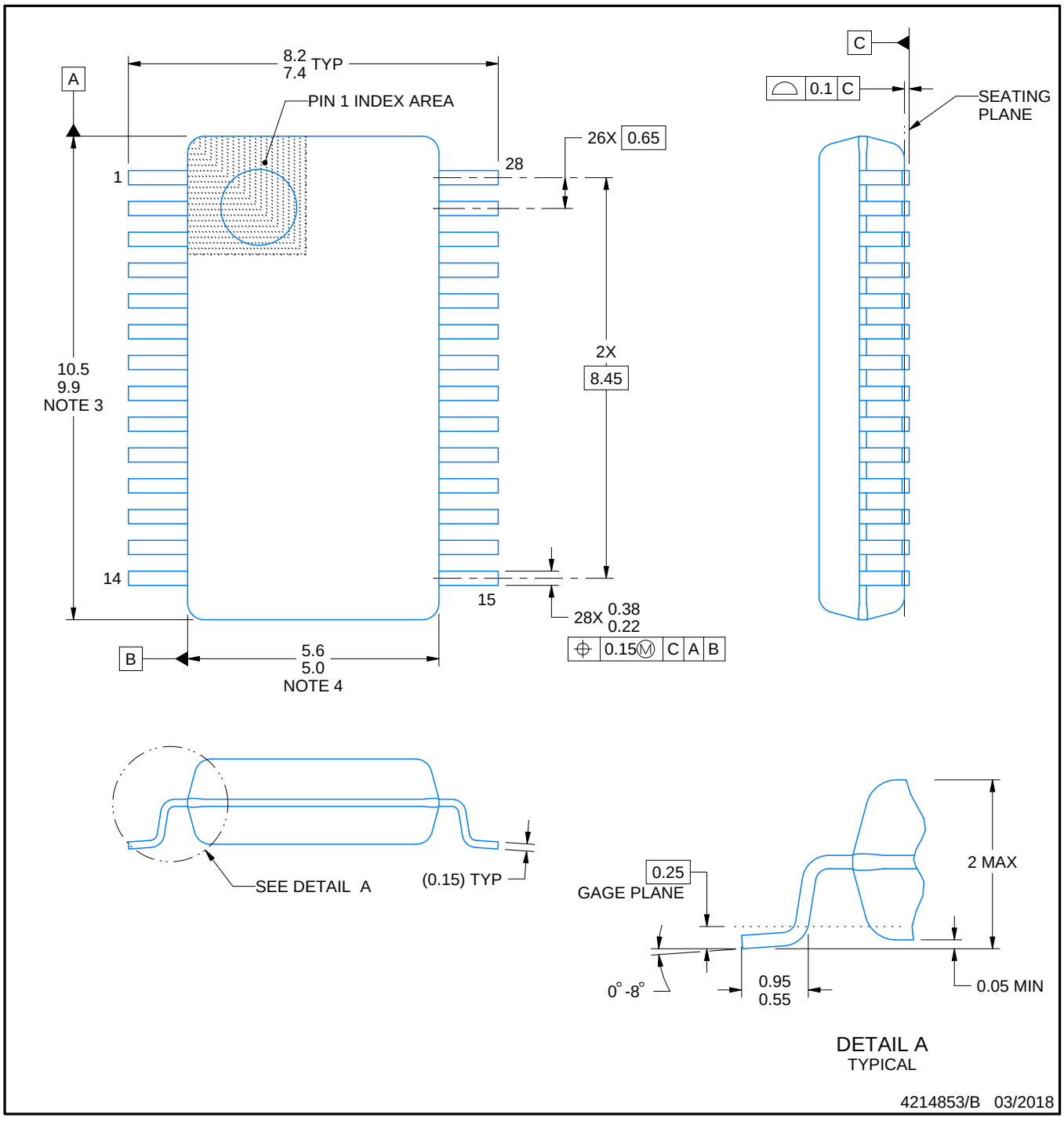
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SRC4192IDB	DB	SSOP	28	50	530	10.5	4000	4.1
SRC4193IDB	DB	SSOP	28	50	530	10.5	4000	4.1

PACKAGE OUTLINE

DB0028A

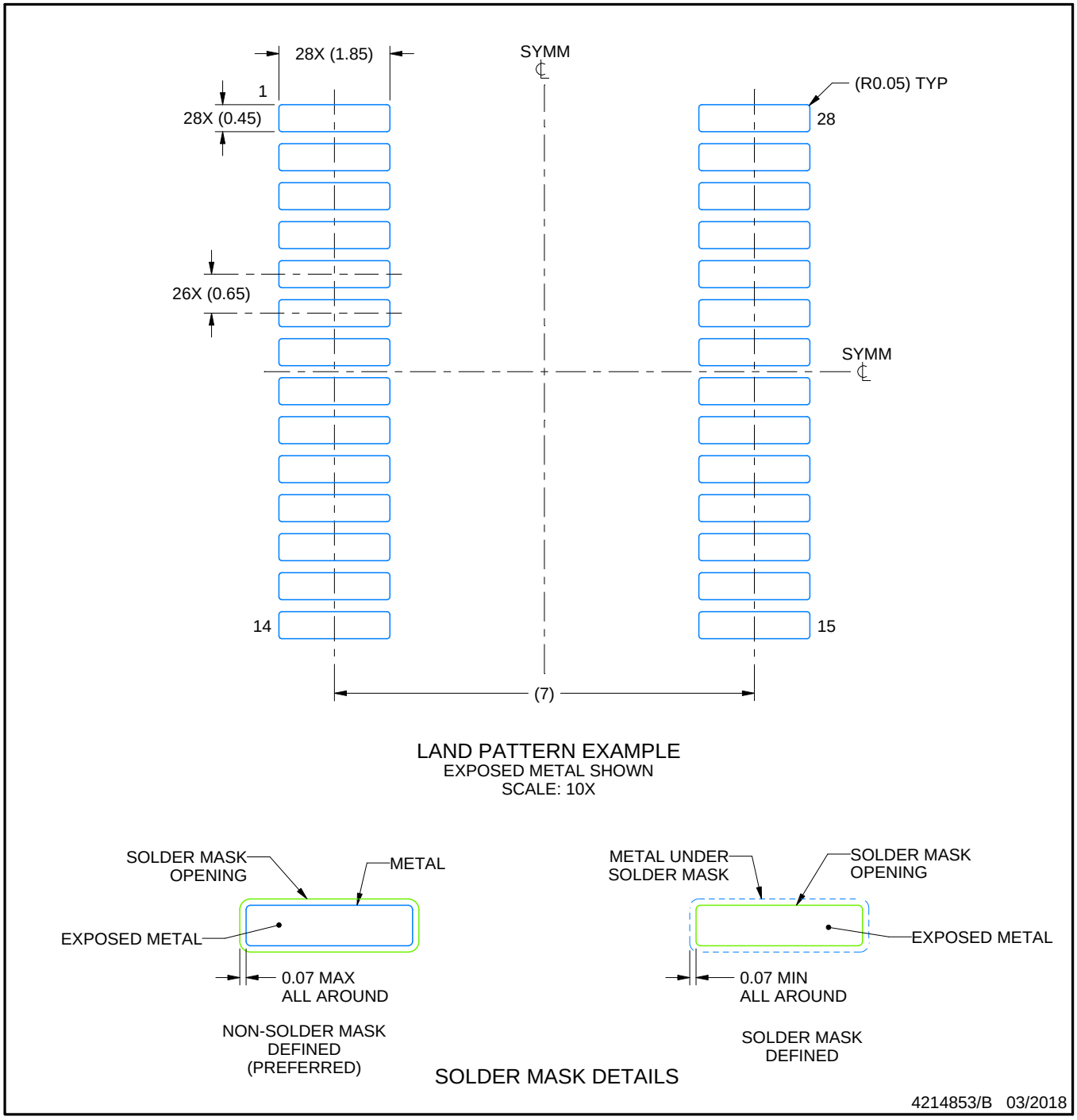
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



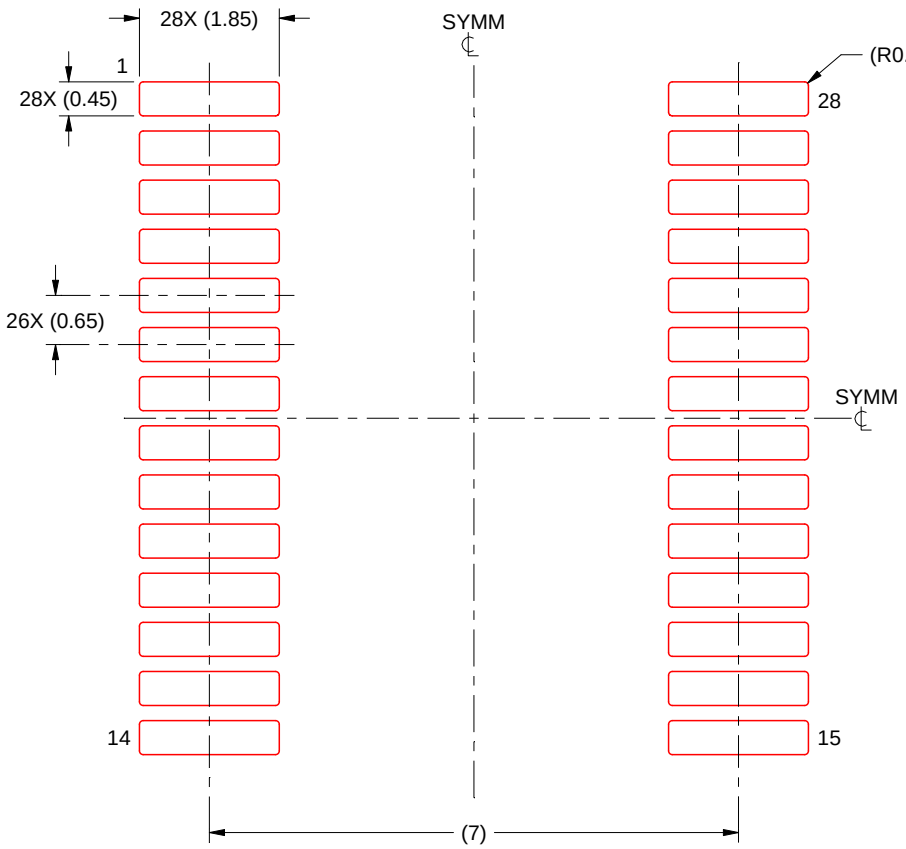
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265